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National Semiconductor

Memory
Databook

- *BiCMOS ECL I/O SRAMs*
- *CMOS EPROMs*
- *CMOS/NMOS EEPROMs*
- *TTL I/O SRAMs*
- *Bipolar PROMs*

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Charlie Sporck

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

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Charlie Sporck

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

MEMORY
DATABOOK

1990 Edition

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Memory Databook Introduction

National Semiconductor's Memory Databook is a comprehensive collection of information on advanced memory products intended to meet the needs of virtually every electronic system being designed today. National Semiconductor is committed to designing and supplying high performance memory products ranging from state-of-the-art static RAMs to programmable non-volatile EPROMs and EEPROMs.

National Semiconductor has an array of advanced technology processes to apply to memory design and development. These range from our unparalleled BiCMOS process used for the industry's most advanced line of high density ECL I/O SRAMs, to our small geometry, silicon gate, oxide isolated CMOS technology which is now producing unsurpassed, high performance EPROM and EEPROM non-volatile memory devices.

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Section 1
CMOS EPROMs

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CMOS EPROMs Non-Volatile Memory Selection Guide

CMOS EPROMs and OTP PROMs

Part No.	Org.	Size	No. of Pins	Access Time	Prog. Volt.	PS Tol.	Temp. Range
NMC27C16Q	2k x 8	16k	24	300, 350, 450, 550	25	5%	0°C to +70°C
NMC27C16QE	2k x 8	16k	24	450	25	5%	−40°C to +85°C
NMC27C32Q	4k x 8	32k	24	300, 350, 450, 550	25	5%	0°C to +70°C
NMC27C32QE	4k x 8	32k	24	450	25	5%	−40°C to +85°C
NMC27C32BQ	4k x 8	32k	24	150, 200, 250	13	5%, 10%	0°C to +70°C
NMC27C32BQE	4k x 8	32k	24	200, 250	13	10%	−40°C to +85°C
NMC27C64Q	8k x 8	64k	28	150	13	5%	0°C to +70°C
NMC27C64Q/N	8k x 8	64k	28	150, 200, 250	13	10%	0°C to +70°C
NMC27C64QE	8k x 8	64k	28	150, 200	13	10%	−40°C to +85°C
NMC27C64QM	8k x 8	64k	28	200, 250	13	10%	−55°C to +125°C
NMC27C128BQ/BN	16k x 8	128k	28	150, 200, 250	13	5%, 10%	0°C to +70°C
NMC27C128BQE	16k x 8	128k	28	150, 200	13	10%	−40°C to +85°C
NMC27C128QM	16k x 8	128k	28	150, 200	13	10%	−55°C to +125°C
NMC27C256Q	32k x 8	256k	28	170, 200, 250	13	5%	0°C to +70°C
NMC27C256Q	32k x 8	256k	28	200, 250, 300	13	10%	0°C to +70°C
NMC27C256QE	32k x 8	256k	28	200, 250	13	10%	−40°C to +85°C
NMC27C256QM	32k x 8	256k	28	250, 350	13	10%	−55°C to +125°C
NMC27C256BQ/BN	32k x 8	256k	28	150, 200, 250	13	5%, 10%	0°C to +70°C
NMC27C256BQE	32k x 8	256k	28	150, 200	13	10%	−40°C to +85°C
NMC27C256BQM	32k x 8	256k	28	150, 200	13	10%	−55°C to +125°C
NMC27C512AQ/AN	64k x 8	512k	28	150, 170, 200, 250	13	5%, 10%	0°C to +70°C
NMC27C512AQE	64k x 8	512k	28	150, 170, 200, 250	13	10%	−40°C to +85°C
NMC27C512ANE	64k x 8	512k	28	150, 170, 200, 250	13	10%	−40°C to +85°C
NMC27C512AQM	64k x 8	512k	28	150, 170, 200, 250	13	10%	−55°C to +125°C
NMC27C010Q	128k x 8	1024k	32	150, 170, 200, 250	13	5%, 10%	0°C to +70°C
NMC27C010QE	128k x 8	1024k	32	150, 170, 200, 250	13	10%	−40°C to +85°C
NMC27C010QM	128k x 8	1024k	32	170, 200, 250	13	10%	−55°C to +125°C
NMC27C1024Q	64k x 16	1024k	40	120, 150, 170, 200, 250	13	5%, 10%	0°C to +70°C
NMC27C1024QE	64k x 16	1024k	40	150, 170, 200	13	10%	−40°C to +85°C
NMC27C1024QM	64k x 16	1024k	40	170, 200	13	10%	−55°C to +125°C

National Semiconductor

ONE TIME PROGRAMMABLE EPROMs

One Time Programmable is the term coined for EPROMs encapsulated in packages without a quartz window. The absence of the quartz window prevents erasure as the EPROM die is no longer capable of being exposed to any source of UV light. Thus the user can program the device only once, thereby giving rise to the term One Time Programmable or OTP.

One Time Programmable EPROMs are frequently packaged in Dual-In-Line Packages (DIP) or surface mount Plastic Leaded Chip Carriers (PLCC).

Dual-In-Line Package

The plastic DIP has lead spacing of 0.100 inch and is particularly advantageous for users of EPROMs that are in high volume production. Plastic being less brittle than ceramic, the PDIPs can be used with auto insertion equipment, thereby offering an additional advantage to high volume users by reducing manufacturing throughput time.

Density	Product Nomenclature
64 kbit	NMC27C64N
128 kbit	NMC27C128BN
256 kbit	NMC27C256BN
512 kbit	NMC27C512AN

Surface Mount Package

Plastic Leaded Chip Carriers (PLCC) allow for a three to one improvement in surface mounting density over the plastic DIP, due to the tighter lead spacings of 0.050 inch. As the leads bond to the surface of the board (vs. through hole mounting for DIPs), system design engineers can optimize their PC board density by placing components on both sides of the PC board.

These packages are advantageous for cost sensitive, high volume users that are board space constrained and want to increase their manufacturing throughput with the aid of auto insertion equipment.

National Semiconductor's scheduled introduction of a broad range of high density EPROMs in PLCC through early 1990 include:

Density	Product Nomenclature
128 kbit	NMC27C128BV
256 kbit	NMC27C256BV
512 kbit	NMC27C512AV
1 Mbit (×8)	NMC27C010V
1 Mbit (×16)	NMC27C1024V

National Semiconductor has had many years of experience building surface mount packages. The company has an excellent reputation in the industry for product reliability. EPROMs in both the Plastic Dual-In-Line Package and the Plastic Leaded Chip Carrier will be built with the same stringent reliability standards as other National products.

National Semiconductor

NMC27C16
16,384-Bit (2048 x 8) UV Erasable CMOS PROM

General Description

The NMC27C16 is a high speed 16k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

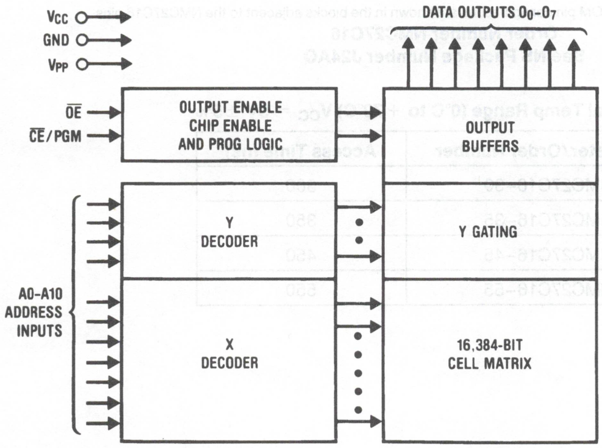
The NMC27C16 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, P²CMOS™ silicon gate technology.

Features

- Access time down to 300 ns
- Low CMOS power consumption
  - — Active Power: 26.25 mW max
  - — Standby Power: 0.53 mW max (98% savings)
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range available (NMC27C16E-45), −40°C to +85°C, 450 ns ±5% power supply
- Pin compatible to MM2716 and higher density EPROMs
- Static—no clocks required
- TTL compatible inputs/outputs
- TRI-STATE® output

Block Diagram


V_{CC}
GND
V_{PP}
$\overline{OE}$
$\overline{CE}$/PGM
OUTPUT ENABLE CHIP ENABLE AND PROG LOGIC
DATA OUTPUTS O_0–O_7
OUTPUT BUFFERS
Y DECODER
Y GATING
A0-A10 ADDRESS INPUTS
X DECODER
16,384-BIT CELL MATRIX

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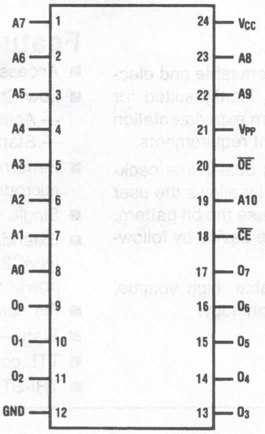
Pin Names

A0–A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

Dual-In-Line Package
NMC27C16


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O0 9
O1 10
O2 11
GND 12
24 VCC
23 A8
22 A9
21 VPP
20 OE
19 A10
18 CE
17 O7
16 O6
15 O5
14 O4
13 O3

27C32 2732	27C64 2764	27C128 27128	27C256 27256
	V_{CC}	V_{CC}	V_{CC}
	$\overline{\text{PGM}}$	$\overline{\text{PGM}}$	A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
A11	A11	A11	A11
$\overline{\text{OE}}/V_{PP}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$
A10	A10	A10	A10
$\overline{\text{CE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

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Top View

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C16 pins.

Order Number NMC27C16
See NS Package Number J24AQ

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C16-30	300
NMC27C16-35	350
NMC27C16-45	450
NMC27C16-55	550

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.3V
All Output Voltages with Respect to Ground (Note 11)	V_{CC}+0.3V to GND−0.3V
V_{PP} Supply Voltage with Respect to Ground During Programming	+26.5V to −0.3V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 9)

Temperature Range	
NMC27C16-30, -35, -45, -55	0°C to +70°C
NMC27C16E-45	−40°C to +85°C
V_{CC} Power Supply (Notes 2 and 3)	5V ±5%
V_{PP} Power Supply (Note 3)	V_{CC}

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	µA
I_{CC1} (Note 3)	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = \overline{CE} = V_{IL}$, f = 1 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		2	10	mA
I_{CC2} (Note 3)	V_{CC} Current (Active) CMOS Inputs	$\overline{OE} = \overline{CE} = V_{IL}$, f = 1 MHz Inputs = V_{CC} or GND, I/O = 0 mA		1	5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.01	0.1	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 µA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 µA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C16								Units
			-30		-35		E-45, -45		-55		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		300		350		450		550	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		300		350		450		550	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		120		120		120		160	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	100	0	100	0	100	0	100	ns
t_{OH} (Note 5)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 5)

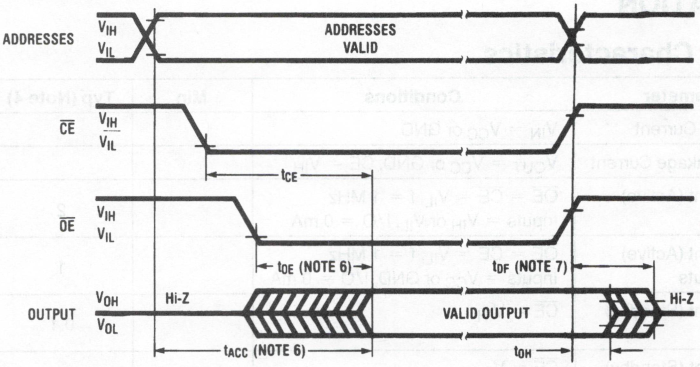
Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.8V to 2.2V

Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 2, 8, 9, 10)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. $I_{CC1} \leq$ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 5: This parameter is only sampled and is not 100% tested.

Note 6: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 7: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) $-$ 0.10V
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V

Note 8: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 9: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 10: The NMC27C16 requires one address transition after initial power-up to reset the outputs.

Note 11: The outputs must be restricted to V_{CC} + 0.3V to avoid latch-up and device damage.

PROGRAMMING CHARACTERISTICS (Note 1)

DC Programming Characteristics (Notes 2 & 3)

(T_A = +25°C ±5°C, V_{CC} = 5V ±5%, V_{PP} = 25V ±1V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (for Any Input)	$V_{IN} = V_{CC}$ or GND			10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}/PGM = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
V_{IL}	Input Low Level		−0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V

AC Programming Characteristics (Notes 2 & 3)

(T_A = +25°C ±5°C, V_{CC} = 5V ±5%, V_{PP} = 25V ±1V)

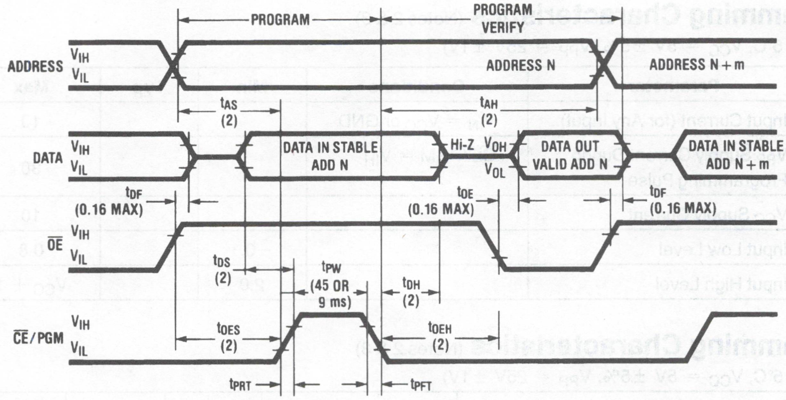
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		2			µs
t_{OEH}	$\overline{OE}$ Hold Time		2			µs
t_{DH}	Data Hold Time		2			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/PGM = V_{IL}$	0		160	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}/PGM = V_{IL}$			160	ns
t_{PW}	Program Pulse Width		45	50	55	ms
t_{PRT}	Program Pulse Rise Time		5			ns
t_{PFT}	Program Pulse Fall Time		5			ns

AC Test Conditions

V_{CC}	5V ±5%
V_{PP}	25V ±1V
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.8V to 2.2V

Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3) $V_{PP} = 25V \pm 1V$, $V_{CC} = 5V \pm 5\%$



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Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C16 must not be inserted into or removed from a board with V_{PP} at 25V ±1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C16 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are a 5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other three modes.

Read Mode

The NMC27C16 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$. The NMC27C16 requires one address transition after initial power-up to reset the outputs.

Standby Mode

The NMC27C16 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53 mW. The NMC27C16 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C16s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 21 (V_{PP}) will damage the NMC27C16.

Initially, and after each erasure, all bits of the NMC27C16 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C16 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. It is required that a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The NMC27C16 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Functional Description (Continued)

Programming multiple NMC27C16s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C16s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{\text{CE}}$/PGM input programs the paralleled NMC27C16s.

Program Inhibit

Programming multiple NMC27C16s in parallel with different data is also easily accomplished. Except for $\overline{\text{CE}}$/PGM, all like inputs (including $\overline{\text{OE}}$) of the parallel NMC27C16s may be common. A TTL level program pulse applied to an NMC27C16's $\overline{\text{CE}}$/PGM input with V_{PP} at 25V will program that NMC27C16. A low level $\overline{\text{CE}}$/PGM input inhibits the other NMC27C16 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 25V. V_{PP} must be at V_{CC}, except during programming and program verify.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C16 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Opaque labels should be placed over the NMC27C16 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C16 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The NMC27C16 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Note: The NMC27C16-55 may take up to 60 minutes for complete erasure to occur.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE I. Mode Selection

Pins Mode	$\overline{\text{CE}}$/PGM (18)	$\overline{\text{OE}}$ (20)	V_P (21)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	25	5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	25	5	Hi-Z
Output Disable	X	V_{IH}	V_{CC}	5	Hi-Z

National Semiconductor

NMC27C32
32,768-Bit (4096 x 8) UV Erasable CMOS PROM

General Description

The NMC27C32 is a high speed 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

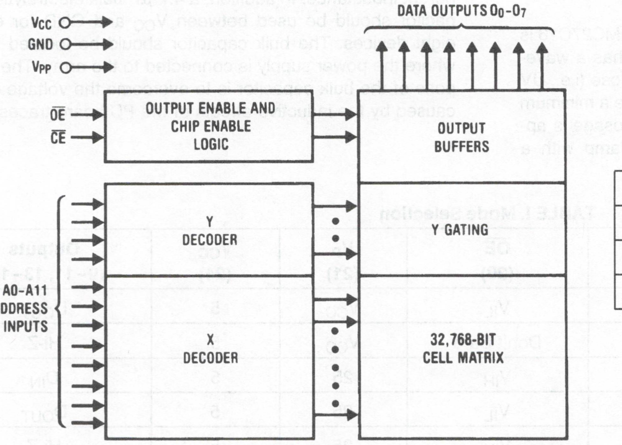
The NMC27C32 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, p²CMOS™ silicon gate technology.

Features

- Access time down to 300 ns
- Low CMOS power consumption
  Active power: 26.25 mW max
  Standby power: 0.53 mW max (98% savings)
- Extended temperature range available (NMC27C32E-45 and NMC27C32HE-45), −40°C to +85°C, 450 ns ±5% power supply
- 10 ms programming available (NMC27C32H), an 80% time savings
- Pin compatible to NMC2732 and higher density EPROMs
- Static-no clocks required
- TTL compatible inputs/ outputs
- Two-line control
- TRI-STATE® output

Block Diagram


DATA OUTPUTS O_0–O_7
V_{CC}
GND
V_{PP}
$\overline{OE}$
$\overline{CE}$
OUTPUT ENABLE AND CHIP ENABLE LOGIC
OUTPUT BUFFERS
Y DECODER
Y GATING
A0–A11 ADDRESS INPUTS
X DECODER
32,768-BIT CELL MATRIX

TL/D/5274–1

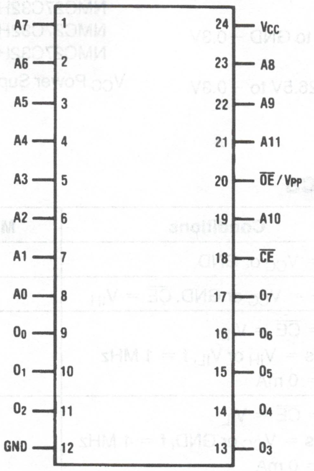
Pin Names

A0–A11	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C16 2716
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

NMC27C32
Dual-In-Line Package


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O_0 9
O_1 10
O_2 11
GND 12
13 O_3
14 O_4
15 O_5
16 O_6
17 O_7
18 $\overline{CE}$
19 A10
20 $\overline{OE}$/V_{PP}
21 A11
22 A9
23 A8
24 V_{CC}

27C216 27216	27C64 2764	27C128 27128	27C256 27256
	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
V_{PP}	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

TL/D/5274-2

Top View

Order Number NMC27C32

See NS Package Number J24AQ

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32 pins.

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C32-30, NMC27C32H-30	300
NMC27C32-35, NMC27C32H-35	350
NMC27C32-45, NMC27C32H-45	450
NMC27C32-55, NMC27C32H-55	550

Extended Temp Range (−40°C to +85°C) V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C32E-45, NMC27C32EH-45	450

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.3V
All Output Voltages with Respect to Ground	V_{CC} + 0.3V to GND −0.3V
V_{PP} Supply Voltage with Respect to Ground during Programming	+26.5V to −0.3V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 7)

Temperature Range	
NMC27C32-30, NMC27C32-35, NMC27C32-45, NMC27C32-55, NMC27C32H-30, NMC27C32H-35, NMC27C32H-45, NMC27C32H-55	0°C to +70°C
NMC27C32HE-45, NMC27C32E-45	−40°C to +85°C
V_{CC} Power Supply	5V ±5%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IH} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{IH} or V_{IL}, f = 1 MHz I/O = 0 mA		2	10	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{CC} or GND, f = 1 MHz I/O = 0 mA		1	5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.01	0.1	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C32								Units
			-30, H-30		-35, H-35		-45, H-45 E-45; HE-45		-55, H-55		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		300		350		450		550	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		300		350		450		550	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		150		150		150		150	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	130	0	130	0	130	0	130	ns
t_{OH} (Note 3)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

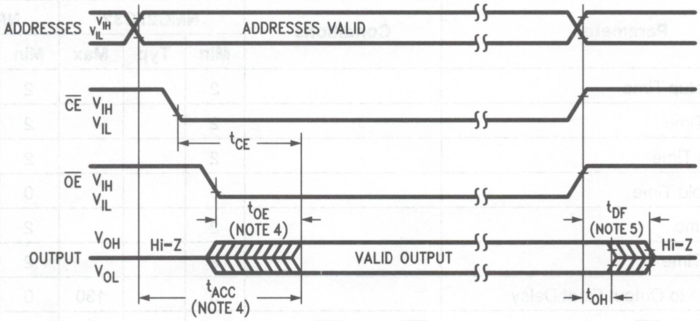
Capacitance $T_A = +25°C$, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$		20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF	Timing Measurement Reference Level	
		Inputs	1V and 2V
		Outputs	0.8V and 2V
Input Rise and Fall Times	≤20 ns		
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6 & 8)



TL/D/5274-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 0.3V to avoid latch-up and device damage.

PROGRAMMING (Note 1)

DC Programming Characteristics

$T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{CC}$ or GND			10	µA
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400$ µA	2.4			V
I_{CC}	V_{CC} Supply Current			2	10	mA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level (All Inputs except $\overline{\text{OE}}/V_{PP}$)		2.0		$V_{CC} + 1$	V
I_{PP}	V_{PP} Supply Current	$\overline{\text{CE}} = V_{IL}$, $\overline{\text{OE}} = V_{PP}$			30	mA

AC Programming Characteristics

$T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$

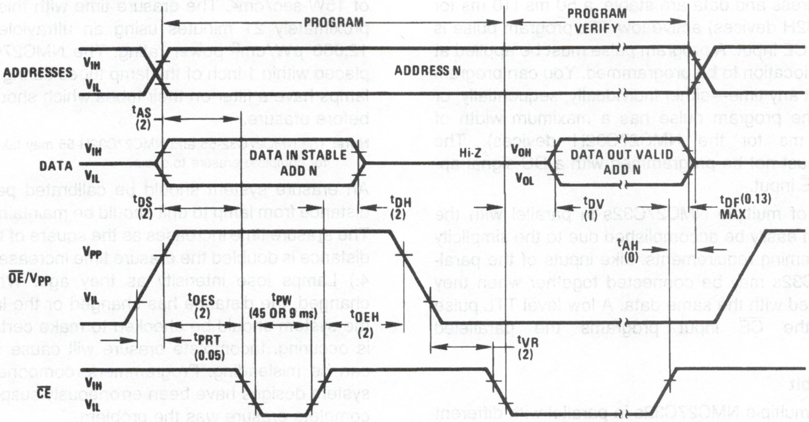
Symbol	Parameter	Conditions	NMC27C32			NMC27C32H			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AS}	Address Setup Time		2			2			µs
t_{OES}	$\overline{\text{OE}}$ Setup Time		2			2			µs
t_{DS}	Data Setup Time		2			2			µs
t_{AH}	Address Hold Time		0			0			µs
t_{OEH}	$\overline{\text{OE}}$ Hold Time		2			2			µs
t_{DH}	Data Hold Time		2			2			µs
t_{DF}	Chip Enable to Output Float Delay		0		130	0		130	ns
t_{DV}	Data Valid from $\overline{\text{CE}}$	$\overline{\text{CE}} = V_{IL}$, $\overline{\text{OE}} = V_{IL}$			1			1	µs
t_{PW}	$\overline{\text{CE}}$ Pulse Width during Programming		45	50	55	9	10	11	ms
t_{PRT}	$\overline{\text{OE}}$ Pulse Rise Time during Programming		50			50			ns
t_{VR}	V_{PP} Recovery Time		2			2			µs

AC Test Conditions

V_{CC}	5V ± 5%
V_{PP}	25V ± 1V
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3)



TL/D/5274-4

Note: All times shown in parentheses are minimum and in μs unless otherwise specified..
The input timing reference level is 1V for a V_{IL} and 2V for a V_{IH}.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must not be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C32 must not be inserted into or removed from a board with V_{PP} at 25V ± 1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description (Continued)

DEVICE OPERATION

The 6 modes of operation of the NMC27C32 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

Read Mode

The NMC27C32 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The NMC27C32 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53 mW. The NMC27C32 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMS are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 20 (V_{PP}) will damage the NMC27C32.

Initially, and after each erasure, all bits of the NMC27C32 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

Functional Description (Continued)

The NMC27C32 is in the programming mode when the $\overline{\text{OE}}/V_{PP}$ input is at 25V. It is required that a 0.1 μF capacitor be placed across $\overline{\text{OE}}/V_{PP}$, V_{CC}, and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms (10 ms for the NMC27C32H devices) active low TTL program pulse is applied to the $\overline{\text{CE}}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms (11 ms for the NMC27C32H devices). The NMC27C32 must not be programmed with a DC signal applied to the $\overline{\text{CE}}$ input.

Programming of multiple NMC27C32s in parallel with the same data can easily be accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{\text{CE}}$ input programs the paralleled NMC27C32s.

Program Inhibit

Programming multiple NMC27C32s in parallel with different data is also easily accomplished. Except for $\overline{\text{CE}}$, all like inputs (including $\overline{\text{OE}}$) of the parallel NMC27C32s may be common. A TTL level program pulse applied to an NMC27C32's $\overline{\text{CE}}$ input with $\overline{\text{OE}}/V_{PP}$ at 25V will program that NMC27C32. A high level $\overline{\text{CE}}$ input inhibits the other NMC27C32s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{\text{OE}}/V_{PP}$ and $\overline{\text{CE}}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{\text{CE}}$.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C32 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C32 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The NMC27C32 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Note: The NMC27C32-55 and NMC27C32H-55 may take up to 60 minutes for complete erasure to occur.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE I. Mode Selection

Pins Mode	$\overline{\text{CE}}$ (18)	$\overline{\text{OE}}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	V_{IL}	5	D_{OUT}
Standby	V_{IH}	Don't Care	5	Hi-Z
Output Disable	Don't Care	V_{IH}	5	Hi-Z
Program	V_{IL}	V_{PP}	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	5	Hi-Z

National Semiconductor

PRELIMINARY

NMC27C32B 32,768-Bit (4k x 8) High Speed Version UV Erasable CMOS PROM

General Description

The NMC27C32B is a high-speed 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C32B is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over the Extended Temperature Range.

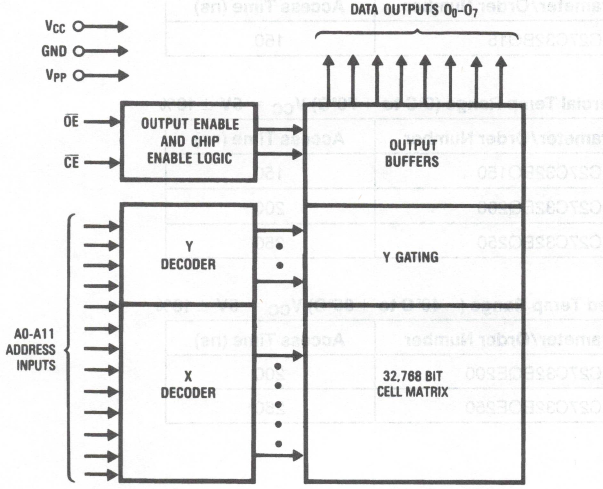
The NMC27C32B is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active Power 55 mW Max
  - — Standby Power 0.55 mW Max
- Optimal EPROM for total CMOS systems
- Single 5V power supply
- Extended temperature range (NMC27C32BQE), −40°C to +85°C, available
- Pin compatible with NMOS 32k EPROMs
- Fast and reliable programming—100 μs typical/byte
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/8827-1

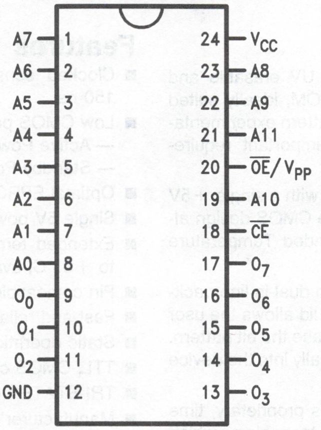
Pin Names

A0–A11	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/ Programming Voltage
O_0–O_7	Outputs

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C16 2716
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

NMC27C32B
Dual-In-Line Package


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O_0 9
O_1 10
O_2 11
GND 12
24 V_{CC}
23 A8
22 A9
21 A11
20 $\overline{\text{OE}}/V_{PP}$
19 A10
18 $\overline{\text{CE}}$
17 O_7
16 O_6
15 O_5
14 O_4
13 O_3

27C16 2716	27C64 2764	27C128 27128	27C256 27256
	V_{CC}	V_{CC}	V_{CC}
	$\overline{\text{PGM}}$	$\overline{\text{PGM}}$	A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
V_{PP}	A11	A11	A11
$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$
A10	A10	A10	A10
$\overline{\text{CE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

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Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32B pins.

Order Number NMC27C32BQ
See NS Package Number J24AQ

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C32BQ15	150

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQ150	150
NMC27C32BQ200	200
NMC27C32BQ250	250

Extended Temp Range (−40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQE200	200
NMC27C32BQE250	250

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Extended Temp Parts	Operating Temp
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 and $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 9)	V_{CC}+1.0V to GND−0.6V
$\overline{OE}$ V_{PP} Supply and A9 Voltage with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

Temperature Range	
NMC27C32BQ150, 200, 250	0°C to +70°C
NMC27C32BQE200, 250	−40°C to +85°C
V_{CC} Power Supply	+5V ±10%
except NMC27C32BQ15	+5V ±5%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	µA
I_{PP}	$\overline{OE}/V_{PP}$ Load Current	$\overline{OE}/V_{PP} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	µA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 1 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		8	20	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 1 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 µA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 µA	$V_{CC} - 0.1$			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C32B						Units
			Q15, Q150		Q200, QE200		Q250, QE250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60		70	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	60	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	6	8	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	25	28	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

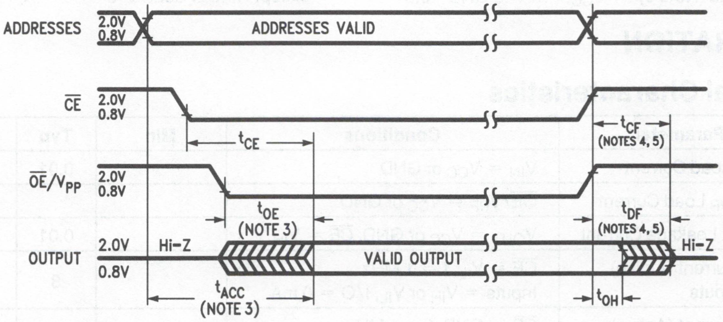
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 7)



TL/D/8827-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

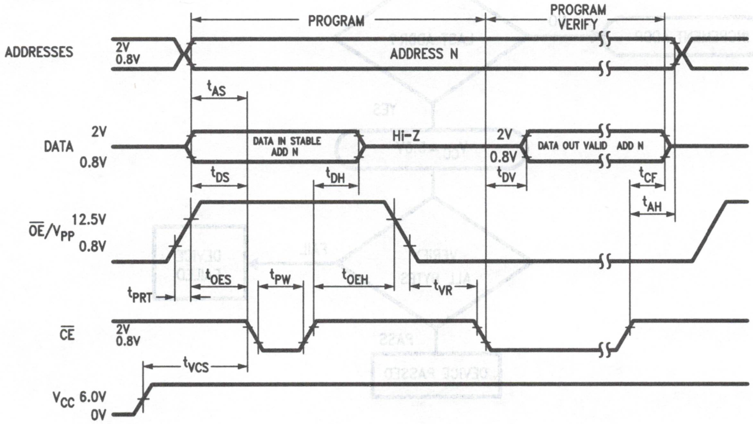
Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to $-2.0V$ for 20 ns Max, except for $\overline{OE}/V_{PP}$ which cannot exceed $-0.2V$.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OEH}	$\overline{OE}$ Hold Time		1			ns
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			µs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms



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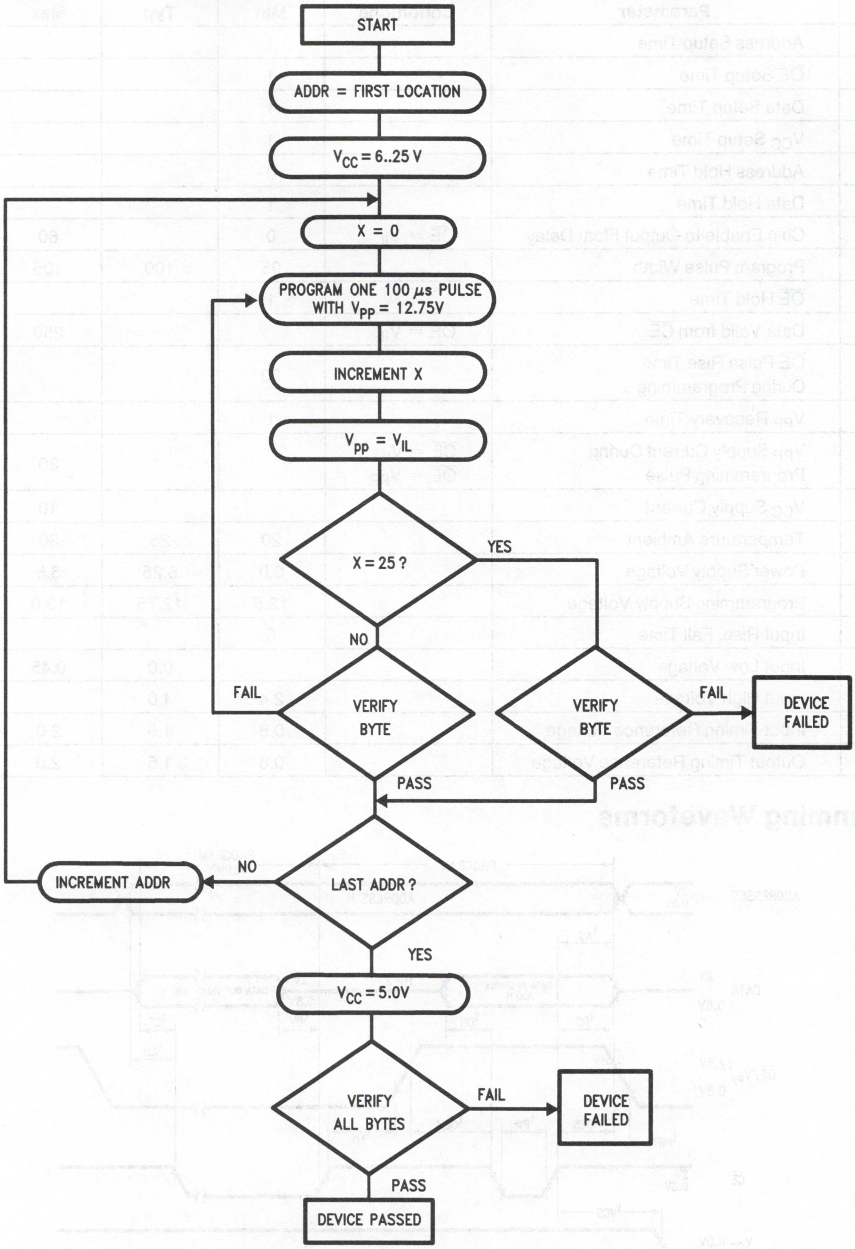
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

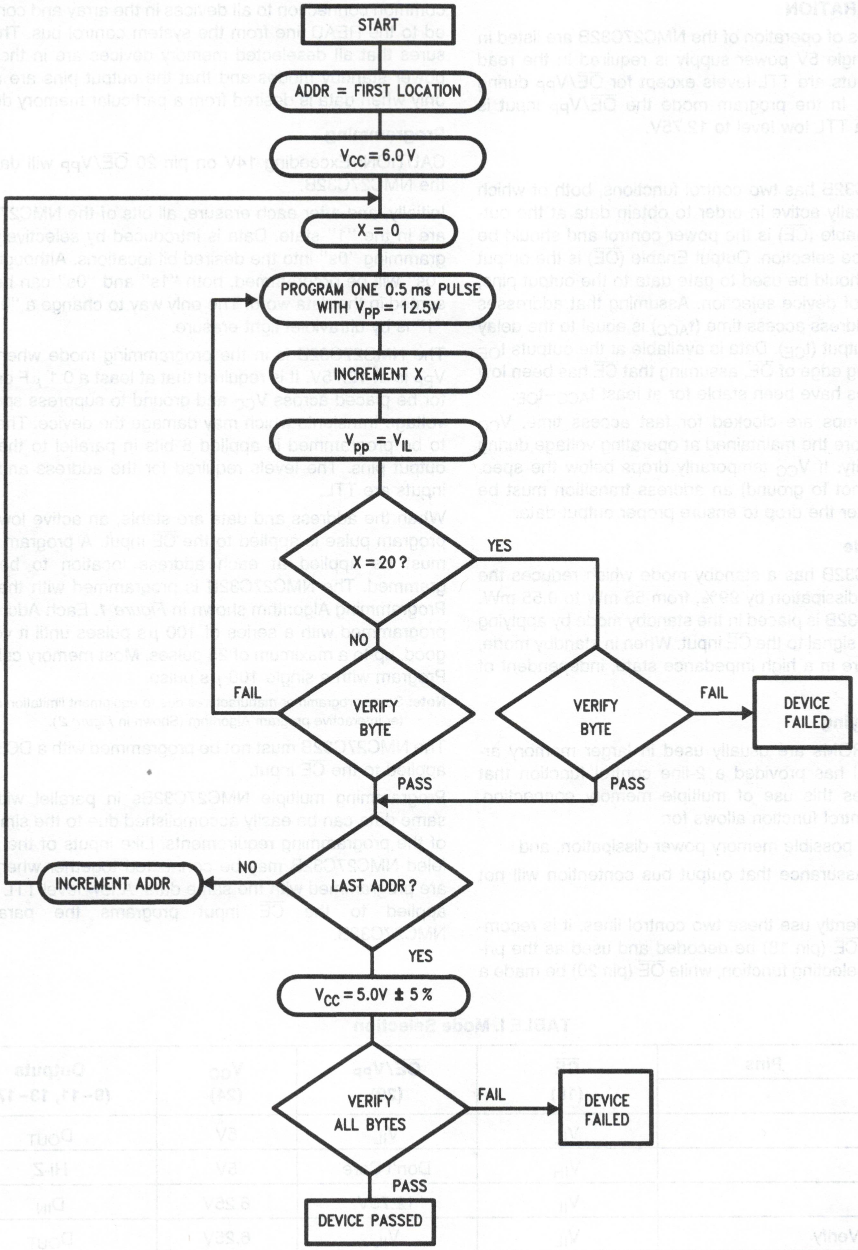
Fast Programming Algorithm Flow Chart (Note 4)


START
ADDR = FIRST LOCATION
V_{CC} = 6..25 V
X = 0
PROGRAM ONE 100 μs PULSE WITH V_{PP} = 12.75V
INCREMENT X
V_{pp} = V_{IL}
X = 25 ?
YES
NO
FAIL
VERIFY BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC} = 5.0V
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

TL/D/8827–5

FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)


START
ADDR = FIRST LOCATION
V_{CC} = 6.0 V
X = 0
PROGRAM ONE 0.5 ms PULSE WITH V_{PP} = 12.5V
INCREMENT X
V_{PP} = V_{IL}
X = 20 ?
YES
NO
FAIL
VERIFY BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
INCREMENT ADDR
NO
LAST ADDR ?
YES
V_{CC} = 5.0V ± 5 %
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

TL/D/8827–6

FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C32B are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 12.75V.

Read Mode

The NMC27C32B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore the maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C32B has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C32B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a. The lowest possible memory power dissipation, and

b. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 20 $\overline{OE}/V_{PP}$ will damage the NMC27C32B.

Initially, and after each erasure, all bits of the NMC27C32B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C32B is in the programming mode when $\overline{OE}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C32B is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will Program with a single 100 μs pulse.

Note: Some programmer manufactures due to equipment limitation may offer interactive program Algorithm (Shown in *Figure 2*).

The NMC27C32B must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C32Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32B may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C32B.

TABLE I. Mode Selection

Pins	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9–11, 13–17)
Mode				
Read	V_{IL}	V_{IL}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	Hi-Z
Program	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C32B in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C32B may be common. A TTL low level program pulse applied to an NMC27C32B's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that NMC27C32B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C32B from being programmed.

Program Verify

A verify should be performed on the programmed bit to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C32B has a manufacturer's identification code to aide in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C32B is, "8F01", where "8F" designates that it is made by National Semiconductor, and "01" designates a 32k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A11, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C32B's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C32B is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC27C32B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C32B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (8)	O_7 (17)	O_6 (16)	O_5 (15)	O_4 (14)	O_3 (13)	O_2 (11)	O_1 (10)	O_0 (9)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	0	0	1	01

TABLE III. Minimum NMC27C32B Erasure Time

Light Intensity (μW/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

NMC27C64 65,536-Bit (8k x 8) UV Erasable CMOS PROM

General Description

The NMC27C64 is a high-speed 64k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C64 is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

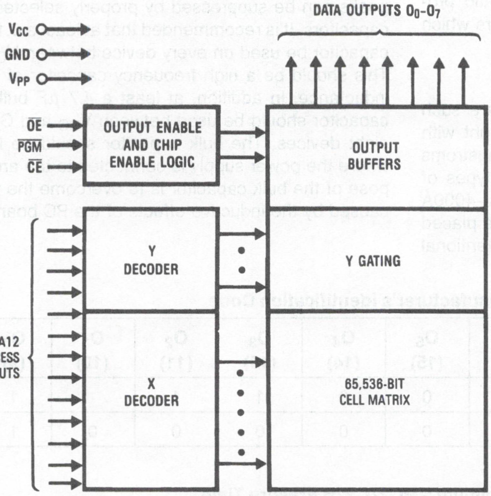
The NMC27C64 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active Power: 55 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C64QE), −40°C to +85°C, and military temperature range (NMC27C64QM), −55°C to +125°C, available
- Pin compatible with NMOS 64k EPROMs
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's identification code for automatic programming control

Block Diagram



TL/D/8634-1

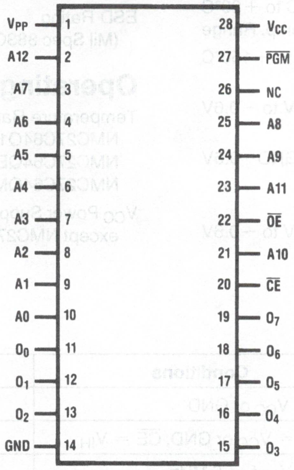
Pin Names

A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C64Q
Dual-In-Line Package


V_{PP} 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O_0 11
O_1 12
O_2 13
GND 14
28 V_{CC}
27 $\overline{\text{PGM}}$
26 NC
25 A8
24 A9
23 A11
22 $\overline{\text{OE}}$
21 A10
20 $\overline{\text{CE}}$
19 O_7
18 O_6
17 O_5
16 O_4
15 O_3

27C16 2716	27C32 2732	27C128 27128	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{\text{PGM}}$	A14	A14
V_{CC}	V_{CC}	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{\text{OE}}$	$\overline{\text{OE}}/V_{PP}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{\text{CE/PGM}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$/PGM	$\overline{\text{CE}}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

TL/D/8634-2

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64 pins.

Order Number NMC27C64Q
See NS Package Number J28AQ

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C64Q15	150

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64Q150	150
NMC27C64Q200	200
NMC27C64Q250	250
NMC27C64Q300	300

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QE150	150
NMC27C64QE200	200

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QM200	200
NMC27C64QM250	250

NOTE: For plastic DIP requirements please refer to NMC27C64N data sheet.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias Commercial Military and Extended	 −10°C to +80°C Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C64Q15, Q150, 200, 250	0°C to +70°C
NMC27C64QE150, 200	−40°C to +85°C
NMC27C64QM200, M250	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%
except NMC27C64Q15	+5V ±5%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64Q						Units
			15, 150, E150		200, E200, M200		250, M250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		60		70	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

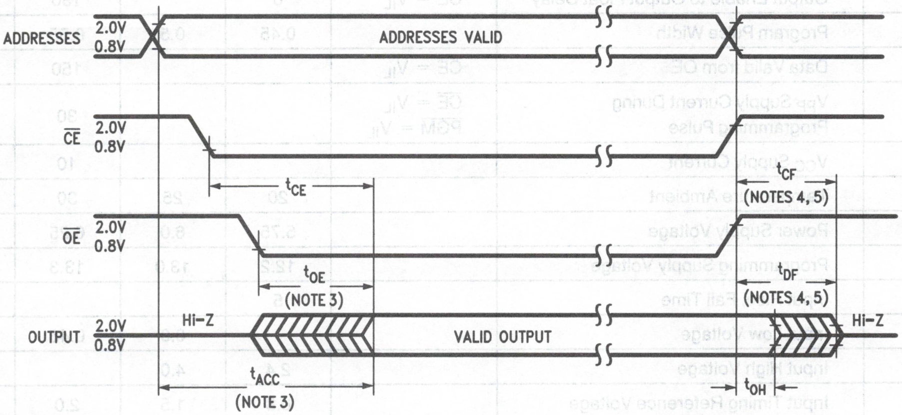
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6 & 9)



TL/D/8634-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

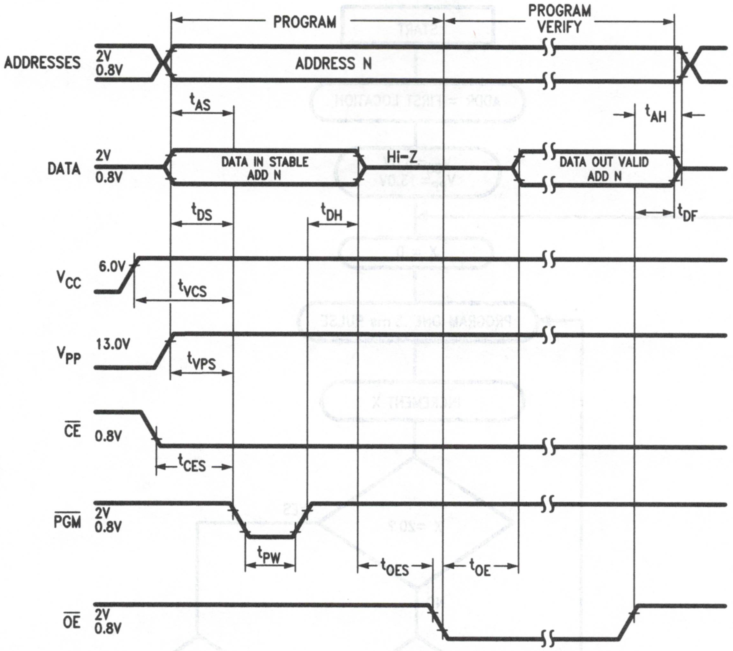
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)


PROGRAM
PROGRAM VERIFY
ADDRESSES
2V
0.8V
ADDRESS N
t_{AS}
t_{AH}
DATA
2V
0.8V
DATA IN STABLE ADD N
Hi-Z
DATA OUT VALID ADD N
t_{DS}
t_{DH}
t_{DF}
V_{CC}
6.0V
t_{VCS}
V_{PP}
13.0V
t_{VPS}
$\overline{CE}$
0.8V
t_{CES}
$\overline{PGM}$
2V
0.8V
t_{PW}
t_{OES}
t_{OE}
$\overline{OE}$
2V
0.8V

TL/D/8634-6

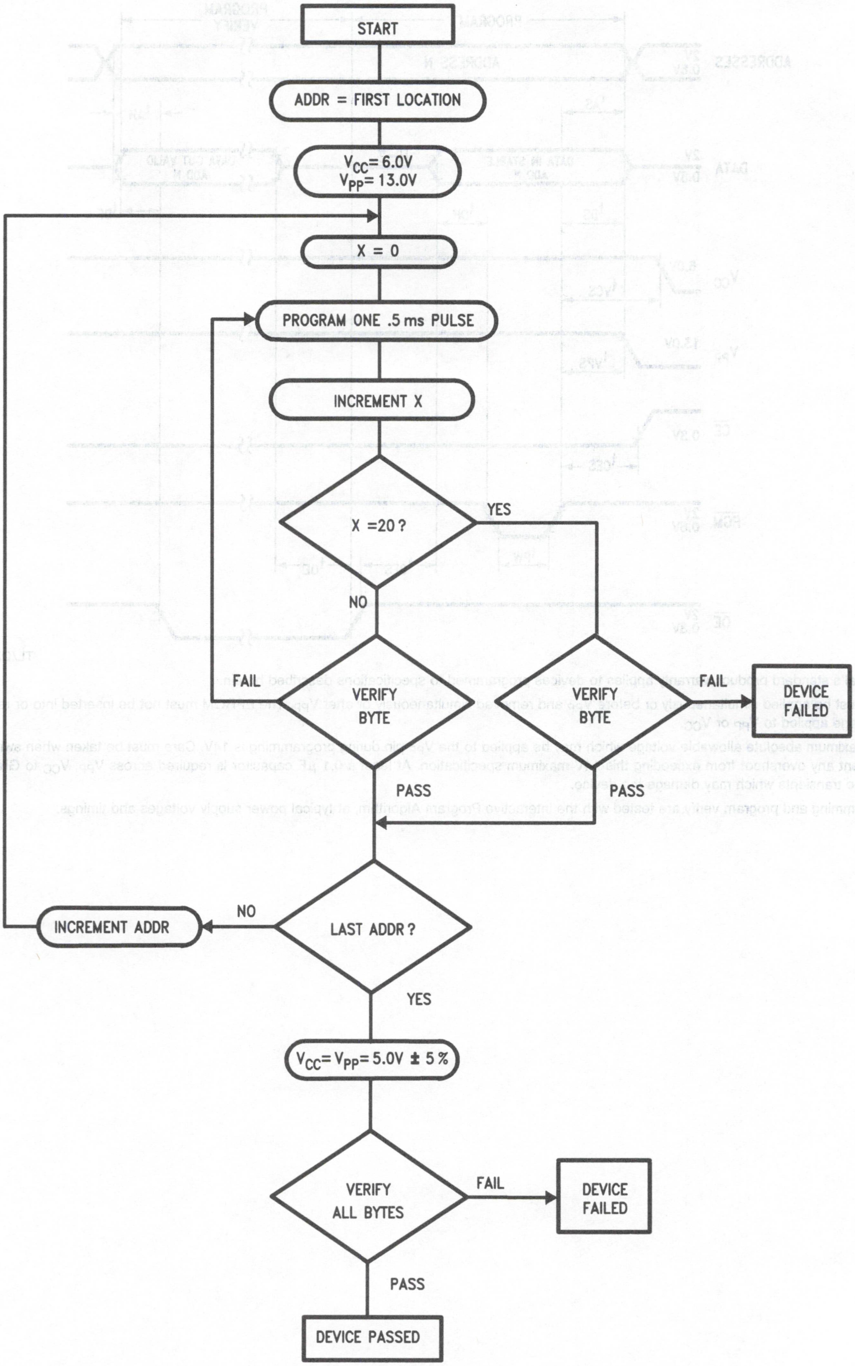
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the interactive Program Algorithm, at typical power supply voltages and timings.

Interactive Programming Algorithm Flow Chart


START
ADDR = FIRST LOCATION
V_{CC}= 6.0V
V_{PP}= 13.0V
X = 0
PROGRAM ONE .5 ms PULSE
INCREMENT X
X =20 ?
YES
NO
FAIL
VERIFY BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC}= V_{PP}= 5.0V ± 5 %
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

TL/D/8634–5

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C64 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C64 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C64 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C64s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C64.

Initially, all bits of the NMC27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. A "0" cannot be changed to a "1" once the bit has been programmed.

The NMC27C64 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 13.0V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C64 is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The NMC27C64 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C64s.

TABLE I. Mode Selection

Pins Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}		13V	6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	13V	6V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	13V	6V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C64s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C64 may be common. A TTL low level program pulse applied to an NMC27C64's PGM input with $\overline{CE}$ at V_{IL} and V_{PP} at 13.0V will program that NMC27C64. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C64 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64 is "8FC2", where "8F" designates that it is made by National Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C64 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming, opaque labels should be placed over the NMC27C64's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C64 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C64 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C64 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2

TABLE III. Minimum NMC27C64 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

NMC27C64N 65,536-Bit (8k x 8) One-Time Programmable CMOS PROM

General Description

The NMC27C64N is a high-speed 64k one-time programmable CMOS PROM. It is ideally suited for high volume production applications where low cost, fast turnaround, and low power consumption are important factors and reprogramming is not required.

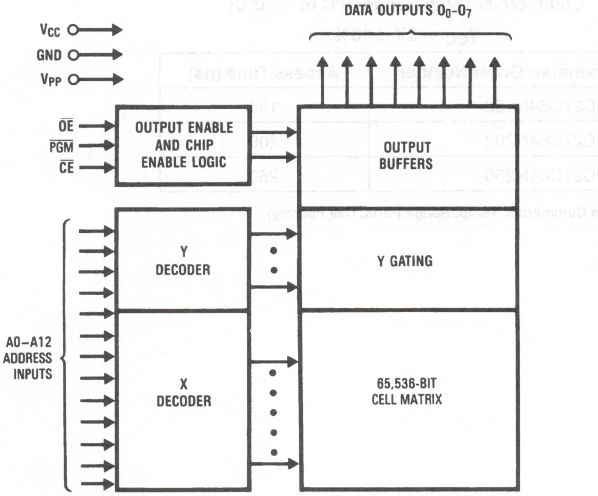
The NMC27C64N is designed to operate with a single +5V power supply with ±10% tolerance. The NMC27C64N is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be done once. Also the plastic molded package works well in auto insertion equipment used in automated assembly lines.

This device is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns, CMOS technology
- Low CMOS power consumption
  - — Active Power: 55 mW max
  - — Standby Power: 0.55 mW max
- Pin compatible with all 64k EPROMs
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum PROM for total CMOS systems
- Manufacture's identification code for automatic programming control

Block Diagram


DATA OUTPUTS O_0-O_7
V_{CC}
GND
V_{PP}
$\overline{OE}$
$\overline{PGM}$
$\overline{CE}$
OUTPUT ENABLE AND CHIP ENABLE LOGIC
OUTPUT BUFFERS
Y DECODER
Y GATING
A0–A12 ADDRESS INPUTS
X DECODER
65,536-BIT CELL MATRIX

TL/D/9686-1

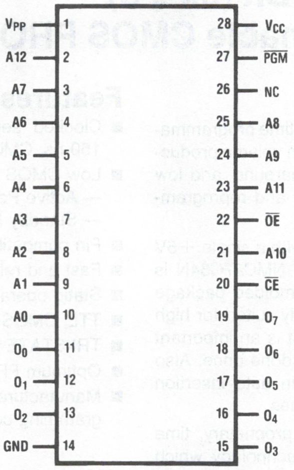
Pin Names

A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C32 2732	27C16 2716	NMC27C64N	Pin
A15	V_{PP}	V_{PP}			V_{PP}	1
A12	A12	A12			A12	2
A7	A7	A7	A7	A7	A7	3
A6	A6	A6	A6	A6	A6	4
A5	A5	A5	A5	A5	A5	5
A4	A4	A4	A4	A4	A4	6
A3	A3	A3	A3	A3	A3	7
A2	A2	A2	A2	A2	A2	8
A1	A1	A1	A1	A1	A1	9
A0	A0	A0	A0	A0	A0	10
O_0	O_0	O_0	O_0	O_0	O_0	11
O_1	O_1	O_1	O_1	O_1	O_1	12
O_2	O_2	O_2	O_2	O_2	O_2	13
GND	GND	GND	GND	GND	GND	14

NMC27C64N
Dual-In-Line Package



V_{PP} 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O_0 11
O_1 12
O_2 13
GND 14
28 V_{CC}
27 $\overline{PGM}$
26 NC
25 A8
24 A9
23 A11
22 $\overline{OE}$
21 A10
20 $\overline{CE}$
19 O_7
18 O_6
17 O_5
16 O_4
15 O_3

Pin	NMC27C64N	27C16 2716	27C32 2732	27C128 27128	27C256 27256	27C512 27512
28	V_{CC}			V_{CC}	V_{CC}	V_{CC}
27	$\overline{PGM}$			$\overline{PGM}$	A14	A14
26	NC	V_{CC}	V_{CC}	A13	A13	A13
25	A8	A8	A8	A8	A8	A8
24	A9	A9	A9	A9	A9	A9
23	A11	V_{PP}	A11	A11	A11	A11
22	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
21	A10	A10	A10	A10	A10	A10
20	$\overline{CE}$	$\overline{CE}$/PGM	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$/PGM	$\overline{CE}$
19	O_7	O_7	O_7	O_7	O_7	O_7
18	O_6	O_6	O_6	O_6	O_6	O_6
17	O_5	O_5	O_5	O_5	O_5	O_5
16	O_4	O_4	O_4	O_4	O_4	O_4
15	O_3	O_3	O_3	O_3	O_3	O_3

TL/D/9686-2

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64N pins.

Order Number NMC27C64N
See NS Package Number N28B

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64N150	150
NMC27C64N200	200
NMC27C64N250	250

(For Non Commercial Temp. Range Parts, Call Factory)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply NMC27C64N150, 200, 250	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		6	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 mA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	$V_{CC} - 0.1$			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64N						Units
			150		200		250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		60		70	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	10	pF

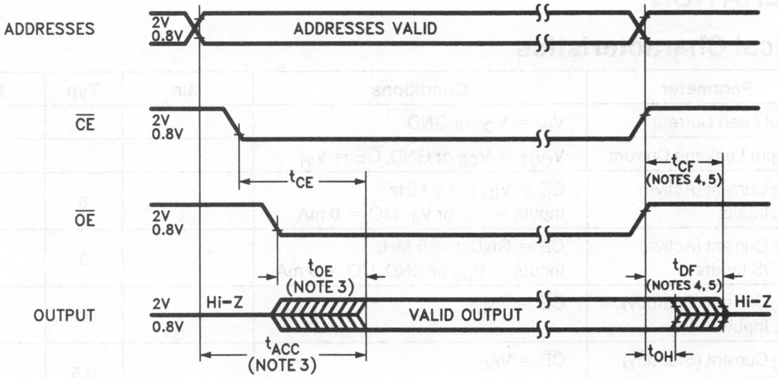
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



TL/D/9686-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ µA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to $-0.2V$ for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

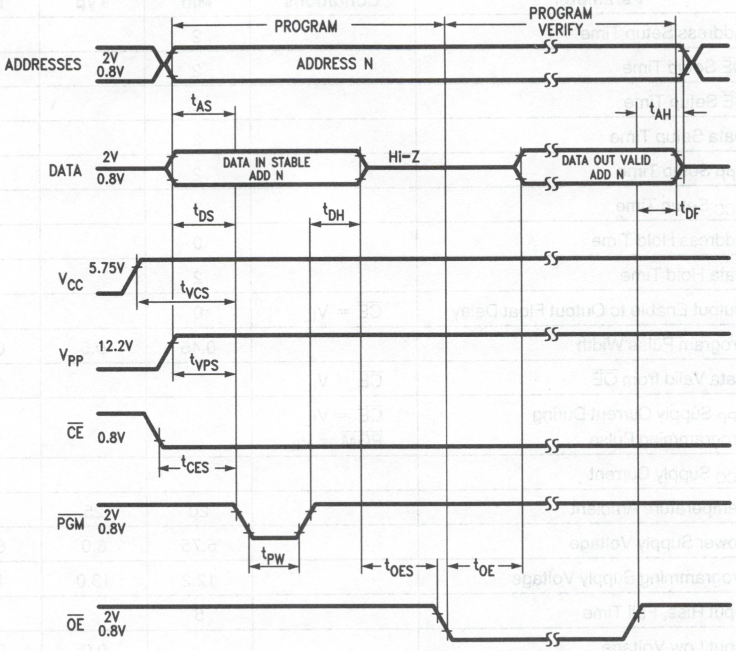
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Interactive Program Algorithm, at typical power supply voltages and timings.

Programming Waveforms (Note 3)


PROGRAM
PROGRAM VERIFY
ADDRESSES
2V
0.8V
ADDRESS N
t_{AS}
t_{AH}
DATA
2V
0.8V
DATA IN STABLE ADD N
Hi-Z
DATA OUT VALID ADD N
t_{DS}
t_{DH}
t_{DF}
V_{CC}
5.75V
t_{VCS}
V_{PP}
12.2V
t_{VPS}
$\overline{CE}$
0.8V
t_{CES}
$\overline{PGM}$
2V
0.8V
t_{PW}
t_{OES}
t_{OE}
$\overline{OE}$
2V
0.8V

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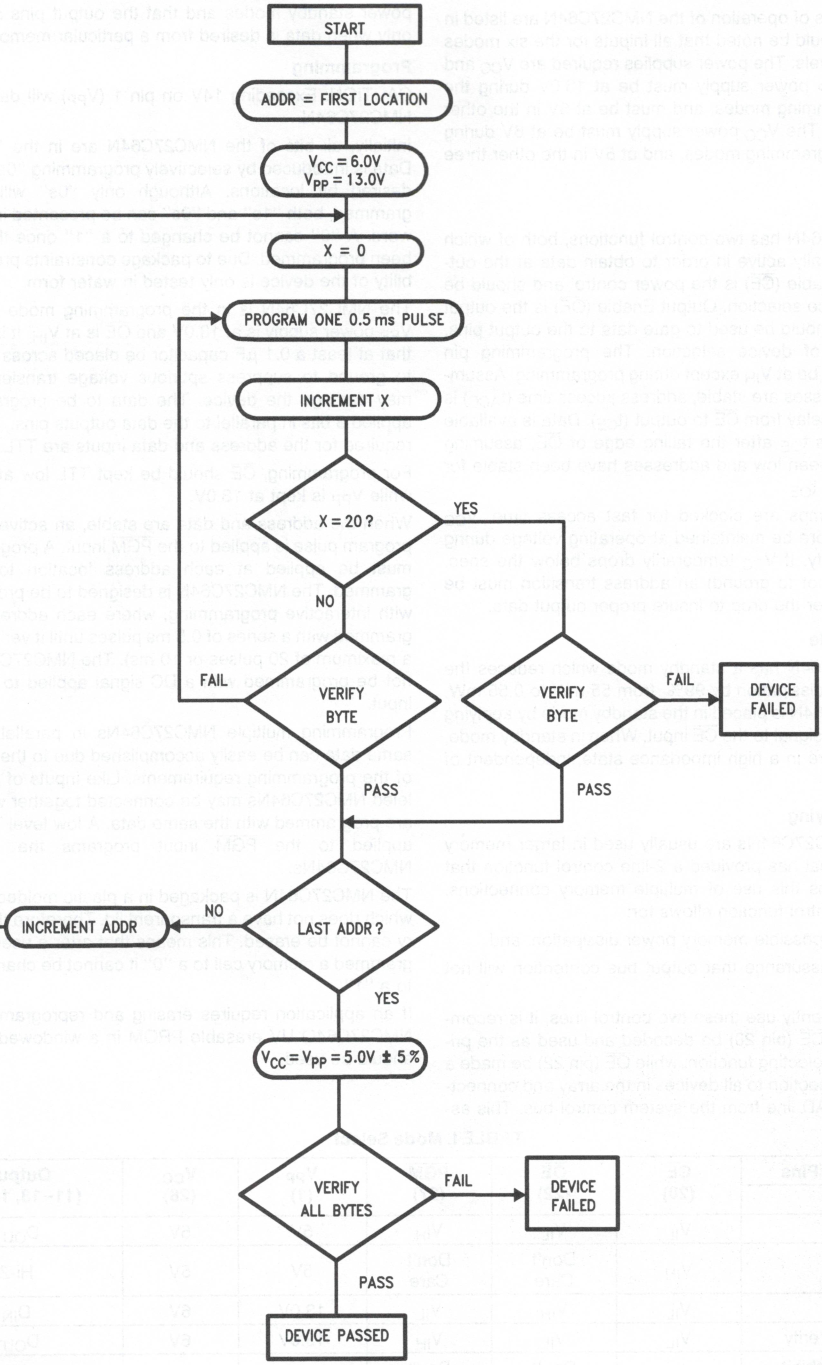
Interactive Programming Algorithm Flow Chart


START
ADDR = FIRST LOCATION
$V_{CC} = 6.0V$
$V_{PP} = 13.0V$
X = 0
PROGRAM ONE 0.5 ms PULSE
INCREMENT X
X = 20 ?
YES
NO
VERIFY BYTE
FAIL
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
LAST ADDR ?
NO
INCREMENT ADDR
YES
$V_{CC} = V_{PP} = 5.0V \pm 5\%$
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

TL/D/9686–5

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C64N are listed in Table I. It should be noted that all iniputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C64N has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{\text{PGM}}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C64N has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C64N is placed in the standby mode by applying a CMOS high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Output OR-Tying

Because NMC27C64Ns are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{\text{CE}}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{\text{OE}}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C64N.

Initially, all bits of the NMC27C64N are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. A "0" cannot be changed to a "1" once the bit has been programmed. Due to package constraints programmability of the device is only tested in wafer form.

The NMC27C64N is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{\text{OE}}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data outputs pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{\text{CE}}$ should be kept TTL low at all times while V_{PP} is kept at 13.0V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{\text{PGM}}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C64N is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The NMC27C64N must not be programmed with a DC signal applied to the $\overline{\text{PGM}}$ input.

Programming multiple NMC27C64Ns in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64Ns may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{\text{PGM}}$ input programs the paralleled NMC27C64Ns.

The NMC27C64N is packaged in a plastic molded package which does not have a transparent lid. Therefore the memory cannot be erased. This means that after a user has programmed a memory cell to a "0" it cannot be changed back to a "1".

If an application requires erasing and reprogramming, the NMC27C64Q UV erasable PROM in a windowed package should be used.

TABLE I. Mode Select

Pins / Mode	$\overline{\text{CE}}$ (20)	$\overline{\text{OE}}$ (22)	$\overline{\text{PGM}}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	13.0V	6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	13.0V	6V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	13.0V	6V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C64Ns in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C64N may be common. A TTL low level program pulse applied to an NMC27C64Ns $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 13.0V will program that NMC27C64N. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64Ns from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S INDENTIFICATION CODE

The NMC27C64N has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64N is "8FC2", where "8F" designates that it is made by National Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$ and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

SYSTEM CONSIDERATION

The power switching characteristics of this device require careful decoupling. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2

National Semiconductor

PRELIMINARY

NMC27C128B High Speed Version 131,072-Bit (16k x 8) UV Erasable CMOS PROM

General Description

The NMC27C128B is a high-speed 128k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C128B is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

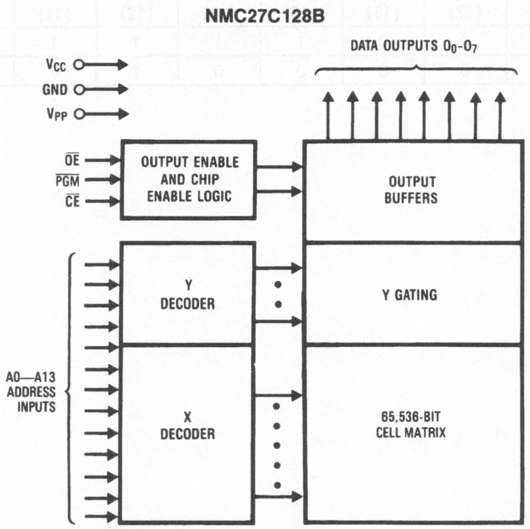
The NMC27C128B is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clock sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active Power: 110 mW max
  - — Standby Power: 0.55 mW max
- Extended temperature range (NMC27C128BQE), −40°C to +85°C, and military temperature range (NMC27C128BQM), −55°C to +125°C available
- Pin compatible with NMOS 128k EPROMs
- Fast and reliable programming—100 μs typical/byte
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



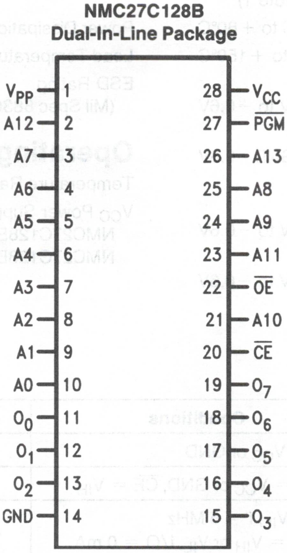
TL/D/9689–1

Pin Names

A0–A13	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagrams

27C512	27C256	27C64	27C32	27C16	NMC27C128B Dual-In-Line Package		27C16	27C32	27C64	27C256	27C512
27512	27256	2764	2732	2716			2716	2732	2764	27256	27512
A15	V_{PP}	V_{PP}			V_{PP} — 1	28 — V_{CC}			V_{CC}	V_{CC}	V_{CC}
A12	A12	A12			A12 — 2	27 — $\overline{\text{PGM}}$			$\overline{\text{PGM}}$	A14	A14
A7	A7	A7	A7	A7	A7 — 3	26 — A13	V_{CC}	V_{CC}	NC	A13	A13
A6	A6	A6	A6	A6	A6 — 4	25 — A8	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	A5 — 5	24 — A9	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	A4 — 6	23 — A11	V_{PP}	A11	A11	A11	A11
A3	A3	A3	A3	A3	A3 — 7	22 — $\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}/V_{PP}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}/V_{PP}$
A2	A2	A2	A2	A2	A2 — 8	21 — A10	A10	A10	A10	A10	A10
A1	A1	A1	A1	A1	A1 — 9	20 — $\overline{\text{CE}}$	CE/$\overline{\text{PGM}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}/\text{PGM}$	$\overline{\text{CE}}$
A0	A0	A0	A0	A0	A0 — 10	19 — O_7	O_7	O_7	O_7	O_7	O_7
O_0	O_0	O_0	O_0	O_0	O_0 — 11	18 — O_6	O_6	O_6	O_6	O_6	O_6
O_1	O_1	O_1	O_1	O_1	O_1 — 12	17 — O_5	O_5	O_5	O_5	O_5	O_5
O_2	O_2	O_2	O_2	O_2	O_2 — 13	16 — O_4	O_4	O_4	O_4	O_4	O_4
GND	GND	GND	GND	GND	GND — 14	15 — O_3	O_3	O_3	O_3	O_3	O_3



TL/D/9689–2

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C128B pins.

Order Number NMC27C128BQ
See NS Package Number J28AQ

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C128BQ150	150
NMC27C128BQ200	200
NMC27C128BQ250	250

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C128BQ15	150
NMC27C128BQ20	200
NMC27C128BQ25	250

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C128BQE150	150
NMC27C128BQE200	200

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C128BQM150	150
NMC27C128BQM200	200

NOTE: For plastic DIP and surface mount PLCC package requirements please refer to NMC27C128BN datasheet.

800-272-9959

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COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V

Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	
NMC27C128BQ150, 200, 250	+5V ±10%
NMC27C128BQ15, 20, 25	±5V ±5%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		10	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		8	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	µA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 µA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C128B						Units
			Q15, Q150		Q20, Q200		Q25, Q250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC}+1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C128BQE150, 200	−40°C to +85°C
NMC27C128BQM150, 200	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = V_{CC} or GND			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND, $\overline{CE}$ = V_{IH}			10	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE}$ = V_{IL}, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		10	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		8	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE}$ = V_{IH}		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE}$ = V_{CC}		0.5	100	µA
I_{PP}	V_{PP} Load Current	V_{PP} = V_{CC}			10	µA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 µA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C128BQ				Units
			E150, M150		E200, M200		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{PGM}$ = V_{IH}		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}		60		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	50	0	55	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	50	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{PGM}$ = V_{IH}	0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

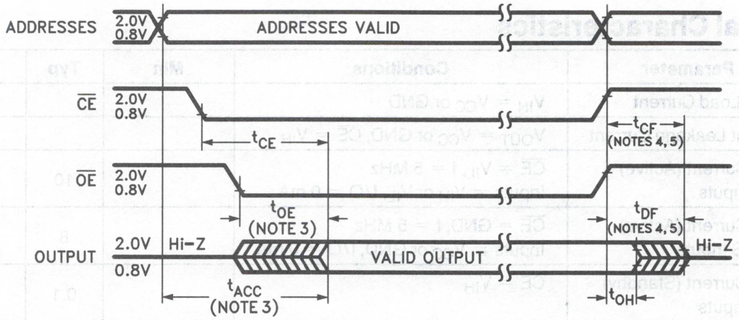
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) $-0.10V$;

Low to TRI-STATE, the measured V_{OL1} (DC) $+0.10V$.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC} + 1.0V$ to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.

C_L: 100 pF includes fixture capacitance.

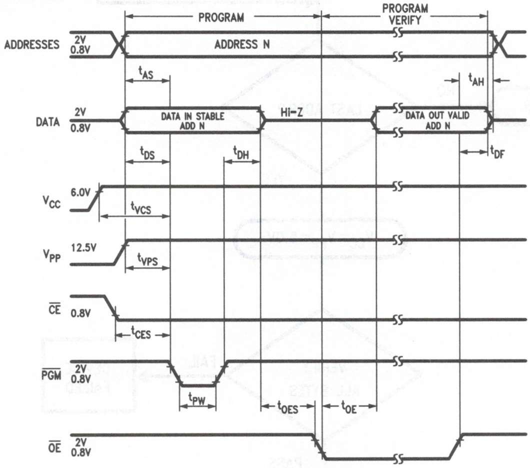
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to $-2.0V$ for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)


PROGRAM
PROGRAM VERIFY
ADDRESSES
2V
0.8V
ADDRESS N
t_{AS}
t_{AH}
DATA
2V
0.8V
DATA IN STABLE ADD N
Hi-Z
DATA OUT VALID ADD N
t_{DS}
t_{DH}
t_{DF}
V_{CC}
6.0V
t_{VCS}
V_{PP}
12.5V
t_{VPS}
$\overline{CE}$
0.8V
t_{CES}
$\overline{PGM}$
2V
0.8V
t_{PW}
t_{OES}
t_{OE}
$\overline{OE}$
2V
0.8V

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Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart (Note 4)

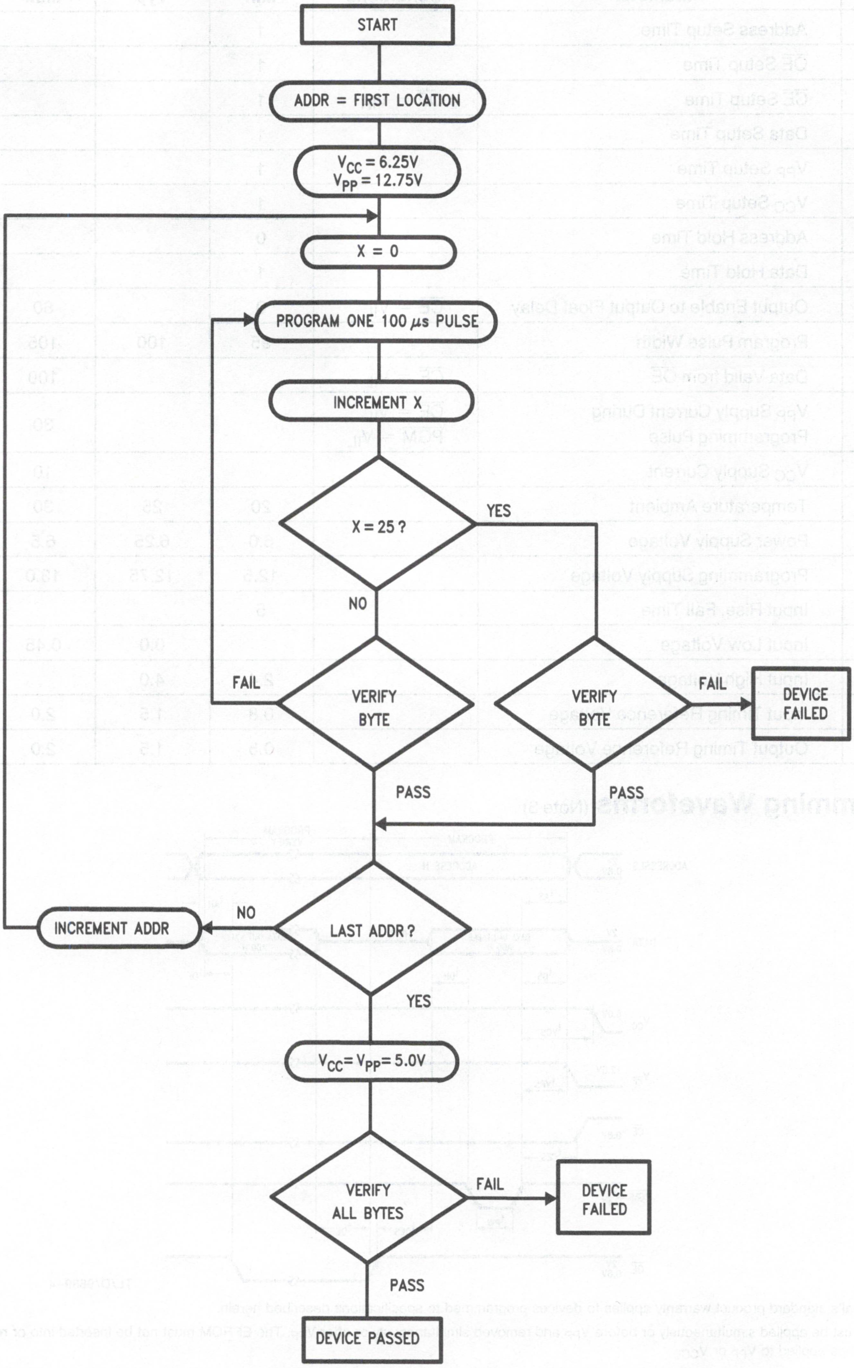
START
ADDR = FIRST LOCATION
V_{CC} = 6.25V
V_{PP} = 12.75V
X = 0
PROGRAM ONE 100 µs PULSE
INCREMENT X
X = 25 ?
YES
NO
FAIL
VERIFY BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC} = V_{PP} = 5.0V
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

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FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)

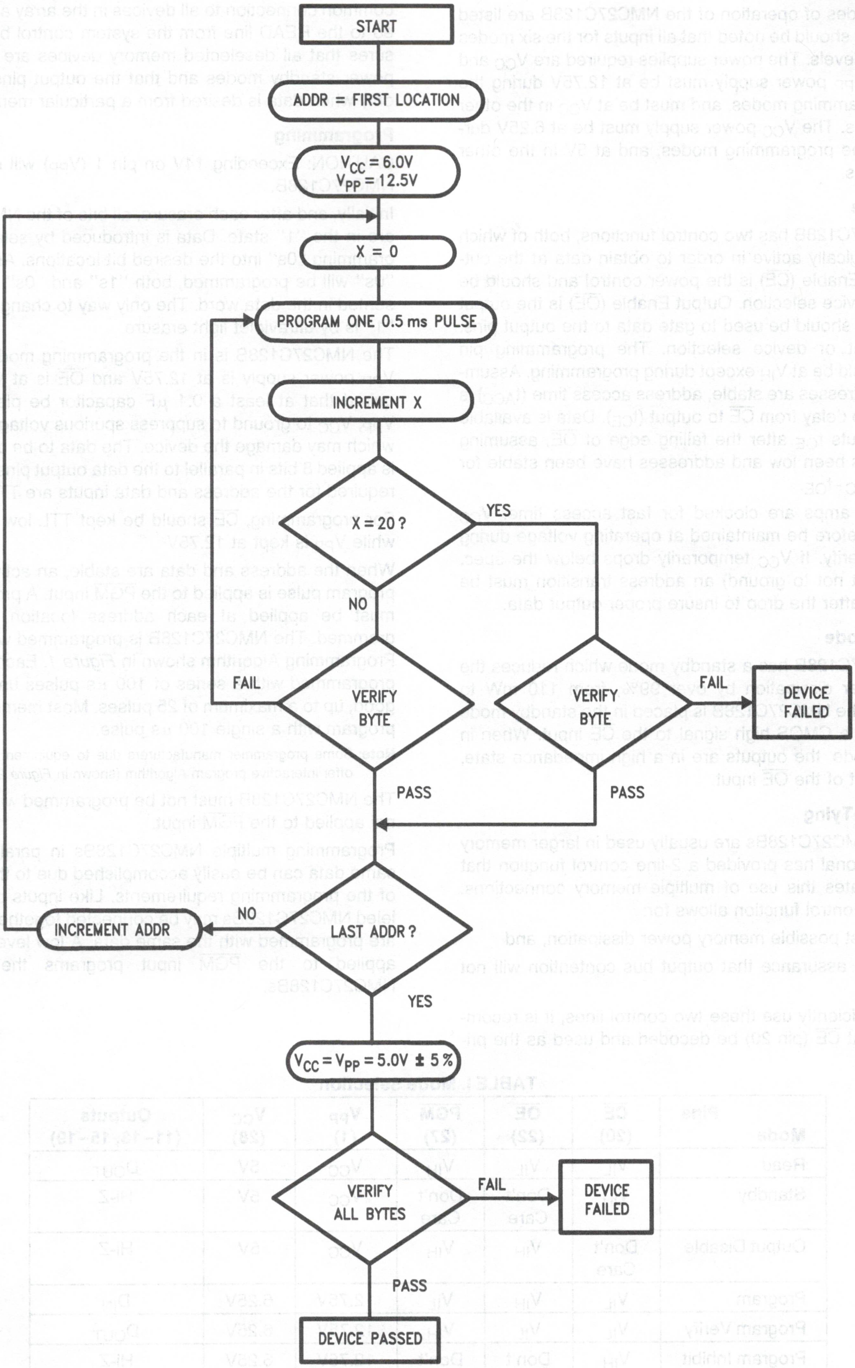
START
ADDR = FIRST LOCATION
$V_{CC} = 6.0V$
$V_{PP} = 12.5V$
X = 0
PROGRAM ONE 0.5 ms PULSE
INCREMENT X
X = 20 ?
YES
NO
FAIL
VERIFY BYTE
FAIL
VERIFY BYTE
DEVICE FAILED
PASS
PASS
INCREMENT ADDR
NO
LAST ADDR ?
YES
$V_{CC} = V_{PP} = 5.0V \pm 5\%$
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C128B are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at V_{CC} in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C128B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C128B has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C128B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C128Bs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C128B.

Initially, and after each erasure, all bits of the NMC27C128B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C128B is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 12.75V

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C128B is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

Note: Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (shown in *Figure 2*).

The NMC27C128B must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C128Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C128Bs may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C128Bs.

TABLE I. Mode Selection

Pins Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	V_{CC}	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C128s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C128Bs may be common. A TTL low level program pulse applied to an NMC27C128B's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that NMC27C128B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C128Bs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C128B has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C128B is "8F83", where "8F" designates that it is made by National Semiconductor, and "83" designates a 128k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A13, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C128B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming opaque labels should be placed over the NMC27C128B's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C128B is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C128B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C128B erasure time for various light intensities.

An erasure system should be cailbrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of this device require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	0	1	1	83

TABLE III. Minimum NMC27C128B Erasure Time

Light Intensity (μW/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C128BN High Speed Version 131,072-Bit (16k x 8) One Time Programmable CMOS PROM

General Description

The NMC27C128BN is a high-speed 128k one time programmable CMOS PROM, ideally suited for applications where fast turnaround and low power consumption are important requirements.

The NMC27C128BN is designed to operate with a single +5V power supply with ±5% or ±10% tolerance.

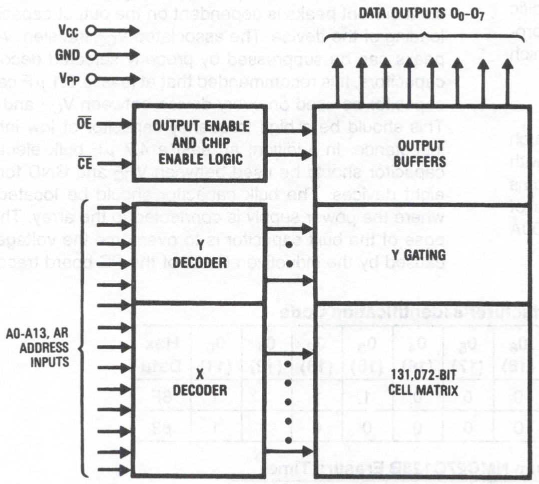
The NMC27C128BN is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be done once. Also the plastic molded package works well in auto insertion equipment used in automated assembly lines.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active Power: 11.0 mW max
  - — Standby Power: 0.55 mW max
- Optimum EPROM for total CMOS systems
- Pin compatible with NMOS 128k EPROMs
- Fast and reliable programming—100 μs typical/byte
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram


DATA OUTPUTS O_0–O_7
V_{CC}
GND
V_{PP}
$\overline{OE}$
$\overline{CE}$
OUTPUT ENABLE AND CHIP ENABLE LOGIC
OUTPUT BUFFERS
Y DECODER
Y GATING
A0-A13, AR ADDRESS INPUTS
X DECODER
131,072-BIT CELL MATRIX

TL/D/9690–1

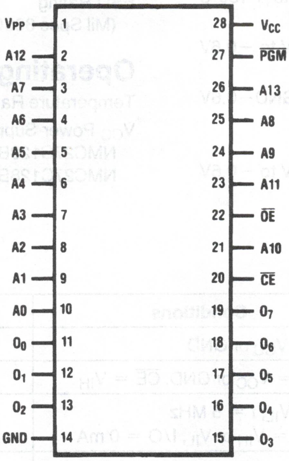
Pin Names

A0–A13	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program

Connection Diagram

27C512 27512	27C256 27256	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

Dual-In-Line Package



V_{PP} 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O_0 11
O_1 12
O_2 13
GND 14
28 V_{CC}
27 $\overline{PGM}$
26 A13
25 A8
24 A9
23 A11
22 $\overline{OE}$
21 A10
20 $\overline{CE}$
19 O_7
18 O_6
17 O_5
16 O_4
15 O_3

27C16 2716	27C32 2732	27C64 2764	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/PGM$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/PGM$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

TL/D/9690-2

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C128BN pins.

Order Number NMC27C128BN
See NS Package Number N28B

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C128BN15	150
NMC27C128BN20	200
NMC27C128BN25	250

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C128BN150	150
NMC27C128BN200	200
NMC27C128BN250	250

For non-commercial temperature range parts, call the factory.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC}+1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −6.0V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	
NMC27C128BN150, 200, 250	+5V ±10%
NMC27C128BN15, 20, 25	+5V ±5%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		10	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		8	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C128B						Units
			N15, N150		N20, N200		N25, N250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

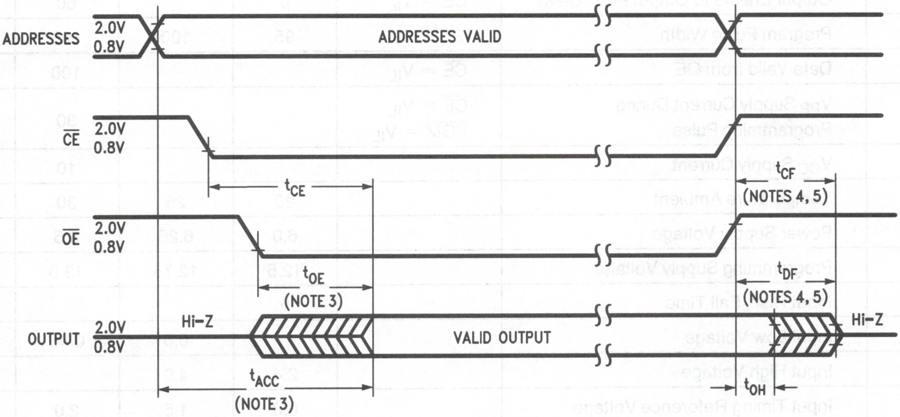
Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	10	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

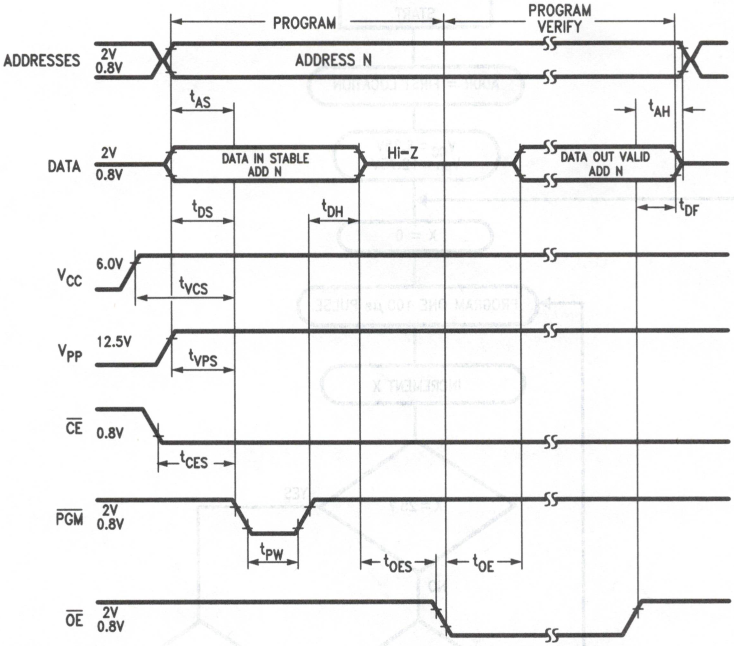
Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns max.

1

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{\text{OE}}$ Setup Time		1			µs
t_{CES}	$\overline{\text{CE}}$ Setup Time	$\overline{\text{OE}} = V_{IH}$	1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{\text{CE}} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{\text{OE}}$	$\overline{\text{CE}} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{\text{CE}} = V_{IL}$ $\overline{\text{PGM}} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)


PROGRAM
PROGRAM VERIFY
ADDRESSES
2V
0.8V
ADDRESS N
t_{AS}
t_{AH}
DATA
2V
0.8V
DATA IN STABLE ADD N
Hi-Z
DATA OUT VALID ADD N
t_{DS}
t_{DH}
t_{DF}
V_{CC}
6.0V
t_{VCS}
V_{PP}
12.5V
t_{VPS}
$\overline{CE}$
0.8V
t_{CES}
$\overline{PGM}$
2V
0.8V
t_{PW}
t_{OES}
t_{OE}
$\overline{OE}$
2V
0.8V

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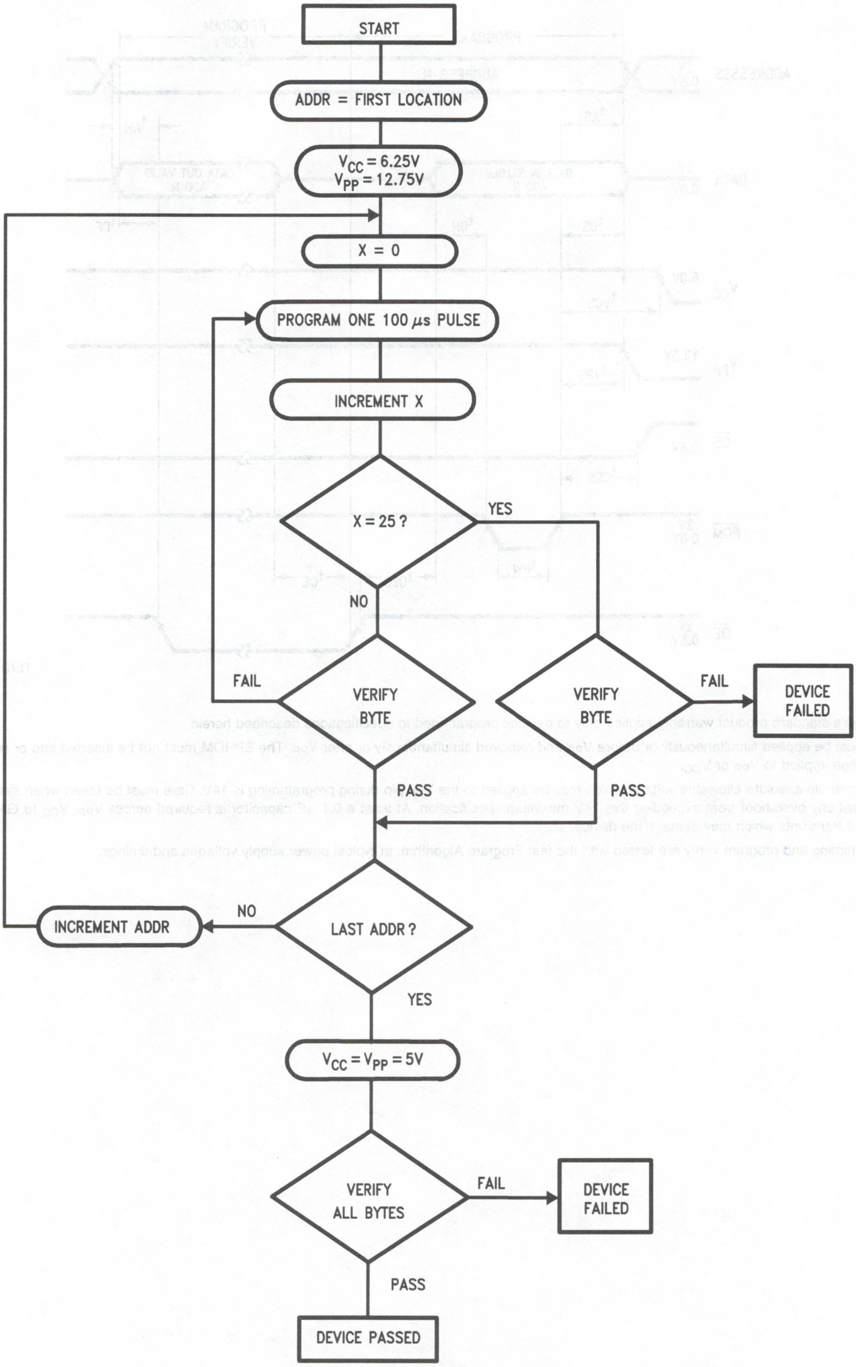
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

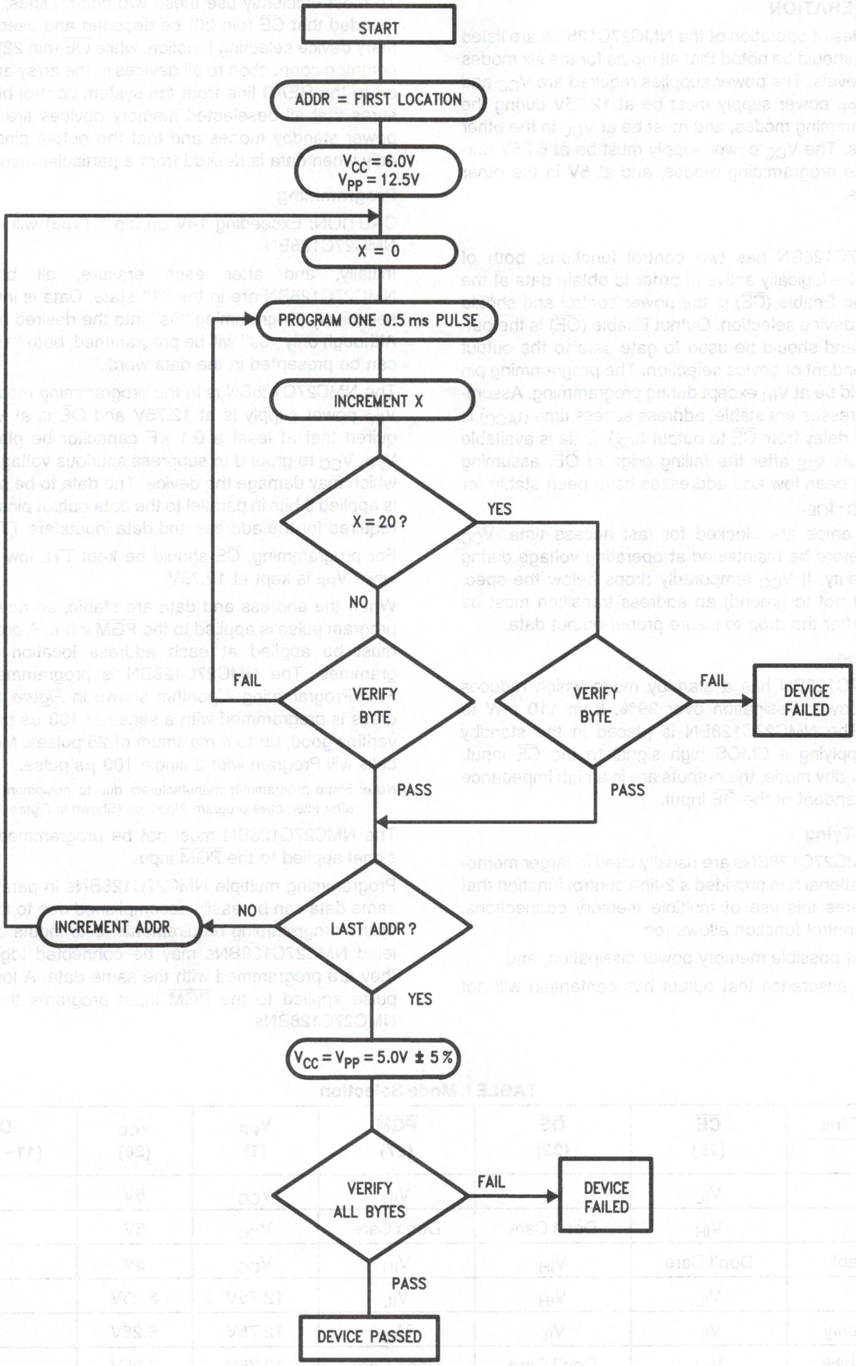
Fast Programming Algorithm Flow Chart (Note 4)


START
ADDR = FIRST LOCATION
V_{CC} = 6.25V
V_{PP} = 12.75V
X = 0
PROGRAM ONE 100 μs PULSE
INCREMENT X
X = 25 ?
YES
NO
FAIL
VERIFY BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC} = V_{PP} = 5V
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

TL/D/9690–5

FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)


START
ADDR = FIRST LOCATION
V_{CC} = 6.0V
V_{PP} = 12.5V
X = 0
PROGRAM ONE 0.5 ms PULSE
INCREMENT X
X = 20 ?
YES
NO
FAIL
VERIFY BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC} = V_{PP} = 5.0V ± 5%
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

TL/D/9690–6

FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C128BN are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at V_{CC} in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C128BN has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{\text{PGM}}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C128BN has a standby mode which reduces the active power dissipation over 99%, from 110 mW to 0.55 mW. The NMC27C128BN is placed in the standby mode by applying a CMOS high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Output OR-Tying

Because NMC27C128BNs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{\text{CE}}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{\text{OE}}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C128BN.

Initially, and after each erasure, all bits of the NMC27C128BN are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word.

The NMC27C128BN is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{\text{OE}}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{\text{CE}}$ should be kept TTL low at all times while V_{PP} is kept at 12.75V.

When the address and data are stable, an active low TTL program pulse is applied to the $\overline{\text{PGM}}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C128BN is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will Program with a single 100 μs pulse.

Note: Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (Shown in *Figure 2*).

The NMC27C128BN must not be programmed with a DC signal applied to the $\overline{\text{PGM}}$ input.

Programming multiple NMC27C128BNs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C128BNs may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{\text{PGM}}$ input programs the paralleled NMC27C128BNs.

TABLE I. Mode Selection

Pins Mode	$\overline{\text{CE}}$ (20)	$\overline{\text{OE}}$ (22)	$\overline{\text{PGM}}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	V_{CC}	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

Functional Description (Continued)

The NMC27C128BN is packaged in a plastic molded package which does not have a transparent lid. Therefore the memory cannot be erased. This means that after a user has programmed a memory cell to a "0" it cannot be changed back to a "1".

If an application requires erasing and reprogramming, the NMC27C128BQ UV Erasable PROM in a windowed package should be used.

Program Inhibit

Programming multiple NMC27C128BNs in parallel with different data is also easily accomplished. Except for $\overline{\text{CE}}$ all like inputs (including $\overline{\text{OE}}$ and $\overline{\text{PGM}}$) of the parallel NMC27C128BNs may be common. A TTL low level program pulse applied to an NMC27C128BNs $\overline{\text{PGM}}$ input with $\overline{\text{CE}}$ at V_{IL} and V_{PP} at 12.75V will program that NMC27C128BN. A TTL high level $\overline{\text{CE}}$ input inhibits the other NMC27C128BNs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V (V_{PP} must be at V_{CC}) except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C128BN has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C128BN is "8F83", where "8F" designates that it is made by National Semiconductor, and "83" designates a 128k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A13, $\overline{\text{CE}}$, and $\overline{\text{OE}}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

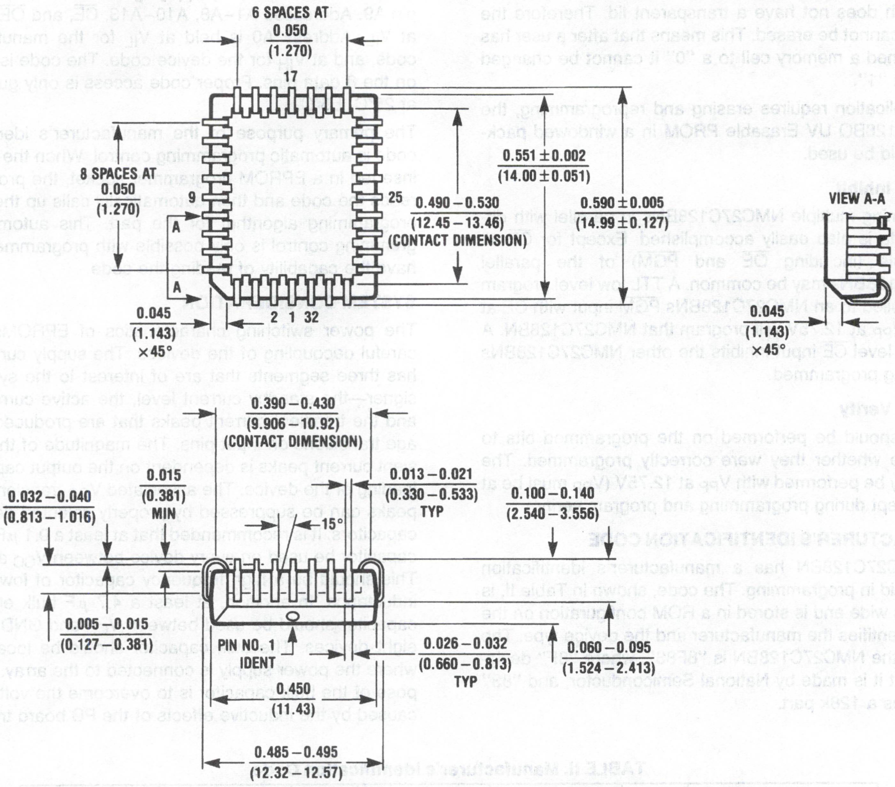
SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	0	1	1	83

Package Information


6 SPACES AT
0.050
(1.270)
17
8 SPACES AT
0.050
(1.270)
9
25
A
A
0.490 – 0.530
(12.45 – 13.46)
(CONTACT DIMENSION)
0.551 ± 0.002
(14.00 ± 0.051)
0.590 ± 0.005
(14.99 ± 0.127)
VIEW A-A
0.045
(1.143)
×45°
2 1 32
0.045
(1.143)
×45°
0.390 – 0.430
(9.906 – 10.92)
(CONTACT DIMENSION)
0.015
(0.381)
MIN
0.013 – 0.021
(0.330 – 0.533)
TYP
0.032 – 0.040
(0.813 – 1.016)
0.100 – 0.140
(2.540 – 3.556)
15°
0.005 – 0.015
(0.127 – 0.381)
PIN NO. 1
IDENT
0.026 – 0.032
(0.660 – 0.813)
TYP
0.060 – 0.095
(1.524 – 2.413)
0.450
(11.43)
0.485 – 0.495
(12.32 – 12.57)

TL/D/9690-7

32-Lead PLCC Package
Order Number NMC27C128BV

National Semiconductor

NMC27C256
262,144-Bit (32k x 8) UV Erasable CMOS PROM

General Description

The NMC27C256 is a high-speed 256k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C256 is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

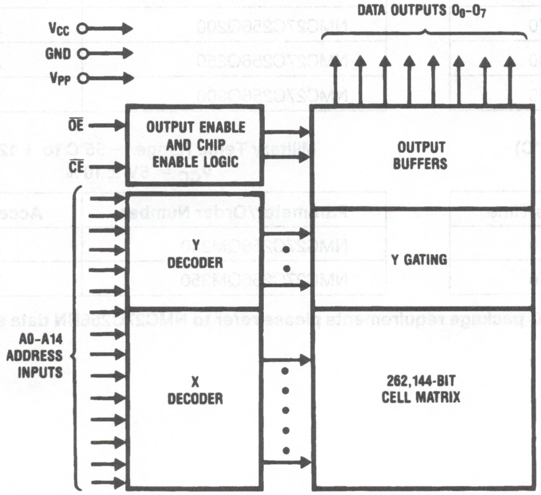
The NMC27C256 is packaged in a 28-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 170 ns
- Low CMOS power consumption
  - — Active power: 55 mW max
  - — Standby power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C256QE), −40°C to +85°C, and military temperature range (NMC27C256QM), −55°C to +125°C, available
- Pin compatible with NMOS 256k EPROMs
- Fast and reliable programming (0.5 ms for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems

Block Diagram



TL/D/7512-1

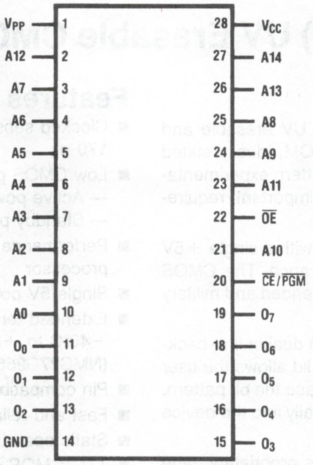
Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C128 27128	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C256Q
Dual-In-Line Package



27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/PGM$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

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Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C256 pins.

Order Number NMC27C256Q
See NS Package Number J28AQ

Commercial Temp Range (0°C to +70°C)
$V_{CC} = 5V \pm 5\%$

Parameter/Order Number	Access Time
NMC27C256Q17	170
NMC27C256Q20	200
NMC27C256Q25	250

Commercial Temp Range (0°C to +70°C)
$V_{CC} = 5V \pm 10\%$

Parameter/Order Number	Access Time
NMC27C256Q200	200
NMC27C256Q250	250
NMC27C256Q300	300

Extended Temp Range (−40°C to +85°C)
$V_{CC} = 5V \pm 10\%$

Parameter/Order Number	Access Time
NMC27C256QE200	200
NMC27C256QE250	250

Military Temp Range (−55°C to +125°C)
$V_{CC} = 5V \pm 10\%$

Parameter/Order Number	Access Time
NMC27C256QM250	250
NMC27C256QM350	350

NOTE: For plastic DIP and surface mount PLCC package requirements please refer to NMC27C256BN data sheet.

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC}+1.0V to GND−0.6V
V_{PP} Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	
NMC27C256Q17, 20, 25	5V ±5%
NMC27C256Q200, 250, 300	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		6	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	µA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 µA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 µA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256								Units
			Q17		Q20, Q200		Q25, Q250		Q300		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		170		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		170		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		75		100		120	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60	0	60	0	105	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	60	0	60	0	60	0	105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	Operating Temp Range
Storage Temperature	$-65°C$ to $+150°C$
All Input Voltages with Respect to Ground (Note 10)	$+6.5V$ to $-0.6V$
All Output Voltages with Respect to Ground (Note 10)	$V_{CC}+1.0V$ to $GND-0.6V$
V_{PP} Supply Voltage with Respect to Ground During Programming	$+14.0V$ to $-0.6V$
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
V_{CC} Supply Voltage with Respect to Ground	$+7.0V$ to $-0.6V$

Operating Conditions (Note 7)

Temperature Range	
NMC27C256QE200, 250	$-40°C$ to $+85°C$
NMC27C256QM250, M350	$-55°C$ to $+125°C$
V_{CC} Power Supply	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		6	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	µA
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -400$ µA	2.4			V
V_{OL2}	Output Low Voltage	I_{OH} = 0 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 µA	$V_{CC} - 0.1$			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256Q						Units
			E200		E250 M250		M350		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		350	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		100		120	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60	0	105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	60	0	60	0	105	ns

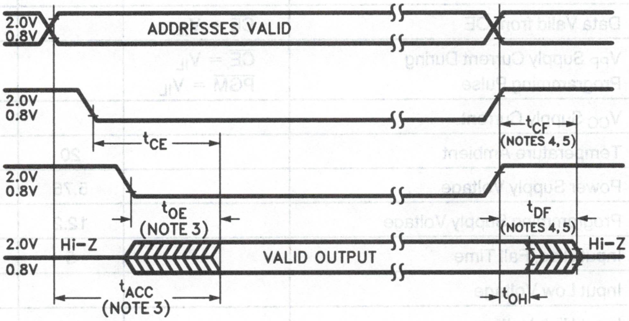
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Timing Measurement Reference Level	
		Inputs	0.8V and 2V
Input Rise and Fall Times	≤5 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6, 7 & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{\text{OE}}$ Setup Time		2			µs
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{\text{CE}} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
t_{OE}	Data Valid from $\overline{\text{OE}}$	$\overline{\text{CE}} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{\text{CE}} = V_{IL}$ $\overline{\text{PGM}} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

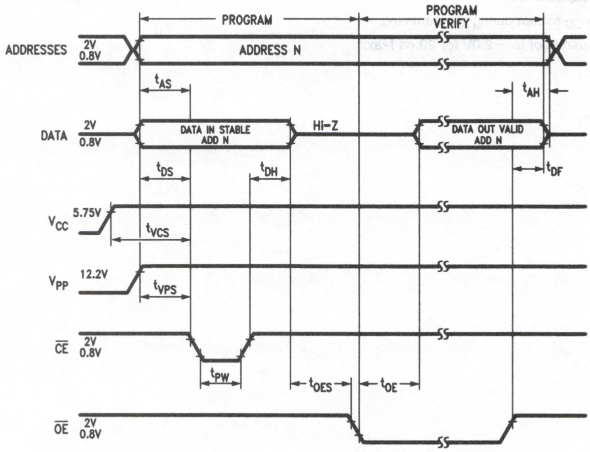
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Interactive Program Algorithm, at typical power supply voltages and timings.

Programming Waveforms (Note 3)


PROGRAM
PROGRAM VERIFY
ADDRESSES
2V
0.8V
ADDRESS N
t_{AS}
t_{AH}
DATA
2V
0.8V
DATA IN STABLE ADD N
HI-Z
DATA OUT VALID ADD N
t_{DS}
t_{DH}
t_{DF}
V_{CC}
5.75V
t_{VCS}
V_{PP}
12.2V
t_{VPS}
$\overline{\text{CE}}$
2V
0.8V
t_{PW}
t_{OES}
t_{OE}
$\overline{\text{OE}}$
2V
0.8V

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Interactive Programming Algorithm Flow Chart

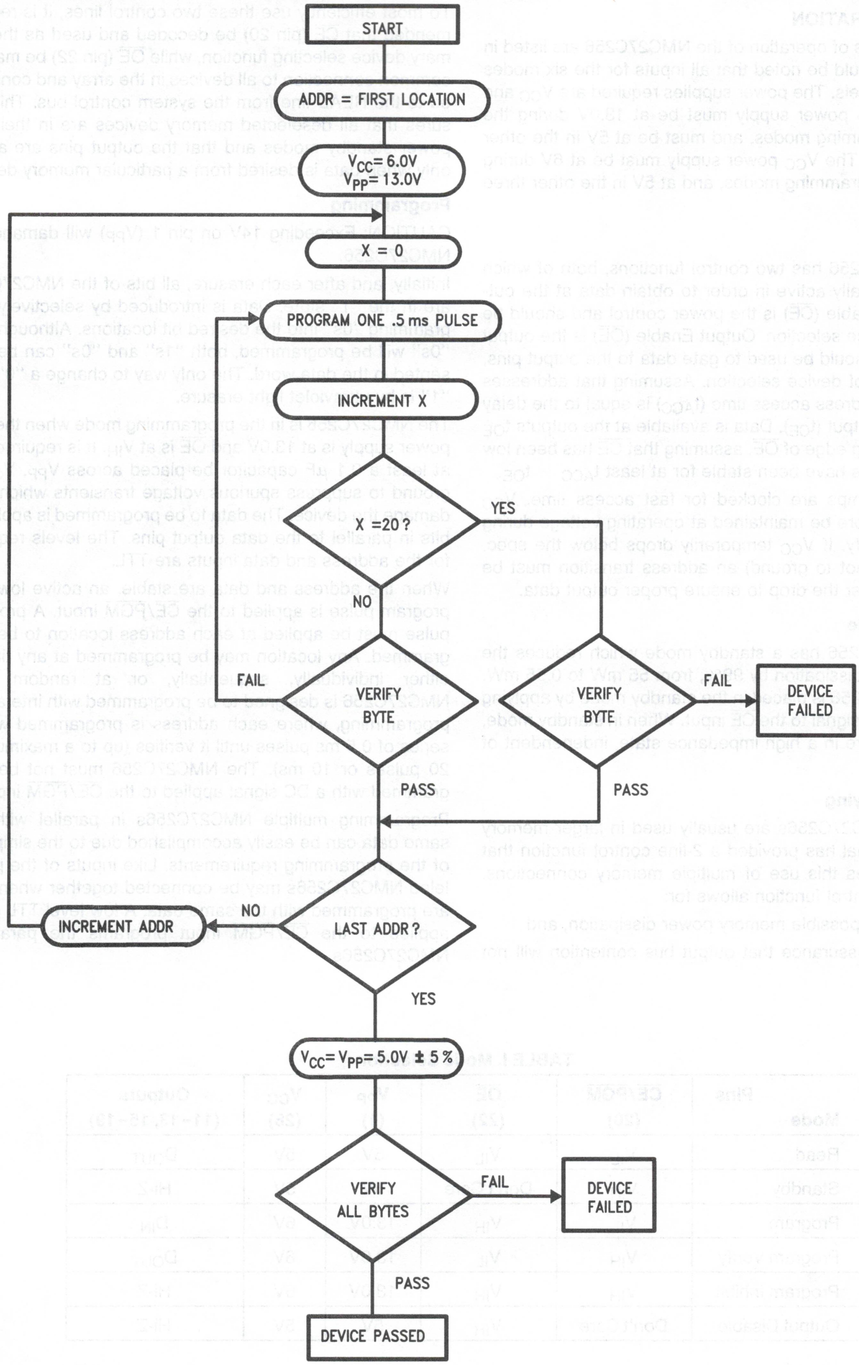
START
ADDR = FIRST LOCATION
V_{CC}= 6.0V
V_{PP}= 13.0V
X = 0
PROGRAM ONE .5 ms PULSE
INCREMENT X
X =20 ?
YES
NO
FAIL
VERIFY BYTE
FAIL
VERIFY BYTE
DEVICE FAILED
PASS
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC}= V_{PP}= 5.0V ± 5%
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

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FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C256 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C256 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C256 is placed in the standby mode by applying a CMOS high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Output OR-Tying

Because NMC27C256s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{\text{CE}}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{\text{OE}}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C256.

Initially, and after each erasure, all bits of the NMC27C256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C256 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{\text{OE}}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low TTL program pulse is applied to the $\overline{\text{CE}/\text{PGM}}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27C256 is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The NMC27C256 must not be programmed with a DC signal applied to the $\overline{\text{CE}/\text{PGM}}$ input.

Programming multiple NMC27C256s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C256s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{\text{CE}/\text{PGM}}$ input programs the paralleled NMC27C256s.

TABLE I. Mode Selection

Pins Mode	$\overline{\text{CE}/\text{PGM}}$ (20)	$\overline{\text{OE}}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}	13.0V	6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	13.0V	6V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	13.0V	6V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	5V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C256s may be common. A TTL low level program pulse applied to an NMC27C256's $\overline{CE}/\overline{PGM}$ input with V_{PP} at 13.0V will program that NMC27C256. A TTL high level $\overline{CE}$ input inhibits the other NMC27C256s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C256 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming, opaque labels should be placed over the NMC27C256's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C256 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C256 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NMC27C256 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Minimum NMC27C256 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C256B High Speed Version 262,144-Bit (32k x 8) UV Erasable CMOS PROM

General Description

The NMC27C256B is a high-speed 256k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C256B is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

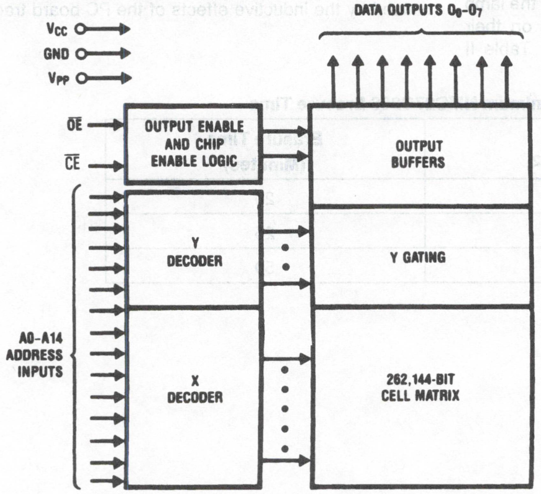
The NMC27C256B is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active power: 110 mW max
  - — Standby power: 0.55 mW max
- Optimal EPROM for total CMOS systems
- Extended temperature range (NMC27C256BQE), −40°C to +85°C, and military temperature range (NMC27C256BQM), −55°C to +125°C available
- Pin compatible with NMOS 256k EPROMs
- Fast and reliable programming—100 µs typical/byte
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/9125-1

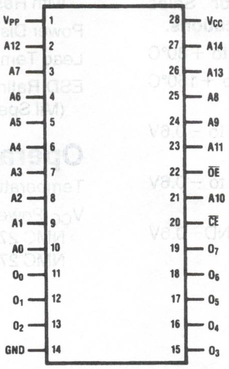
Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C128 27128	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C256BQ
Dual-In-Line Package



27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE/PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

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Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C256B pins.

Order Number NMC27C256BQ
See NS Package Number J28AQ

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C256BQ15	150
NMC27C256BQ20	200
NMC27C256BQ25	250

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BQ150	150
NMC27C256BQ200	200
NMC27C256BQ250	250

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BQE150	150
NMC27C256BQE200	200

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BQM150	150
NMC27C256BQM200	200

NOTE: For plastic DIP and surface mount PLCC package requirements please refer to NMC27C256BN data sheet.

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltages with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	
NMC 27C256BQ15, 20, 25	+5V ±5%
NMC 27C256BQ150, 200, 250	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{\text{CE}} = V_{IH}$			1.0	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{\text{CE}} = V_{IL}$, f = 5 MHz All Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{\text{CE}}$ = GND, f = 5 MHz All Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{\text{CE}} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{\text{CE}} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256B						Units
			Q15, Q150		Q20, Q200		Q25, Q250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$		150		200		250	ns
t_{CE}	$\overline{\text{CE}}$ to Output Delay	$\overline{\text{OE}} = V_{IL}$		150		200		250	ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay	$\overline{\text{CE}} = V_{IL}$		60		75		100	ns
t_{DF}	$\overline{\text{OE}}$ High to Output Float	$\overline{\text{CE}} = V_{IL}$	0	50	0	55		60	ns
t_{CF}	$\overline{\text{CE}}$ High to Output Float	$\overline{\text{OE}} = V_{IL}$	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{\text{CE}}$ or $\overline{\text{OE}}$, Whichever Occurred First	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltages with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC}+1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

V_{CC} Power Supply	5V ±10%
Temperature Range	
NMC27C256BQE150, 200	−40°C to +85°C
NMC27C256BQM150, 200	−55°C to +125°C

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz All Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz All Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC}+1$	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	$V_{CC} - 0.1$			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256B				Units
			QE150, QM150		QE200, QM200		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	55	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

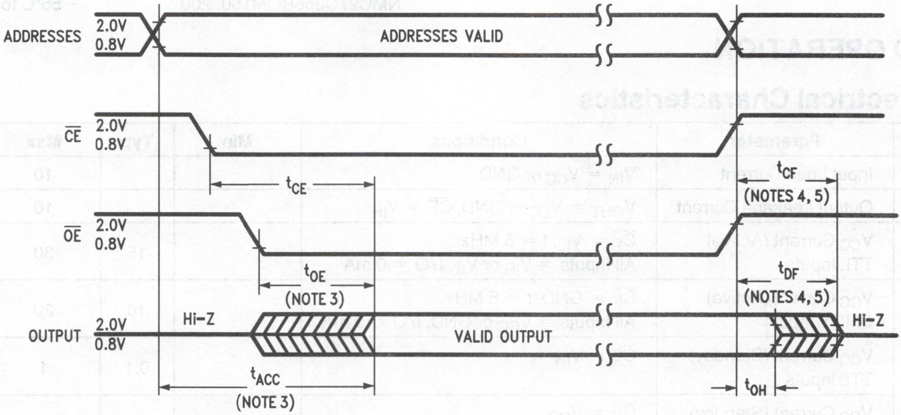
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) $- 0.10V$;
Low to TRI-STATE, the measured V_{OL1} (DC) $+ 0.10V$.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC} + 1.0V$ to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

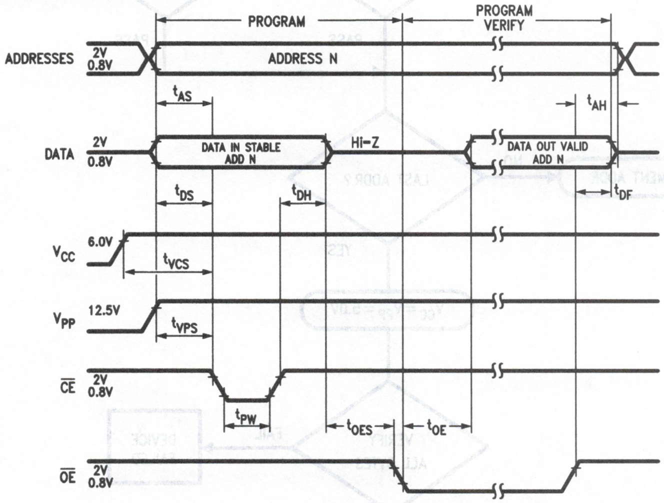
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to $-2.0V$ for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay		0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{OE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms


PROGRAM
PROGRAM VERIFY
ADDRESSES
2V
0.8V
ADDRESS N
t_{AS}
t_{AH}
DATA
2V
0.8V
DATA IN STABLE ADD N
Hi-Z
DATA OUT VALID ADD N
t_{DS}
t_{DH}
t_{DF}
V_{CC}
6.0V
t_{VCS}
V_{PP}
12.5V
t_{VPS}
$\overline{CE}$
2V
0.8V
t_{PW}
t_{OES}
t_{OE}
$\overline{OE}$
2V
0.8V

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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart (Note 4)

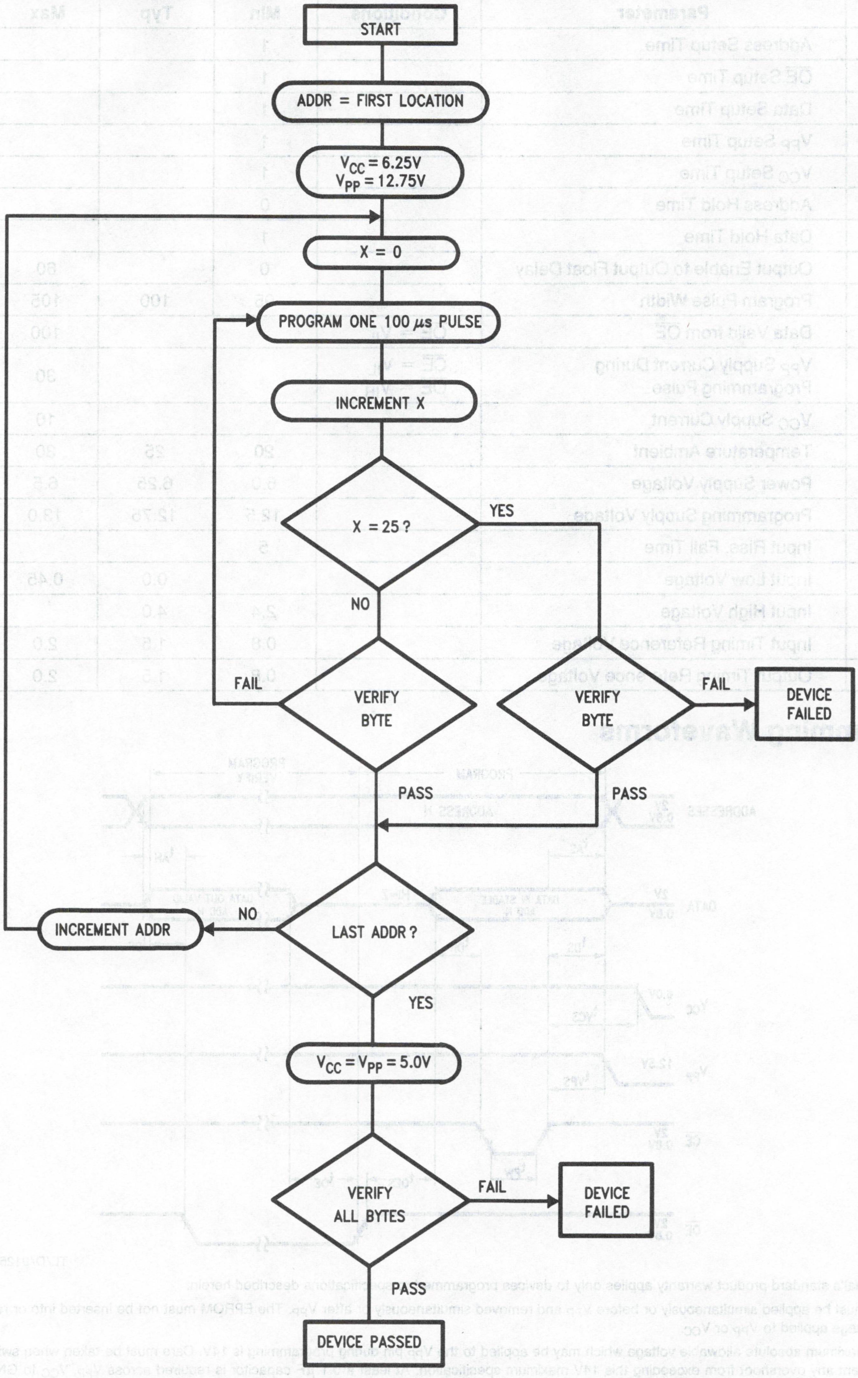
START
ADDR = FIRST LOCATION
$V_{CC} = 6.25V$
$V_{PP} = 12.75V$
X = 0
PROGRAM ONE 100 μs PULSE
INCREMENT X
X = 25 ?
YES
NO
FAIL
VERIFY BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
$V_{CC} = V_{PP} = 5.0V$
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

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FIGURE 1

Interactive Programming Flow Chart (Note 4)

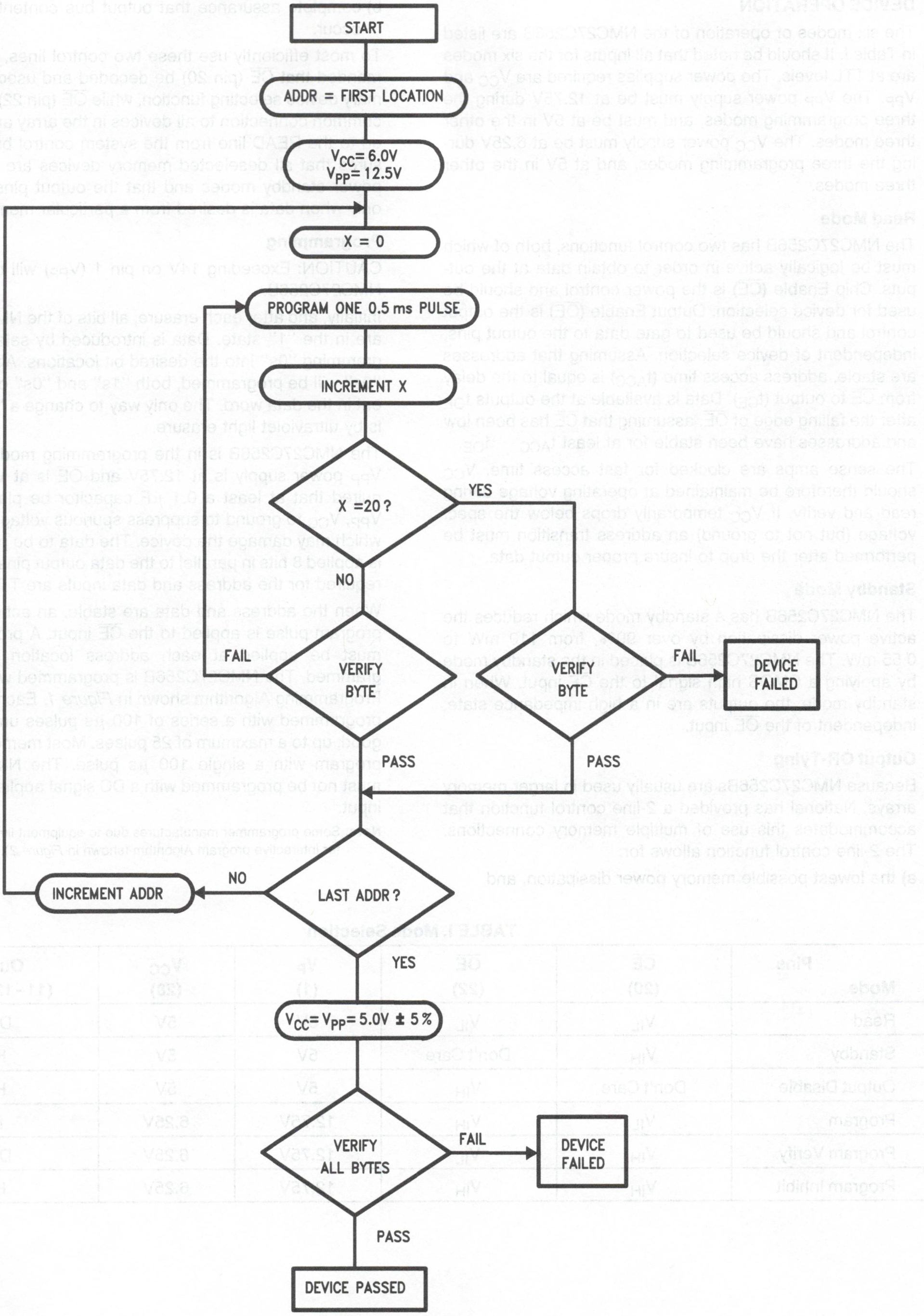

START
ADDR = FIRST LOCATION
V_{CC}= 6.0V
V_{PP}= 12.5V
X = 0
PROGRAM ONE 0.5 ms PULSE
INCREMENT X
X =20 ?
YES
NO
FAIL
VERIFY BYTE
PASS
FAIL
VERIFY BYTE
DEVICE FAILED
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC}= V_{PP}= 5.0V ± 5%
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
TL/D/9125–6

FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C256B are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C256B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C256B has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C256B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C256Bs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C256B.

Initially, and after each erasure, all bits of the NMC27C256B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C256B is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C256B is programmed with the Fast Programming Algorithm shown in *Figure 1.* Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C256B must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Note: Some programmer manufactures due to equipment limitation may offer interactive program Algorithm (shown in *Figure 2*).

TABLE I. Mode Selection

Pins Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_P (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	Hi-Z

Functional Description (Continued)

Programming multiple NMC27C256Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C256B may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C256B.

Program Inhibit

Programming multiple NMC27C256Bs in parallel with different data is also easily accomplished. Except $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NMC27C256Bs may be common. A TTL low level program pulse applied to an NMC27C256B $\overline{CE}$ input with V_{PP} at 12.75V will program that NMC27C256B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C256Bs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

Manufacturer's Identification Code

The NMC27C256B has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for NMC27C256B is "8F04", where "8F" designates that it is made by National Semiconductor, and "04" designates a 256k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A14, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C256B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C256B window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C256B is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C256B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C256B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

TABLE III. Minimum NMC27C256B Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C256BN
High Speed Version 262,144-Bit (32k x 8) One-Time Programmable CMOS PROM

General Description

The NMC27C256BN is a high-speed 256k one-time programmable CMOS PROM, ideally suited for applications where fast turnaround and low power consumption are important requirements.

The NMC27C256BN is designed to operate with a single +5V power supply with ±5% or ±10% tolerance.

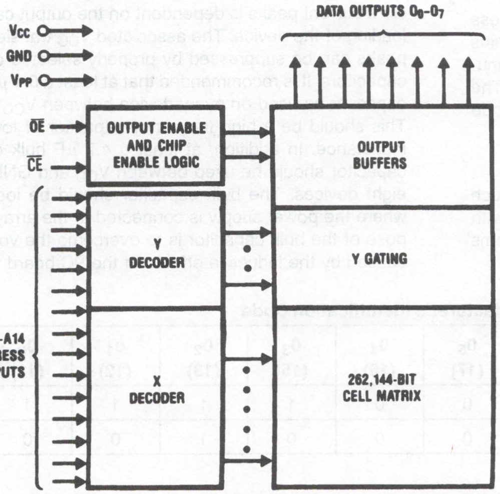
The NMC27C256BN is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be done once. Also the plastic molded package works well in auto insertion equipment used in automated assembly lines.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active power: 110 mW max
  - — Standby power: 0.55 mW max
- Pin compatible with NMOS 256k EPROMs
- Fast and reliable programming—100 µs typical/byte
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/9691–1

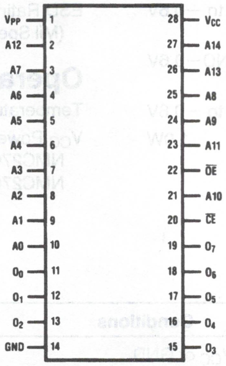
Pin Names

A0–A14	Addresses
CE	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C128 27128	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C256BN
Dual-In-Line Package



TL/D/9691–2

27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/PGM$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C256BN pins.

Order Number NMC27C256BN
See NS Package Number N28B

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C256BN15	150
NMC27C256BN20	200
NMC27C256BN25	250

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BN150	150
NMC27C256BN200	200
NMC27C256BN250	250

Note: For non-commercial temperature range parts, call factory.

Extended Temp. Range (−40°C to +85°C)
V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C256BNE15	150
NMC27C256BNE20	200
NMC27C256BNE25	250

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BNE150	150
NMC27C256BNE200	200
NMC27C256BNE250	250

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	
NMC27C256BN15, 20, 25	+5V ±5%
NMC27C256BN150, 200, 250	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			1	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	µA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 µA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256B						Units
			N15, N150		N20, N200		N25, N250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns

EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltages with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

Temperature Range	−40°C to +85°C
V_{CC} Power Supply	
NMC27C256BNE15, 20, 25	+5V ±5%
NMC27C256BNE150, 200, 250	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz All Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz All Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	µA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.40	V
V_{OH1}	Output High Voltage	$I_{OH} = -1.6$ mA	3.5			V
V_{OL2}	Output Low Voltage	$I_{OL} = 10$ µA			0.1	V
V_{OH2}	Output High Voltage	$I_{OH} = -10$ µA	$V_{CC} - 0.1$			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256B						Units
			NE15, NE150		NE20, NE200		NE25, NE250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

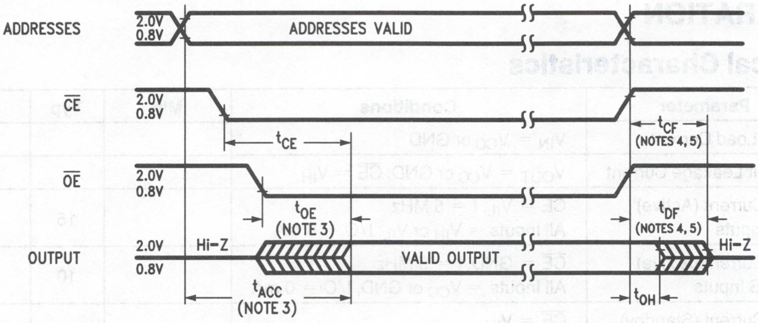
Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	10	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC} + 1.0V$ to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

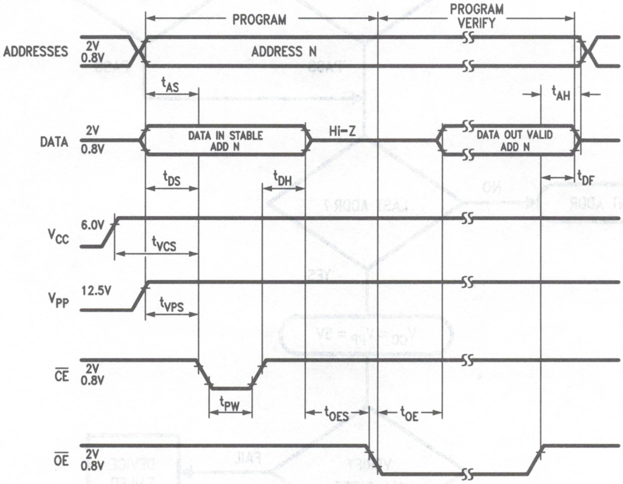
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to $-2.0V$ for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay		0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{OE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	ns
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	ns

Programming Waveforms



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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart (Note 4)

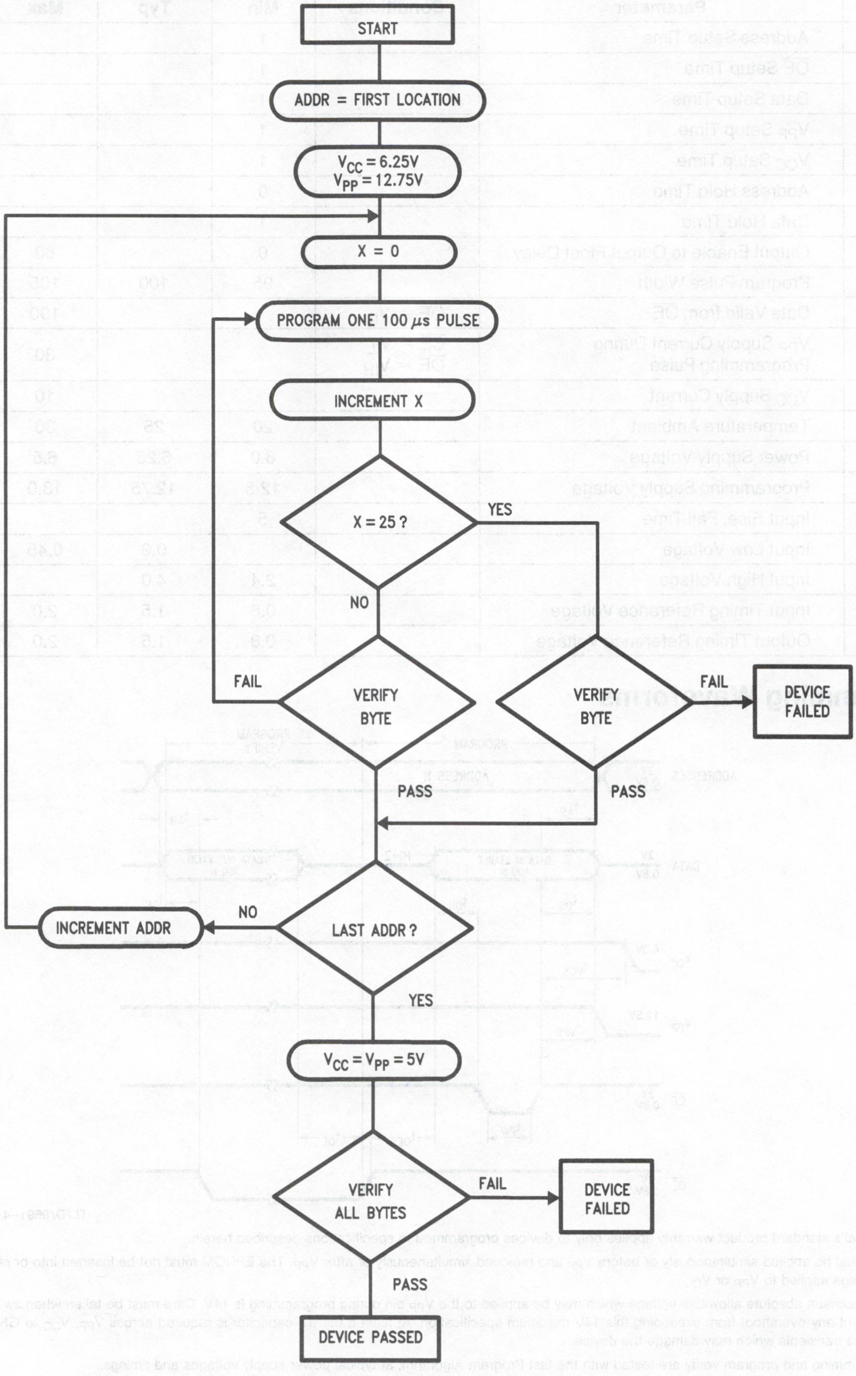
START
ADDR = FIRST LOCATION
V_{CC} = 6.25V
V_{PP} = 12.75V
X = 0
PROGRAM ONE 100 μs PULSE
INCREMENT X
X = 25 ?
YES
NO
FAIL
VERIFY BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC} = V_{PP} = 5V
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

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FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)

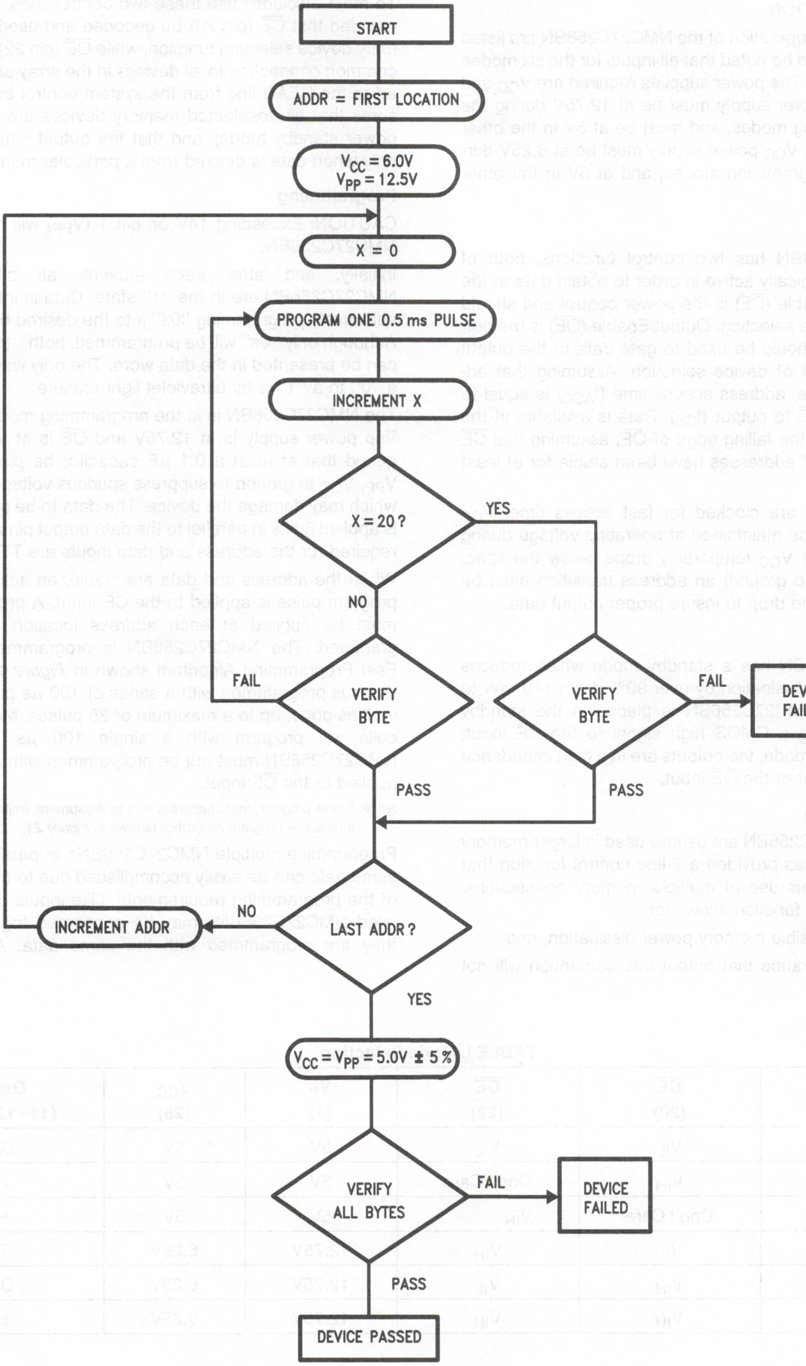
START
ADDR = FIRST LOCATION
V_{CC} = 6.0V
V_{PP} = 12.5V
X = 0
PROGRAM ONE 0.5 ms PULSE
INCREMENT X
X = 20 ?
YES
NO
FAIL
VERIFY BYTE
FAIL
VERIFY BYTE
DEVICE FAILED
PASS
PASS
LAST ADDR ?
NO
INCREMENT ADDR
YES
V_{CC} = V_{PP} = 5.0V ± 5%
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C256BN are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C256BN has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C256BN has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C256BN is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C256BN are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C256BN.

Initially, and after each erasure, all bits of the NMC27C256BN are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C256BN is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C256BN is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C256BN must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Note: Some program manufacturers due to equipment limitation may offer interactive program Algorithm (shown in *Figure 2*).

Programming multiple NMC27C256BNs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C256BNs may be connected together when they are programmed with the same data. A low level

TABLE I. Mode Selection

Pins Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_P (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	Hi-Z

Functional Description (Continued)

TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C256BNs.

The NMC27C256BN is packaged in a plastic molded package which does not have a transparent lid. Therefore the memory cannot be erased. This means that after a user has programmed a memory cell to a "0" it cannot be changed back to a "1".

If an application requires erasing and reprogramming, the NMC27C256BQ UV erasable PROM in a windowed package should be used.

Program Inhibit

Programming multiple NMC27C256BNs in parallel with different data is also easily accomplished. Except $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NMC27C256BNs may be common. A TTL low level program pulse applied to an NMC27C256BNs $\overline{CE}$ input with V_{PP} at 12.75V will program that NMC27C256BN. A TTL high level $\overline{CE}$ input inhibits the other NMC27C256BNs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

Manufacturer's Identification Code

The NMC27C256BN has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for NMC27C256BN is "8F04", where "8F" designates that it is made by National Semiconductor, and "04" designates a 256k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A14, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

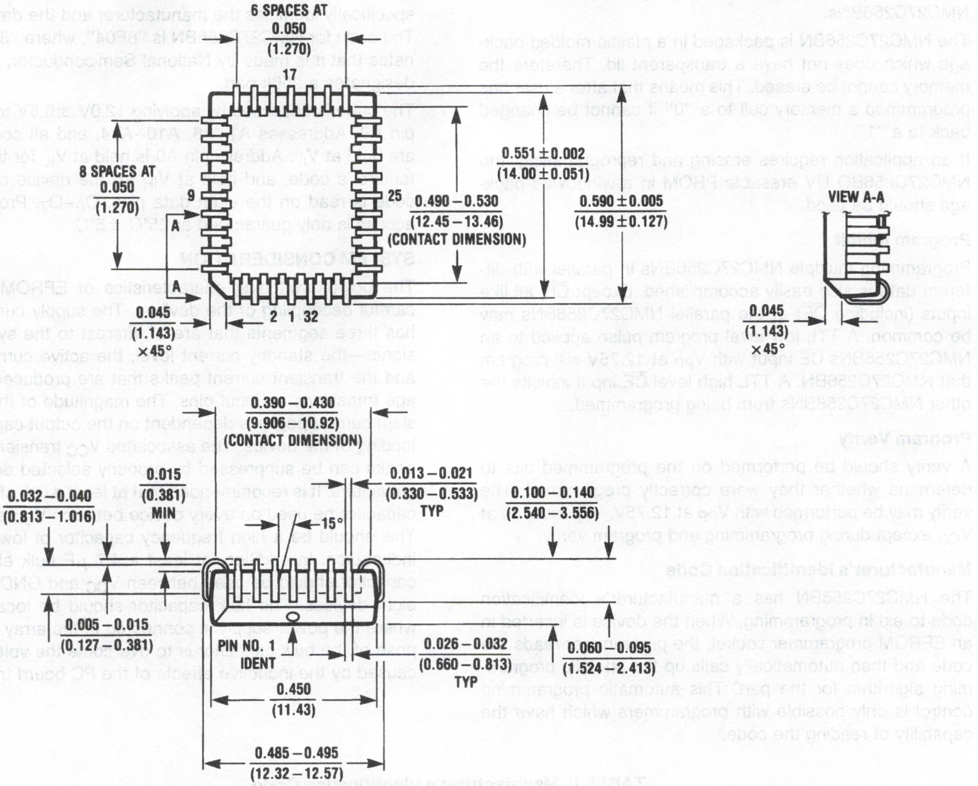
SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

Packaging Information


6 SPACES AT
0.050
(1.270)
17
8 SPACES AT
0.050
(1.270)
9
25
A
A
0.551 ± 0.002
(14.00 ± 0.051)
0.490 – 0.530
(12.45 – 13.46)
(CONTACT DIMENSION)
0.590 ± 0.005
(14.99 ± 0.127)
VIEW A-A
0.045
(1.143)
×45°
2
32
0.045
(1.143)
×45°
0.390 – 0.430
(9.906 – 10.92)
(CONTACT DIMENSION)
0.015
(0.381)
MIN
0.032 – 0.040
(0.813 – 1.016)
0.013 – 0.021
(0.330 – 0.533)
TYP
0.100 – 0.140
(2.540 – 3.556)
15°
0.005 – 0.015
(0.127 – 0.381)
PIN NO. 1
IDENT
0.026 – 0.032
(0.660 – 0.813)
TYP
0.060 – 0.095
(1.524 – 2.413)
0.450
(11.43)
0.485 – 0.495
(12.32 – 12.57)

TL/D/9691-7

32-Lead PLCC Package
Order Number NMC27C256

National Semiconductor

PRELIMINARY

NMC27C512A
524,288-Bit (64k x 8) UV Erasable CMOS PROM

General Description

The NMC27C512A is a high-speed 512k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C512A is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

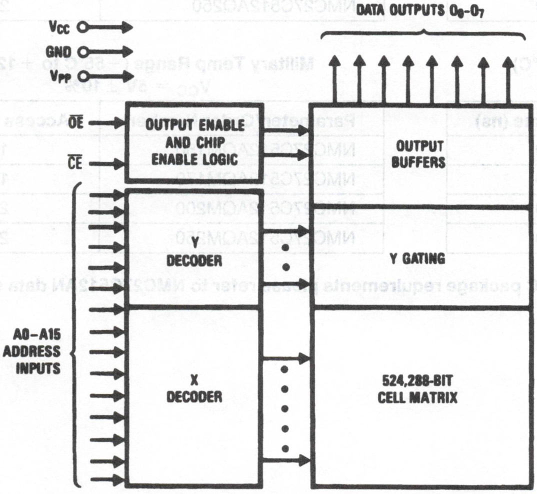
The NMC27C512A is packaged in a 28-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active Power: 110 mW max
  - — Standby Power: 0.55 mW max
- Optimum EPROM for total CMOS system
- Extended temperature range (NMC27C512AQE), −40°C to 85°C, and military temperature range (NMC27C512AQM), −55°C to 125°C, available
- Pin compatible with NMOS 512k EPROM
- Fast and reliable programming—100 μs typical/byte
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control.
- High current CMOS level output drivers

Block Diagram



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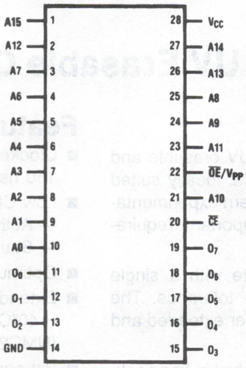
Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/Programming Voltage
O_0–O_7	Outputs
$\overline{PGM}$	Program

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732	27C16 2716
V_{PP}	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C512AQ
Dual-In-Line Package



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27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C256 27256
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10	A10
$\overline{CE}/V_{PP}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Order Part Number NMC27C512AQ
See NS Package Number J28AQ

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C512A pins.

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C512AQ15	150
NMC27C512AQ17	170
NMC27C512AQ20	200
NMC27C512AQ25	250

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512AQ150	150
NMC27C512AQ170	170
NMC27C512AQ200	200
NMC27C512AQ250	250

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512AQE150	150
NMC27C512AQE170	170
NMC27C512AQE200	200
NMC27C512AQE250	250

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512AQM150	150
NMC27C512AQM170	170
NMC27C512AQM200	200
NMC27C512AQM250	250

NOTE: For plastic DIP and surface mount PLCC package requirements please refer to NMC27C512AN data sheet.

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 & $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
ESD Rating (Mil. Std. 883C, Method 3015.2)	2000V
All Output Voltages with Respect to Ground (Note 9)	V_{CC} + 1.0V to GND − 0.6V
$\overline{OE}/V_{PP}$ Supply Voltage & A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 6)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	
NMC27C512AQ15, 17, 20, 25	5V ±5%
NMC27C512AQ150, 170, 200, 250	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	μA
I_{PP}	V_{PP} Load Current	$\overline{OE}/V_{PP} = V_{CC}$ or GND			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C512A								Units
			Q15, Q150		Q17, Q170		Q20, Q200		Q25, Q250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		75		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	55	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 & $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 9)	V_{CC}+1.0V to GND−0.6V
$\overline{OE}/V_{PP}$ Supply Voltage & A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
ESD Rating (Mil. Std. 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

Temperature Range	
NMC27C256BQE150, 170, 200, 250	−40°C to +85°C
NMC27C256BQM150, 170, 200, 250	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$\overline{OE}/V_{PP} = V_{CC}$ or GND			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C512A								Units
			QE150, QM150		QE170, QM170		QE200, QM200		QE250, QM250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		75		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	55	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

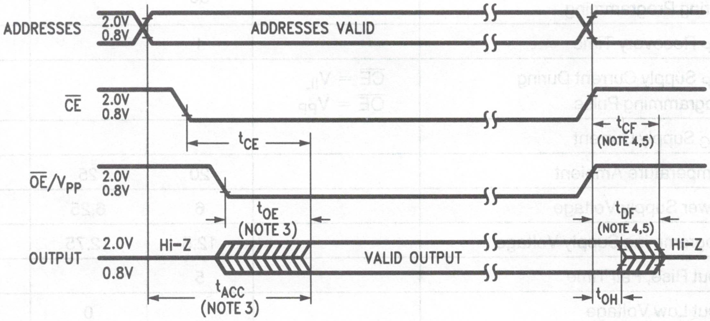
Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	20	25	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{cf}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OEH}	$\overline{OE}$ Hold Time		1			µs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			µs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
T_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2	V

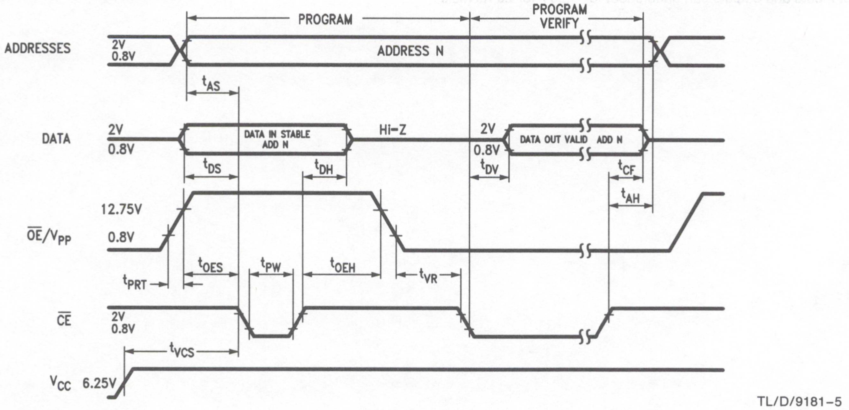
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least 0.1 µF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Programming Waveforms



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Fast Programming Algorithm Flow Chart (Note 4)

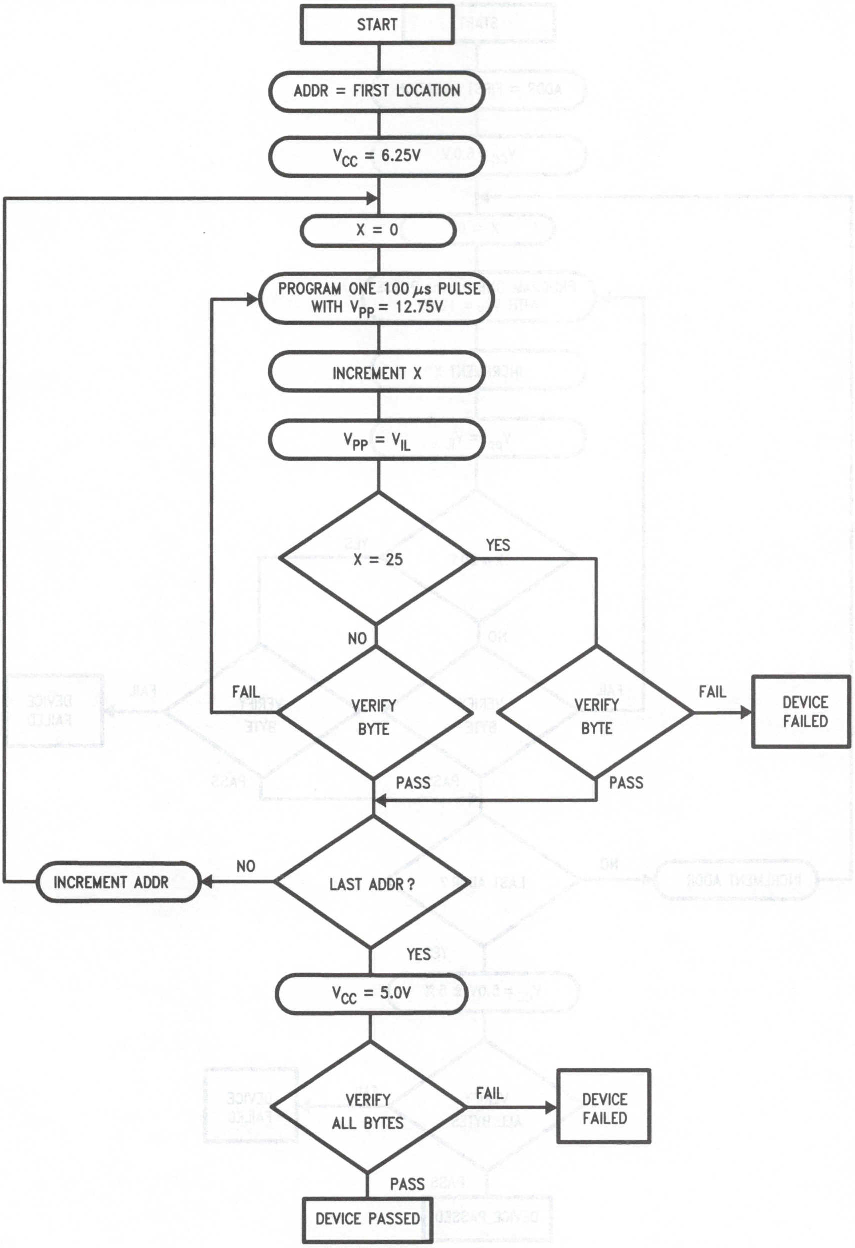
START
ADDR = FIRST LOCATION
VCC = 6.25V
X = 0
PROGRAM ONE 100 μs PULSE WITH VPP = 12.75V
INCREMENT X
VPP = VIL
X = 25
YES
NO
FAIL
VERIFY BYTE
FAIL
VERIFY BYTE
DEVICE FAILED
PASS
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
VCC = 5.0V
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

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FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)

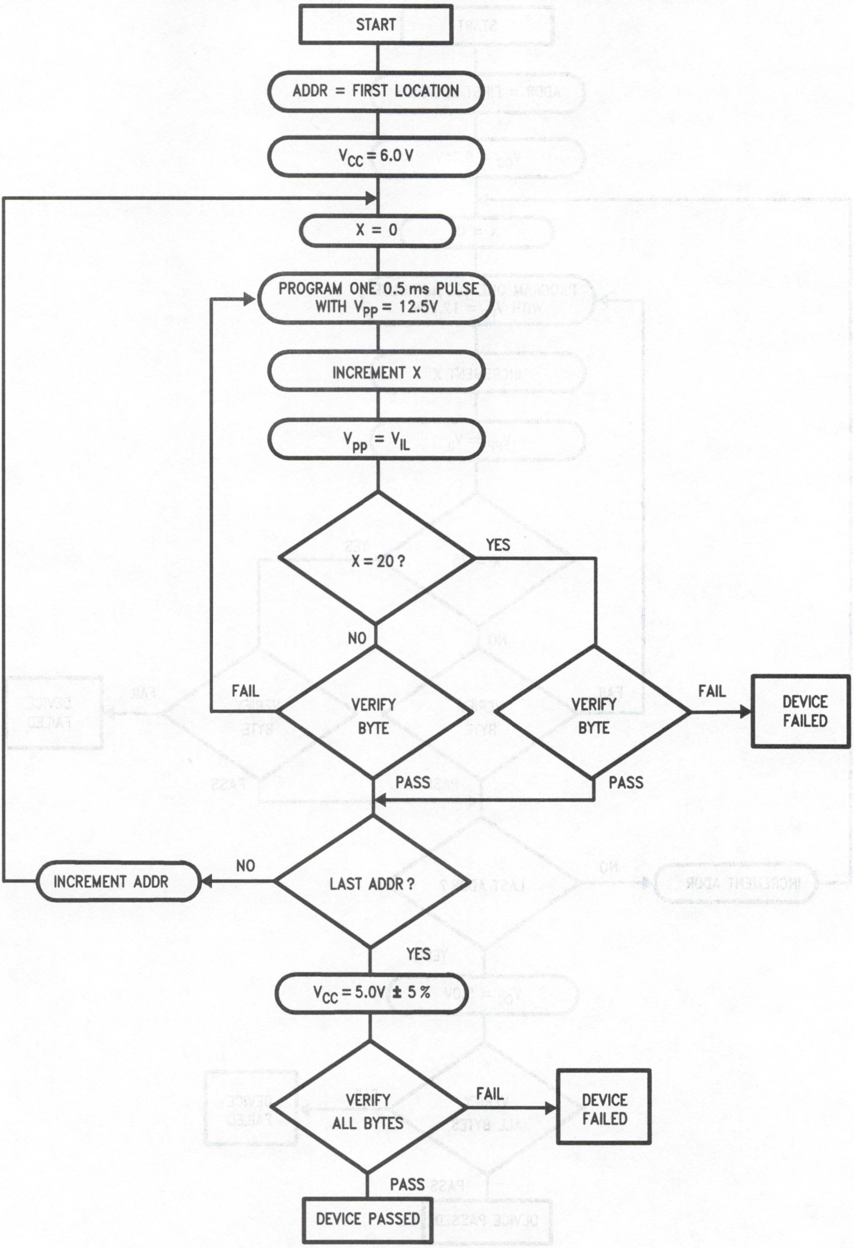
START
ADDR = FIRST LOCATION
V_{CC} = 6.0 V
X = 0
PROGRAM ONE 0.5 ms PULSE WITH V_{PP} = 12.5V
INCREMENT X
V_{PP} = V_{IL}
X = 20 ?
YES
NO
VERIFY BYTE
FAIL
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
LAST ADDR ?
NO
INCREMENT ADDR
YES
V_{CC} = 5.0V ± 5 %
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C512A are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{\text{OE}}/V_{PP}$ during programming. In the program mode the $\overline{\text{OE}}/V_{PP}$ input is pulsed from a TTL low level to 12.75V.

Read Mode

The NMC27C512A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C512A has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C512A is placed in the standby mode by applying a CMOS high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Output OR-Tying

Because NMC27C512A are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{\text{CE}}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{\text{OE}}/V_{PP}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 ($\overline{\text{OE}}/V_{PP}$) will damage the NMC27C512A.

Initially, and after each erasure, all bits of the NMC27C512A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C512A is in the programming mode when the $\overline{\text{OE}}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 µF capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{\text{CE}}$ input. A program pulse must be applied at each address location to be programmed.

The NMC27C512A is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 µs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will Program with a single 100 µs pulse.

The NMC27C512A must not be programmed with a DC signal applied to the $\overline{\text{CE}}$ input.

Programming multiple NMC27C512AS in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C512A may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{\text{CE}}$ input programs the paralleled NMC27C512A.

Note: Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (Shown in *Figure 2*).

TABLE I. Mode Selection

Pins / Mode	$\overline{\text{CE}}$ (20)	$\overline{\text{OE}}/V_{PP}$ (22)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5.0V	D_{OUT}
Standby	V_{IH}	Don't Care	5.0V	Hi-Z
Program	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	Hi-Z
Output Disable	Don't Care	V_{IH}	5.0V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C512A in parallel with different data is also easily accomplished. Except $\overline{\text{CE}}$ all like inputs (including $\overline{\text{OE}}$) of the parallel NMC27C512A may be common. A TTL low level program pulse applied to an NMC27C512A's $\overline{\text{CE}}$ input with $\overline{\text{OE}}/V_{PP}$ at 12.75V will program that NMC27C512A. A TTL high level $\overline{\text{CE}}$ input inhibits the other NMC27C512A from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{\text{OE}}/V_{PP}$ and $\overline{\text{CE}}$ at V_{IL}. data should be verified t_{DV} after the falling edge of $\overline{\text{CE}}$.

Manufacturer's Identification Code

The NMC27C512A has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C512A is, "8F 85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A15, $\overline{\text{CE}}$, and $\overline{\text{OE}}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C512A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming opaque labels should be placed over the NMC27C512A's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C512A is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C512A should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C512A erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk, capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	1	0	1	85

TABLE III. Minimum NMC27C512A Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C512AN 524,288-Bit (64k x 8) One Time Programmable CMOS PROM

General Description

The NMC27C512AN is a high-speed 512k UV one time programmable CMOS EPROM, ideally suited for applications where fast turnaround and low power consumption are important requirements.

The NMC27C512AN is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

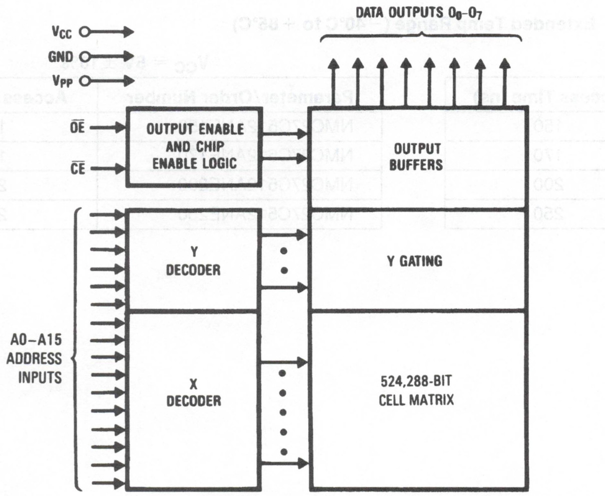
The NMC27C512AN is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be done once. Also the plastic molded package works well in auto insertion equipment used in automated assembly lines.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active Power: 110 mW max
  - — Standby Power: 0.55 mW max
- Optimum EPROM for total CMOS systems
- Pin compatible with NMOS 512k EPROMs
- Fast and reliable programming —100 µs typical/byte
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



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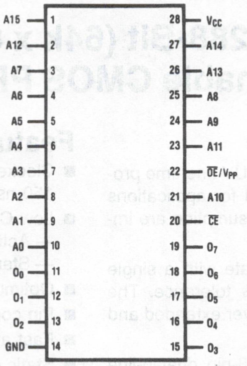
Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/Programming Voltage
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732	27C16 2716
V_{PP}	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C512AN
Dual-In-Line Package



27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C256 27256
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10	A10
$\overline{CE}/V_{PP}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

TL/D/8754-2

Order Number NMC27C512AN
See NS Package Number N28B

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C512AN pins.

Commercial Temp Range (0°C to +70°C)

V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C512AN15	150
NMC27C512AN17	170
NMC27C512AN20	200
NMC27C512AN25	250

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512AN150	150
NMC27C512AN170	170
NMC27C512AN200	200
NMC27C512AN250	250

Extended Temp Range (−40°C to +85°C)

V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C512ANE15	150
NMC27C512ANE17	170
NMC27C512ANE20	200
NMC27C512ANE25	250

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512ANE150	150
NMC27C512ANE170	170
NMC27C512ANE200	200
NMC27C512ANE250	250

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 and $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
All Output Voltages with Respect to Ground (Note 9)	V_{CC} +1 to GND −0.6V
$\overline{OE}/V_{PP}$ Supply Voltage and A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Std. 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	
NMC27C512AN15, 17, 20, 25	+5V ±5%
NMC27C512AN150, 170, 200, 250	+5V ±10%
Temperature Range	−40°C to +85°C
V_{CC} Power Supply	
NMC27C512ANE15, 17, 20, 25	+5V ±5%
NMC27C512ANE150, 170, 200, 250	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND $\overline{CE} = V_{IH}$		0.01	1	µA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		10	30	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		8	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	µA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 µA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C512AN/ANE								Units
			15, 150		17, 170		20, 200		25, 250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		75		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	55	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance Except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	10	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	16	20	pF

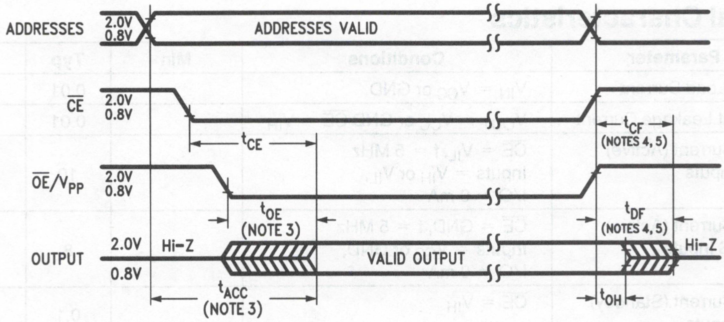
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) $-0.10V$.

Low to TRI-STATE, the measured V_{OL1} (DC) $+0.10V$.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC} + 1.0V$ to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.

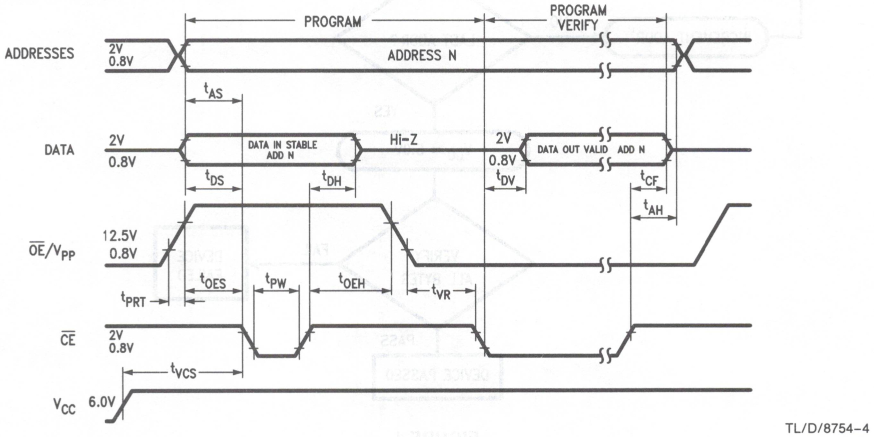
CL: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to $-2.0V$ for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V
t_{VCS}	V_{CC} Setup Time		1			μs

Programming Waveforms


PROGRAM
PROGRAM VERIFY
ADDRESSES
2V
0.8V
ADDRESS N
t_{AS}
DATA
2V
0.8V
DATA IN STABLE ADD N
Hi-Z
2V
0.8V
DATA OUT VALID ADD N
t_{DS}
t_{DH}
t_{DV}
t_{CF}
t_{AH}
$\overline{OE}/V_{PP}$
12.5V
0.8V
t_{OES}
t_{PW}
t_{OEH}
t_{VR}
t_{PRT}
$\overline{CE}$
2V
0.8V
t_{VCS}
V_{CC}
6.0V

TL/D/8754-4

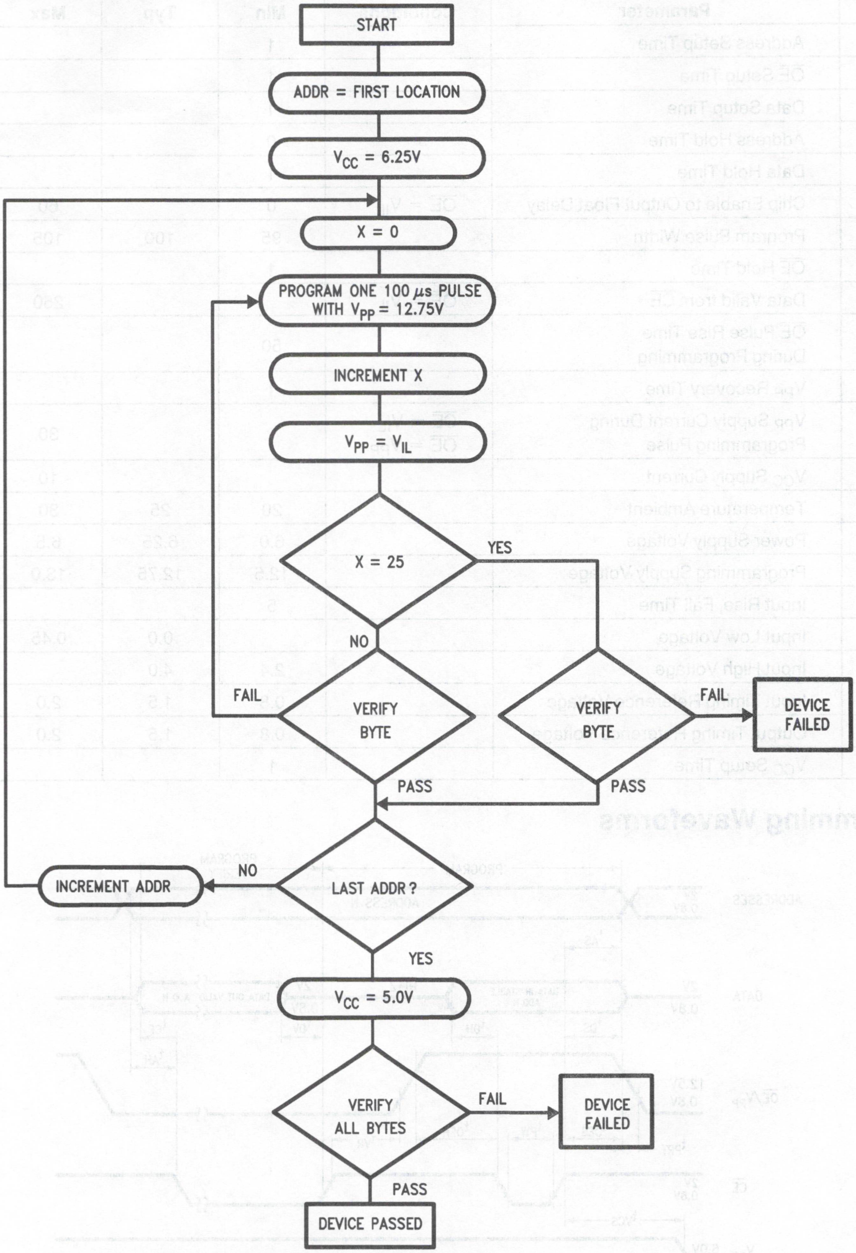
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm at typical power supply voltages and timings.

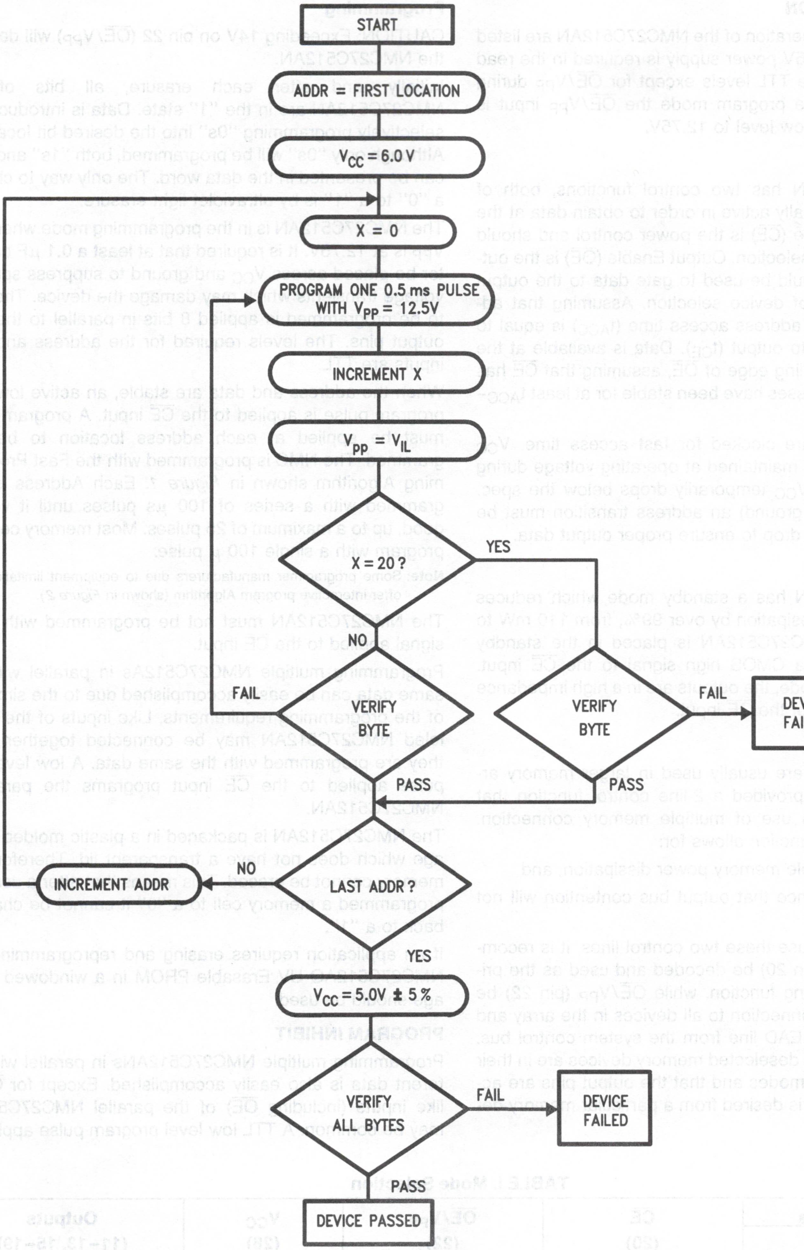
Fast Programming Algorithm Flow Chart (Note 4)


START
ADDR = FIRST LOCATION
V_{CC} = 6.25V
X = 0
PROGRAM ONE 100 μs PULSE WITH V_{PP} = 12.75V
INCREMENT X
V_{PP} = V_{IL}
X = 25
YES
NO
FAIL
VERIFY BYTE
PASS
FAIL
VERIFY BYTE
DEVICE FAILED
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC} = 5.0V
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

TL/D/8754-5

FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)


START
ADDR = FIRST LOCATION
V_{CC} = 6.0 V
X = 0
PROGRAM ONE 0.5 ms PULSE WITH V_{PP} = 12.5V
INCREMENT X
V_{PP} = V_{IL}
X = 20 ?
YES
NO
FAIL
VERIFY BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC} = 5.0V ± 5%
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

TL/D/8754–6

FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C512AN are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{\text{OE}}/V_{PP}$ during programming. In the program mode the $\overline{\text{OE}}/V_{PP}$ input is pulsed from a TTL low level to 12.75V.

Read Mode

The NMC27C512AN has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C512AN has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C512AN is placed in the standby mode by applying a CMOS high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{\text{CE}}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{\text{OE}}/V_{PP}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 ($\overline{\text{OE}}/V_{PP}$) will damage the NMC27C512AN.

Initially, and after each erasure, all bits of the NMC27C512AN are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C512AN is in the programming mode when $\overline{\text{OE}}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{\text{CE}}$ input. A program pulse must be applied at each address location to be programmed. The NMC is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μ pulse.

Note: Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (shown in *Figure 2*).

The NMC27C512AN must not be programmed with a DC signal applied to the $\overline{\text{CE}}$ input.

Programming multiple NMC27C512As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C512AN may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{\text{CE}}$ input programs the paralleled NMC27C512AN.

The NMC27C512AN is packaged in a plastic molded package which does not have a transparent lid. Therefore the memory cannot be erased. This means that after a user has programmed a memory cell to a "0" it cannot be changed back to a "1".

If an application requires erasing and reprogramming, the NMC27C512AQ UV Erasable PROM in a windowed package should be used.

PROGRAM INHIBIT

Programming multiple NMC27C512ANs in parallel with different data is also easily accomplished. Except for $\overline{\text{CE}}$ all like inputs (including $\overline{\text{OE}}$) of the parallel NMC27C512AN may be common. A TTL low level program pulse applied to

TABLE I. Mode Selection

Pins Mode	$\overline{\text{CE}}$ (20)	$\overline{\text{OE}}/V_{PP}$ (22)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5.0V	D_{OUT}
Standby	V_{IH}	Don't Care	5.0V	Hi-Z
Output Disable	Don't Care	V_{IH}	5.0V	Hi-Z
Program	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	Hi-Z

Functional Description (Continued)

an NMC27C512A's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that NMC27C512AN. A TTL high level $\overline{CE}$ input inhibits the other NMC27C512A from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C512AN has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for NMC27C512AN is "8F 85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A15, $\overline{CE}$ and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the eight data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

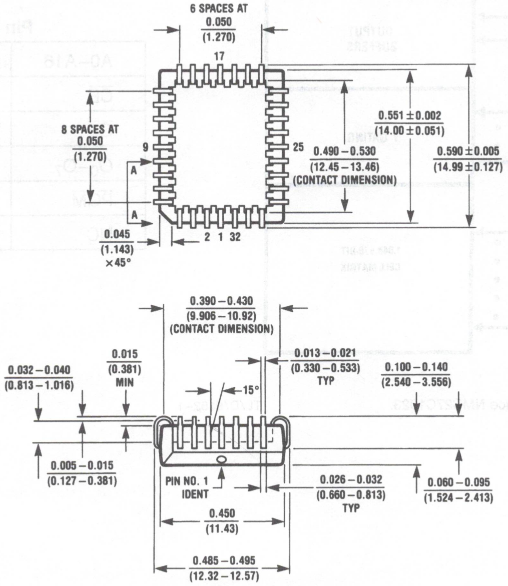
SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	1	0	1	85

Package Information


6 SPACES AT
0.050
(1.270)
17
8 SPACES AT
0.050
(1.270)
9
25
A
A
0.490–0.530
(12.45–13.46)
(CONTACT DIMENSION)
0.551±0.002
(14.00±0.051)
0.590±0.005
(14.99±0.127)
0.045
(1.143)
×45°
2 1 32
VIEW A-A
0.045
(1.143)
×45°
0.390–0.430
(9.906–10.92)
(CONTACT DIMENSION)
0.015
(0.381)
MIN
0.032–0.040
(0.813–1.016)
0.013–0.021
(0.330–0.533)
TYP
0.100–0.140
(2.540–3.556)
15°
0.005–0.015
(0.127–0.381)
PIN NO. 1
IDENT
0.026–0.032
(0.660–0.813)
TYP
0.060–0.095
(1.524–2.413)
0.450
(11.43)
0.485–0.495
(12.32–12.57)

TL/D/8754-7

32-Lead PLCC Package
Order Number NMC27C512AV

National Semiconductor

PRELIMINARY

NMC27C010 (Former NMC27C1023)* 1,048,576-Bit (128k x 8) UV Erasable CMOS PROM

General Description

The NMC27C010 is a high-speed 1024k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C010 is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

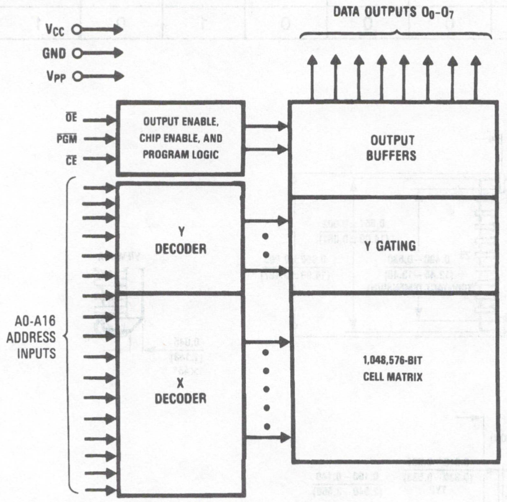
The NMC27C010 is packaged in a 32-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active power: 110 mW max
  - — Standby power: 0.55 mW max
- Extended temperature range (NMC27C010QE), −40°C to +85°C and military temperature range (NMC27C010QM), −55°C to +125°C, available
- Pin compatible with NMOS bytewide 1024k EPROMs
- Fast and reliable programming—100 µs typical/byte
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/9182-1

Pin Names

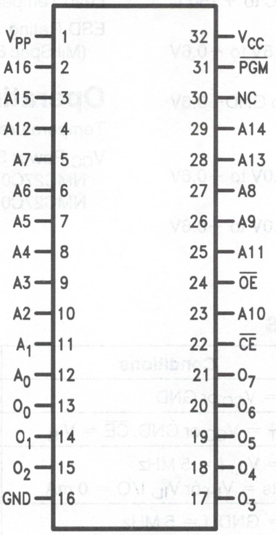
A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

*Some programmer manufacturers will call this device NMC27C1023.

Connection Diagram

NMC27C010Q
Dual-In-Line Package

4 Mbit	2 Mbit
V_{PP}	V_{PP}
A16	A16
A15	A15
A12	A12
A7	A7
A6	A6
A5	A5
A4	A4
A3	A3
A2	A2
A1	A1
A0	A0
O_0	O_0
O_1	O_1
O_2	O_2
GND	GND


V_{PP} 1
A16 2
A15 3
A12 4
A7 5
A6 6
A5 7
A4 8
A3 9
A2 10
A_1 11
A_0 12
O_0 13
O_1 14
O_2 15
GND 16
32 V_{CC}
31 PGM
30 NC
29 A14
28 A13
27 A8
26 A9
25 A11
24 $\overline{OE}$
23 A10
22 $\overline{CE}$
21 O_7
20 O_6
19 O_5
18 O_4
17 O_3

2 Mbit	4 Mbit
V_{CC}	V_{CC}
$\overline{PGM}$	A18
A17	A17
A14	A14
A13	A13
A8	A8
A9	A9
A11	A11
$\overline{OE}$	$\overline{OE}$
A10	A10
$\overline{CE}$	$\overline{CE}$
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3

TL/D/9182–2

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C010 pins.

Order Number NMC27C010Q
See NS Package Number J32AQ

Commercial Temperature Range (0°C to +70°C)
$V_{CC} = 5V \pm 5\%$

Parameter/Order Number	Access Time (ns)
NMC27C010Q15	150
NMC27C010Q17	170
NMC27C010Q20	200
NMC27C010Q25	250

Commercial Temperature Range (0°C to +70°C)
$V_{CC} = 5V \pm 10\%$

Parameter/Order Number	Access Time (ns)
NMC27C010Q150	150
NMC27C010Q170	170
NMC27C010Q200	200
NMC27C010Q250	250

Extended Temperature Range (−40°C to +85°C)
$V_{CC} = 5V \pm 10\%$

Parameter/Order Number	Access Time (ns)
NMC27C010QE170	170
NMC27C010QE200	200
NMC27C010QE250	250

Military Temperature Range (−55°C to +125°C)
$V_{CC} = 5V \pm 10\%$

Parameter/Order Number	Access Time (ns)
NMC27C010QM170	170
NMC27C010QM200	200
NMC27C010QM250	250

NOTE: Surface mount PLCC package available for commercial and extended temperature ranges only.

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	
NMC27C010Q15, 17, 20, 25	+5V ±5%
NMC27C010Q150, 170, 200, 250	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			1	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	µA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 µA	$V_{CC} - 0.1$			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C010								Units
			Q15, Q150		Q17, Q170		Q20, Q200		Q25, Q250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	$V_{CC}+1.0V$ to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C010QE150, 170, 200, 250	−40°C to +85°C
NMC27C010QM170, 200, 250	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	µA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC}+1$	V
V_{OL1}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.40	V
V_{OH1}	Output High Voltage	$I_{OH} = -1.6$ mA	3.5			V
V_{OL2}	Output Low Voltage	$I_{OL} = 10$ µA			0.1	V
V_{OH2}	Output High Voltage	$I_{OH} = -10$ µA	$V_{CC} - 0.1$			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C010Q								Units
			E150		E170, M170		E200, M200		E250, M250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

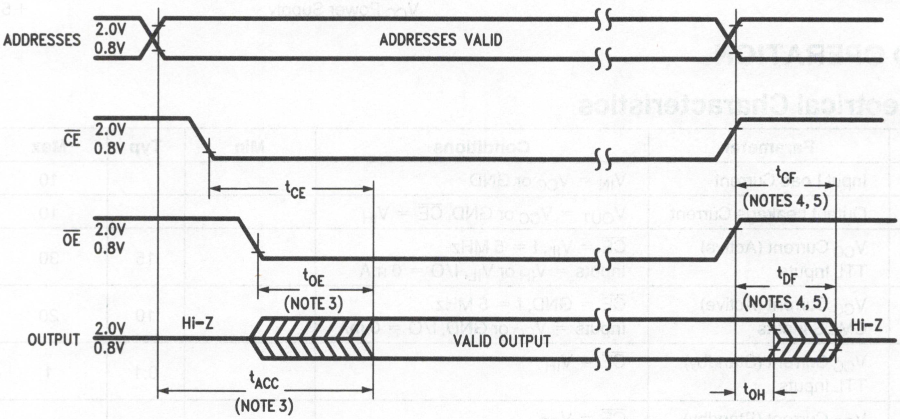
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, & 9)



TL/D/9182-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

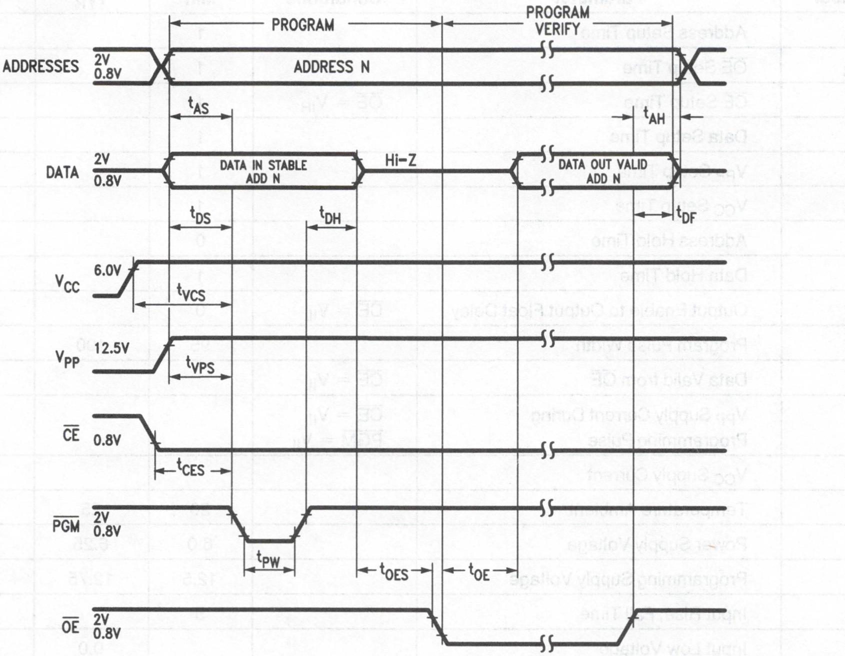
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)


PROGRAM
PROGRAM VERIFY
ADDRESSES
2V
0.8V
ADDRESS N
t_{AS}
t_{AH}
DATA
2V
0.8V
DATA IN STABLE ADD N
Hi-Z
DATA OUT VALID ADD N
t_{DS}
t_{DH}
t_{DF}
V_{CC}
6.0V
t_{VCS}
V_{PP}
12.5V
t_{VPS}
$\overline{CE}$
0.8V
t_{CES}
$\overline{PGM}$
2V
0.8V
t_{PW}
t_{OES}
t_{OE}
$\overline{OE}$
2V
0.8V

TL/D/9182–5

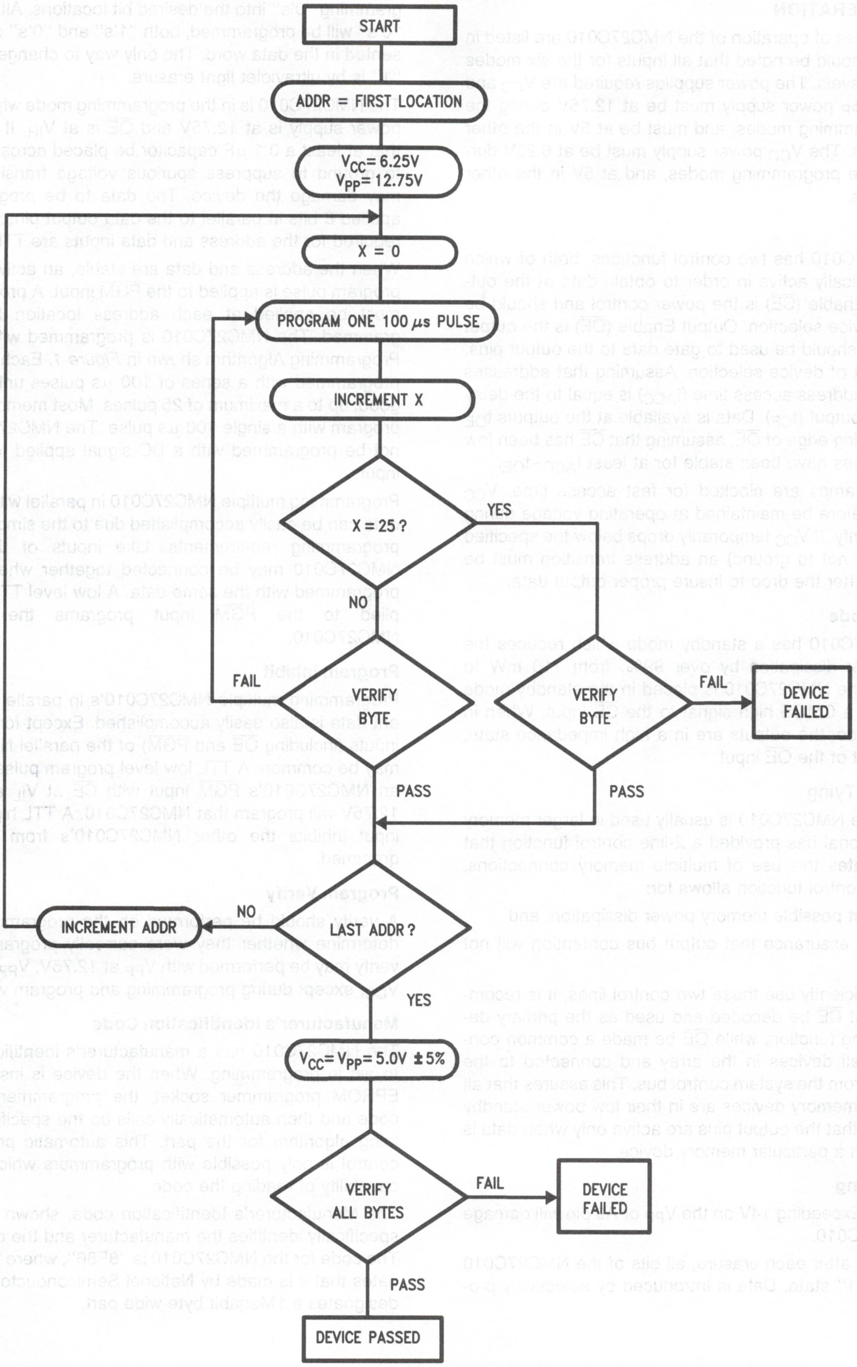
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart


START
ADDR = FIRST LOCATION
V_{CC}= 6.25V
V_{PP}= 12.75V
X = 0
PROGRAM ONE 100 µs PULSE
INCREMENT X
X = 25 ?
YES
NO
FAIL
VERIFY BYTE
FAIL
VERIFY BYTE
DEVICE FAILED
PASS
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC}= V_{PP}= 5.0V ±5%
FAIL
VERIFY ALL BYTES
DEVICE FAILED
PASS
DEVICE PASSED

TL/D/9182–6

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C010 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C010 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the specified voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C010 has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C010 is placed in the standby mode by applying a CMOS high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Output OR-Tying

Because the NMC27C010 is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{\text{CE}}$ be decoded and used as the primary device selecting function, while $\overline{\text{OE}}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the NMC27C010.

Initially, and after each erasure, all bits of the NMC27C010 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C010 is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{\text{OE}}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{\text{PGM}}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C010 is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C010 must not be programmed with a DC signal applied to the $\overline{\text{PGM}}$ input.

Programming multiple NMC27C010 in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel NMC27C010 may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{\text{PGM}}$ input programs the paralleled NMC27C010.

Program Inhibit

Programming multiple NMC27C010's in parallel with different data is also easily accomplished. Except for $\overline{\text{CE}}$ all like inputs (including $\overline{\text{OE}}$ and $\overline{\text{PGM}}$) of the parallel NMC27C010 may be common. A TTL low level program pulse applied to an NMC27C010's $\overline{\text{PGM}}$ input with $\overline{\text{CE}}$ at V_{IL} and V_{PP} at 12.75V will program that NMC27C010. A TTL high level $\overline{\text{CE}}$ input inhibits the other NMC27C010's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

Manufacturer's Identification Code

The NMC27C010 has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for the NMC27C010 is "8F86", where "8F" designates that it is made by National Semiconductor, and "86" designates a 1Megabit byte-wide part.

Functional Description (Continued)

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	Outputs (13–15, 17–21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	V_{CC}	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

TABLE II. Manufacturer's Identificatiion Code

Pins	A_0 (12)	O_7 (21)	O_6 (20)	O_5 (19)	O_4 (18)	O_3 (17)	O_2 (15)	O_1 (14)	O_0 (13)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	1	1	0	86

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C010 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

AFTER PROGRAMMING

Opaque labels should be placed over the NMC27C010 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C010 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC27C010 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C010 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

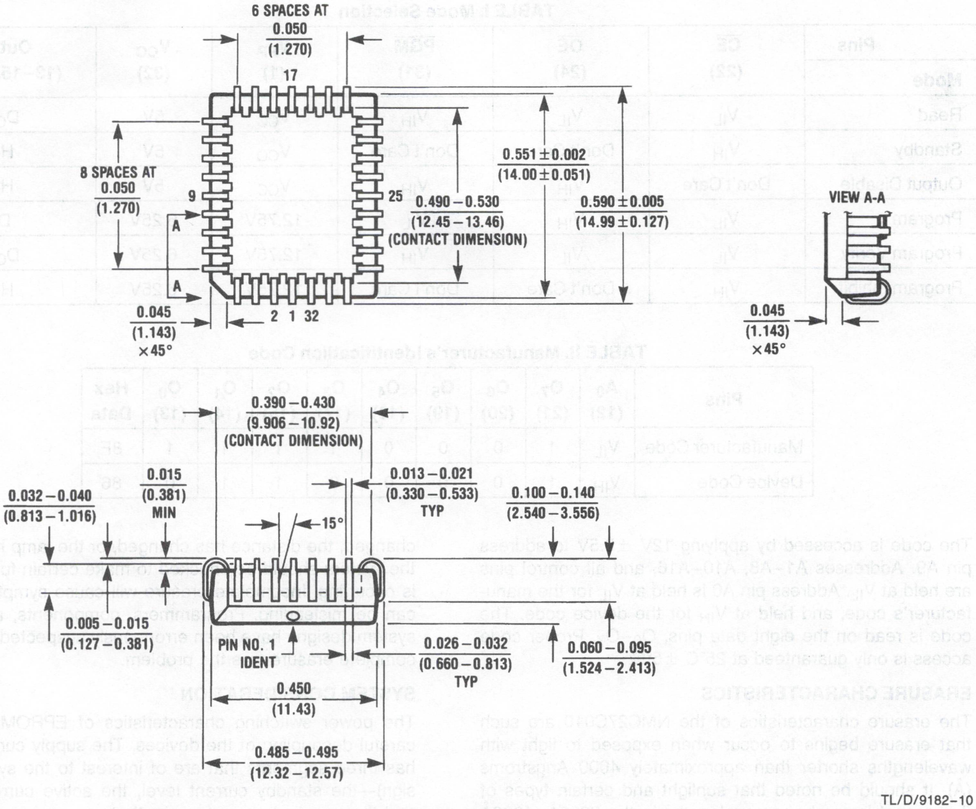
SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system design)—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE III. NMC27C010
Minimum Erasure Time

Light Intensity (μWatts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

Package Information


6 SPACES AT
0.050
(1.270)
17
8 SPACES AT
0.050
(1.270)
9
25
A
A
0.551 ± 0.002
(14.00 ± 0.051)
0.490 – 0.530
(12.45 – 13.46)
(CONTACT DIMENSION)
0.590 ± 0.005
(14.99 ± 0.127)
VIEW A-A
0.045
(1.143)
×45°
2 1 32
0.045
(1.143)
×45°
0.390 – 0.430
(9.906 – 10.92)
(CONTACT DIMENSION)
0.015
(0.381)
MIN
0.013 – 0.021
(0.330 – 0.533)
TYP
0.032 – 0.040
(0.813 – 1.016)
0.100 – 0.140
(2.540 – 3.556)
15°
0.005 – 0.015
(0.127 – 0.381)
PIN NO. 1
IDENT
0.026 – 0.032
(0.660 – 0.813)
TYP
0.060 – 0.095
(1.524 – 2.413)
0.450
(11.43)
0.485 – 0.495
(12.32 – 12.57)
TL/D/9182-10

32-Lead PLCC Package
Order Number NMC27C010V

National Semiconductor

PRELIMINARY

NMC27C1024
1,048,576-Bit (64k x 16) UV Erasable CMOS PROM

General Description

The NMC27C1024 is a high-speed 1024k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C1024 is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

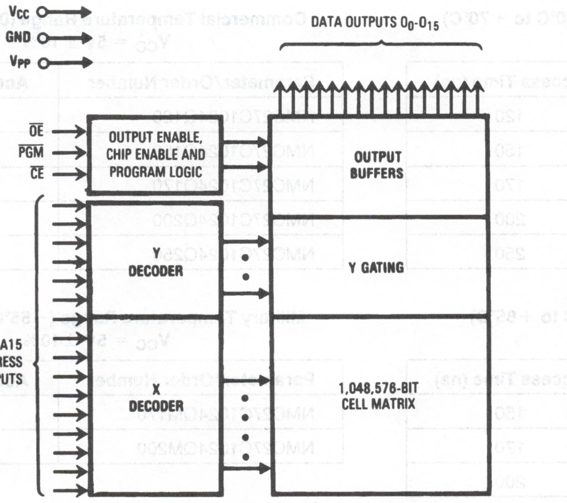
The NMC27C1024 is packaged in a 40-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 120 ns
- Low CMOS power consumption
  - — Active Power: 110 mW max
  - — Standby Power: 550 µW max
- Performance compatible to 16-bit and 32-bit microprocessors
- Extended temperature range (NMC27C1024QE), −40°C to +85°C, and military temperature range (NMC27C1024QM), −55°C to +125°C, available
- Pin compatible with NMOS wordwide 1024k EPROMs
- Fast and reliable programming—100 µs typical/byte
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's Identification Code for automatic programming control
- High current CMOS level output drivers

Block Diagram



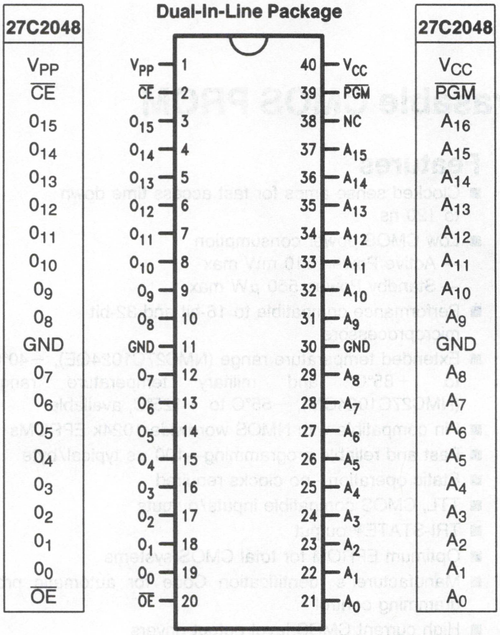
TL/D/8806–1

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O$_0$–O$_{15}$	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

NMC27C1024Q
Dual-In-Line Package

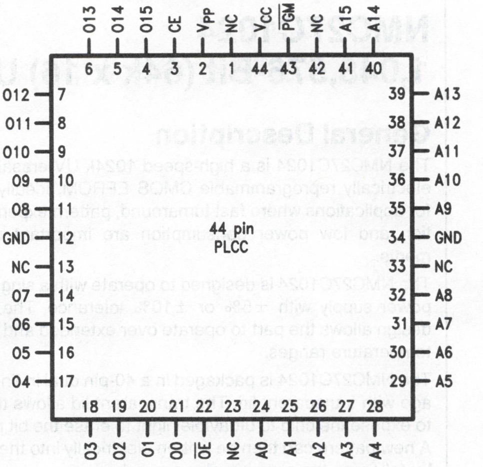

27C2048
V_{PP}
$\overline{CE}$
O_{15}
O_{14}
O_{13}
O_{12}
O_{11}
O_{10}
O_9
O_8
GND
O_7
O_6
O_5
O_4
O_3
O_2
O_1
O_0
$\overline{OE}$
V_{PP} 1
$\overline{CE}$ 2
O_{15} 3
O_{14} 4
O_{13} 5
O_{12} 6
O_{11} 7
O_{10} 8
O_9 9
O_8 10
GND 11
O_7 12
O_6 13
O_5 14
O_4 15
O_3 16
O_2 17
O_1 18
O_0 19
$\overline{OE}$ 20
40 V_{CC}
39 $\overline{PGM}$
38 NC
37 A_{15}
36 A_{14}
35 A_{13}
34 A_{12}
33 A_{11}
32 A_{10}
31 A_9
30 GND
29 A_8
28 A_7
27 A_6
26 A_5
25 A_4
24 A_3
23 A_2
22 A_1
21 A_0
27C2048
V_{CC}
$\overline{PGM}$
A_{16}
A_{15}
A_{14}
A_{13}
A_{12}
A_{11}
A_{10}
A_9
GND
A_8
A_7
A_6
A_5
A_4
A_3
A_2
A_1
A_0

TL/D/8806–2

Order Number NMC27C1024Q
See NS Package Number J40AQ

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C1024 pins.

NMC27C1024V
Plastic Chip Carrier


O13 6
O14 5
O15 4
$\overline{CE}$ 3
V_{PP} 2
NC 1
V_{CC} 44
$\overline{PGM}$ 43
NC 42
A15 41
A14 40
O12 7
O11 8
O10 9
O9 10
O8 11
GND 12
NC 13
O7 14
O6 15
O5 16
O4 17
44 pin PLCC
39 A13
38 A12
37 A11
36 A10
35 A9
34 GND
33 NC
32 A8
31 A7
30 A6
29 A5
18 O3
19 O2
20 O1
21 O0
22 $\overline{OE}$
23 NC
24 A0
25 A1
26 A2
27 A3
28 A4

TL/D/8806–11

Order Number NMC27C1024V
See NS Package Number V44A

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C1024Q12	120
NMC27C1024Q15	150
NMC27C1024Q17	170
NMC27C1024Q20	200
NMC27C1024Q25	250

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C1024Q120	120
NMC27C1024Q150	150
NMC27C1024Q170	170
NMC27C1024Q200	200
NMC27C1024Q250	250

Extended Temperature (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C1024QE150	150
NMC27C1024QE170	170
NMC27C1024QE200	200

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C1024QM170	170
NMC27C1024QM200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC}+1.0 to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V

Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD rating (MiL Spec 883C Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	
NMC27C1024Q12, 15, 17, 20, 25	+5V ±5%
NMC27C1024Q120, 150, 170, 200, 250	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		13	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	Q12, Q120		Q15, Q150		Q17, Q170		Q20, Q200		Q25, Q250		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		120		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		120		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$		50		60		75		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	$V_{CC}+1.0V$ to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C1024QE150, 170, 200	−40°C to +85°C
NMC27C1024QM170, 200	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		13	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	µA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 µA	$V_{CC} - 0.1$			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C1024Q						Units
			E150		E170, M170		E200, M200		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		170		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	12	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	13	20	pF

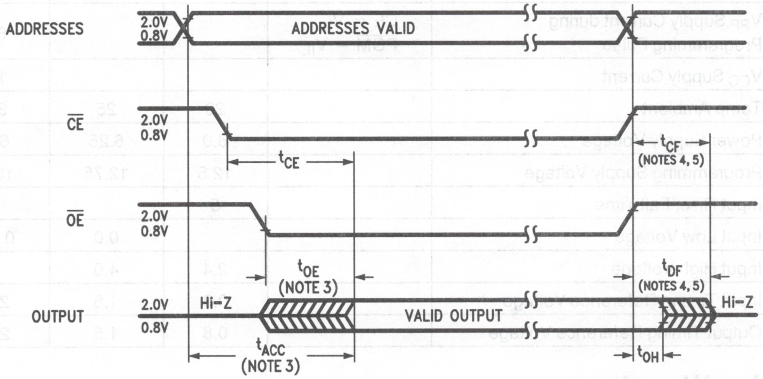
AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, & 9)



TL/D/8806-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V

Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} +1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 µA.
CL: 100 pF includes fixture capacitance.

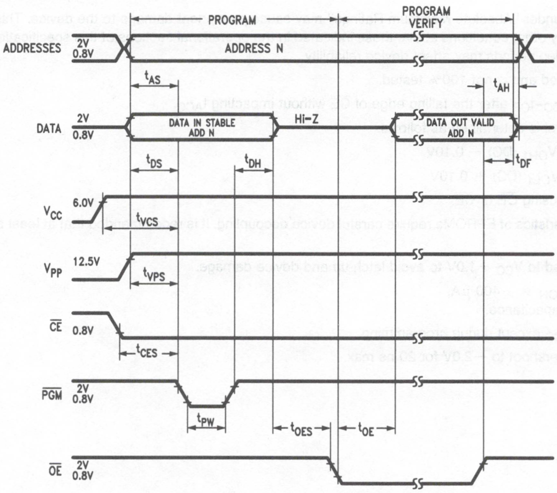
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		1			μs
t_{OES}	$\overline{OE}$ Set-Up Time		1			μs
t_{CES}	$\overline{CE}$ Set-Up Time		1			μs
t_{DS}	Data Set-Up Time		1			μs
t_{VPS}	V_{PP} Set-Up Time		1			μs
t_{VCS}	V_{CC} Set-Up Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid From $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			60	mA
I_{CC}	V_{CC} Supply Current				10	mA
t_R	Temp Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
T_{CR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)


PROGRAM
PROGRAM VERIFY
ADDRESSES
2V
0.8V
ADDRESS N
t_{AS}
t_{AH}
DATA
2V
0.8V
DATA IN STABLE ADD N
Hi-Z
DATA OUT VALID ADD N
t_{DS}
t_{DH}
t_{DF}
V_{CC}
6.0V
t_{VCS}
V_{PP}
12.5V
t_{VPS}
$\overline{CE}$
0.8V
t_{CES}
$\overline{PGM}$
2V
0.8V
t_{PW}
t_{OES}
t_{OE}
$\overline{OE}$
2V
0.8V

TL/D/8806-10

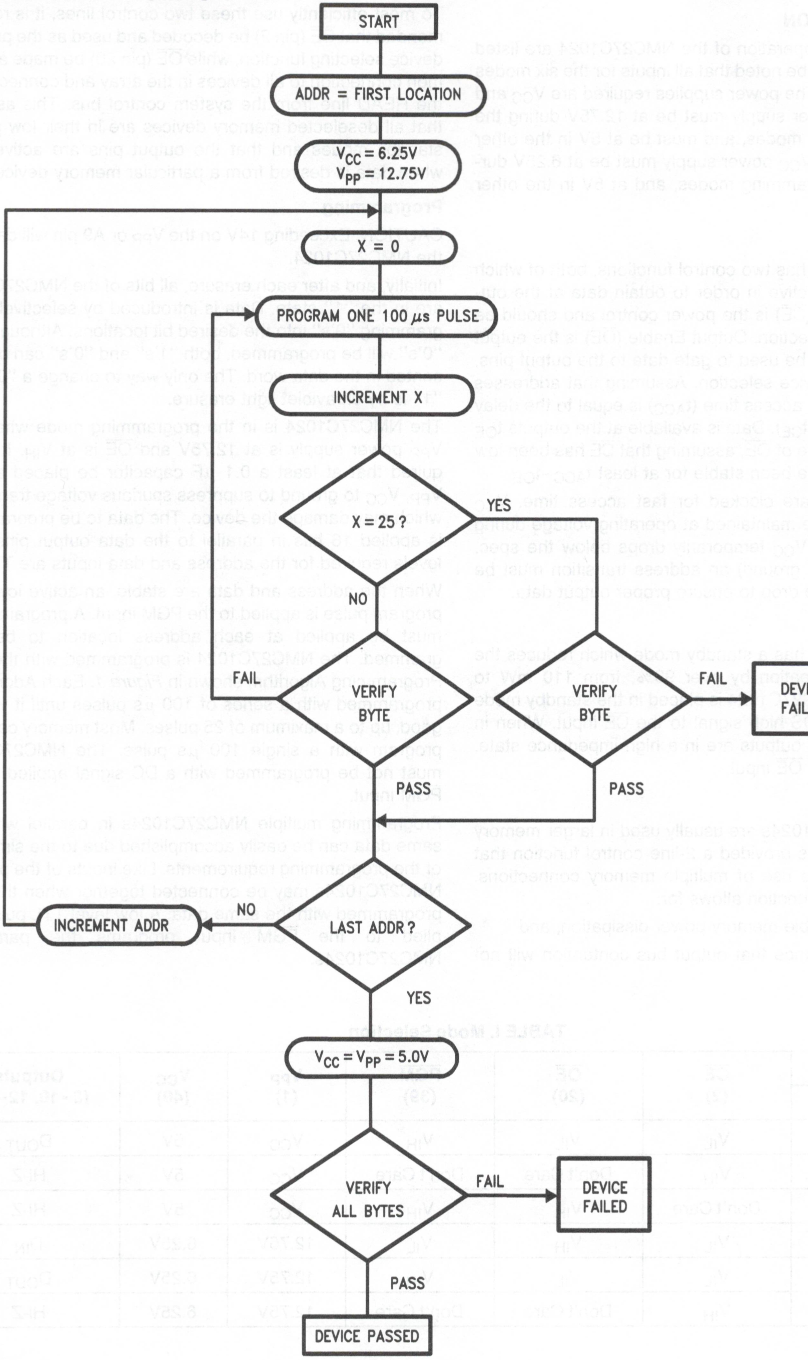
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Fast Program Algorithm, at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart


START
ADDR = FIRST LOCATION
V_{CC} = 6.25V
V_{PP} = 12.75V
X = 0
PROGRAM ONE 100 μs PULSE
INCREMENT X
X = 25 ?
YES
NO
FAIL
VERIFY BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
NO
INCREMENT ADDR
LAST ADDR ?
YES
V_{CC} = V_{PP} = 5.0V
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

TL/D/8806–5

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C1024 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C1024 has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C1024 is placed in the standby mode by applying a CMOS high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Output OR-Tying

Because NMC27C1024s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{\text{CE}}$ (pin 2) be decoded and used as the primary device selecting function, while $\overline{\text{OE}}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the NMC27C1024.

Initially, and after each erasure, all bits of the NMC27C1024 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C1024 is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{\text{OE}}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the PGM input. A program pulse must be applied at each address location to be programmed. The NMC27C1024 is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C1024 must not be programmed with a DC signal applied to the $\overline{\text{PGM}}$ input.

Programming multiple NMC27C1024s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel NMC27C1024s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{\text{PGM}}$ input programs the paralleled NMC27C1024s.

TABLE I. Mode Selection

Pins Mode	$\overline{\text{CE}}$ (2)	$\overline{\text{OE}}$ (20)	$\overline{\text{PGM}}$ (39)	V_{PP} (1)	V_{CC} (40)	Outputs (3–10, 12–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	V_{CC}	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C1024s in parallel with different data is also easily accomplished. Except for $\overline{\text{CE}}$, all like inputs (including $\overline{\text{OE}}$ and $\overline{\text{PGM}}$) of the parallel NMC27C1024 may be common. A TTL low level program pulse applied to an NMC27C1024 $\overline{\text{PGM}}$ input with CE at V_{IL} and V_{PP} at 12.5V will program that NMC27C1024. A TTL high level $\overline{\text{CE}}$ input inhibits the other NMC27C1024s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.5V. V_{PP} must be at V_{CC} except during programming and program verify.

Manufacturer's Identification Code

The NMC27C1024 has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for the NMC27C1024 is "8FD6", where "8F" designates that it is made by National Semiconductor, and "D6" designates a 1 Meg part.

The code is accessed by applying 12 ±0.5V to address pin A9. Addresses A1–A8, A10–A15, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C1024 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming opaque labels should be placed over the NMC27C1024 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C1024 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C1024 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C1024 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (21)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	1	0	1	1	0	D6

TABLE III. Minimum NMC27C1024 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

Section 2
EEPROMs

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NMC93CS06/CS46 256-Bit/1024-Bit Serial Electrically Erasable Programmable Memory 2-19
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National Semiconductor

EEPROM Selection Guide

Capacity	Organization	Part Number	Access Time (ns)	Cycle Time (ns)	Power Supply (V)	Power Dissipation		Packaging		Operating Temperature
						Active (mA)	Standby (μA)	DIP	SO	
CMOS EEPROM										
256-Bit	16 x 16 Serial	NMC93C06 NMC93CS06*	500	500	+5	2	50	8	14	
1024-Bit	64 x 16 Serial	NMC93C46 NMC93CS46*	500	500	+5	2	50	8	14	
2048-Bit	128 x 16 Serial	NMC93C56 NMC93CS56*	500	500	+5	2	50	8	14	
4096-Bit	256 x 16 Serial	NMC93C66 NMC93CS66*	500	500	+5	2	50	8	14	
NMOS EEPROM										
256-Bit	16 x 16	NMC9306	2	4	+5	10	3	8	14, 8	C, E, M
		NMC9307	2	4		10	3	8		
		NMC9313B	2	5		15	5	8		C
1024-Bit	64 x 16	NMC9346	2	4	+5	12	3	8	14, 8	C, E, M
		NMC9314B	2	5		17	5	8		C

*On chip write protection circuitry

Temperature Ranges
C = 0°C to +70°C
E = −40°C to +85°C
M = −55°C to +125°C

National
Semiconductor

NMC9306 256-Bit Serial Electrically Erasable Programmable Memory

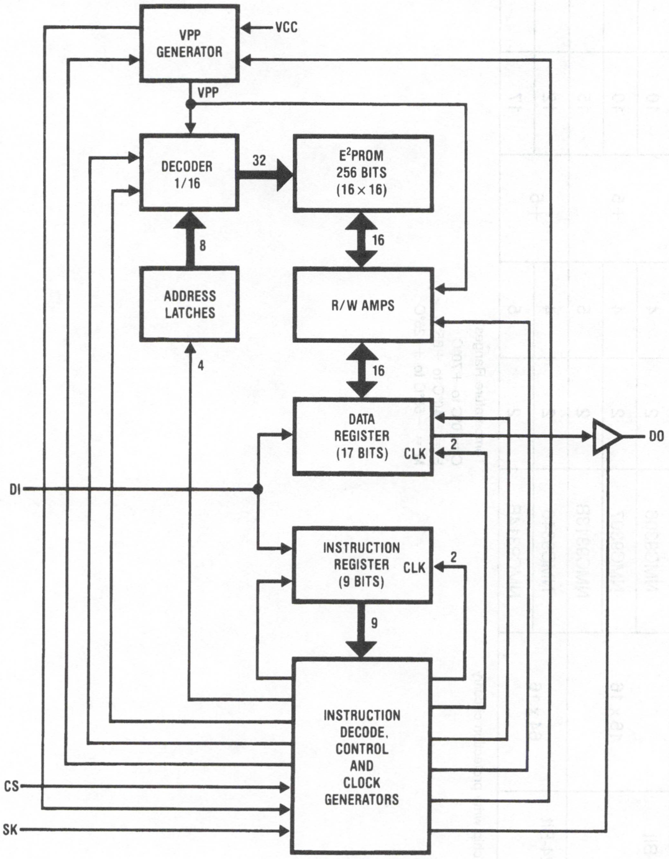
General Description

The NMC9306 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^{2}PROM technology. It is accessed via the simple MICROWIRE™ serial interface and is designed for data storage and/or timing applications. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306 has been designed to meet applications requiring up to 4×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16×16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Designed for 40,000 erase/write cycles

Block Diagram

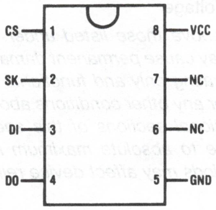

VPP GENERATOR
VCC
VPP
DECODER 1/16
32
E²PROM 256 BITS (16 × 16)
8
16
ADDRESS LATCHES
R/W AMPS
4
16
DATA REGISTER (17 BITS)
CLK
2
DO
DI
INSTRUCTION REGISTER (9 BITS)
CLK
2
9
INSTRUCTION DECODE, CONTROL AND CLOCK GENERATORS
CS
SK

TL/D/5029-1

Pin Names	
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

Connection Diagram

Dual-In-Line Package (N)

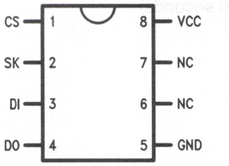

CS
1
8
VCC
SK
2
7
NC
DI
3
6
NC
DO
4
5
GND

TL/D/5029-10

Top View

See NS Package Number N08E

8-Pin
SO Package (M8)


CS
1
8
VCC
SK
2
7
NC
DI
3
6
NC
DO
4
5
GND

TL/D/5029-11

Top View

See NS Package Number M08A

Ordering Information

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ± 10%

Order Number	Device Marking
NMC9306N	NMC9306N
NMC9306M8	9306

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ± 10%

Order Number	Device Marking
NMC9306EN	NMC9306EN
NMC9306EM8	9306E

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Storage Temperature	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC9306/COP494	0°C to +70°C
NMC9306E	−40°C to +85°C
Positive Supply Voltage	4.5V to 5.5V

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Parameter	Part Number	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})	NMC9306, NMC9306E		4.5		5.5	V
Operating Current (I_{CC1})	NMC9306	V_{CC} = 5.5V, CS = 1			10	mA
	NMC9306E	V_{CC} = 5.5V, CS = 1			12	mA
Standby Current (I_{CC2})	NMC9306	V_{CC} = 5.5V, CS = 0			3	mA
	NMC9306E	V_{CC} = 5.5V, CS = 0			4	mA
Input Voltage Levels V_{IL} V_{IH}	 NMC9306		 −0.1 2.0		 0.8 V_{CC} + 1	 V V
V_{IL} V_{IH}	NMC9306E		−0.1 2.0		0.8 V_{CC} + 1	V V
Output Voltage Levels V_{OL} V_{OH}	NMC9306, NMC9306E	 I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4		 0.4	 V V
Input Leakage Current	NMC9306, NMC9306E	V_{IN} = 5.5V			10	μA
Output Leakage Current	NMC9306, NMC9306E	V_{OUT} = 5.5V, CS = 0			10	μA
SK Frequency SK HIGH TIME t_{SKH} (Note 2) SK LOW TIME t_{SKL} (Note 2)	NMC9306		0 1 1		250	kHz μs μs
SK Frequency SK HIGH TIME t_{SKH} (Note 2) SK LOW TIME t_{SKL} (Note 2)	NMC9306E		0 1 1		 250	kHz μs μs
Input Set-up and Hold Times CS t_{CSS} t_{CSH} DI t_{DIS} t_{DIH}	NMC9306, NMC9306E		 0.2 0 0.4 0.4			 μs μs μs μs
Output Delay DO t_{PD1} t_{PD0}	NMC9306, NMC9306E	C_L = 100 pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V			 2 2	 μs μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)	NMC9306, NMC9306E		10		30	ms
CS Low Time (t_{CS}) (Note 3)	NMC9306, NMC9306E		1			μs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. e.g. if t_{SKL} = 1 μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Functional Description

The NMC9306 is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 10-bit instructions can be executed. The instruction format has a logical 0 as a start bit, followed by a logical 1, four bits as an op code, and four bits of address. An SK clock cycle is necessary after CS equals logical 0 followed by a logical 1 before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming enable instruction (EWEN) is needed to keep the part in the enable state if the power supply (V_{CC}) noise falls below operating range. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1's) before the register can be written (certain bits set to 0's). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1's. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to $V_{IH,}$ the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

Instruction Set

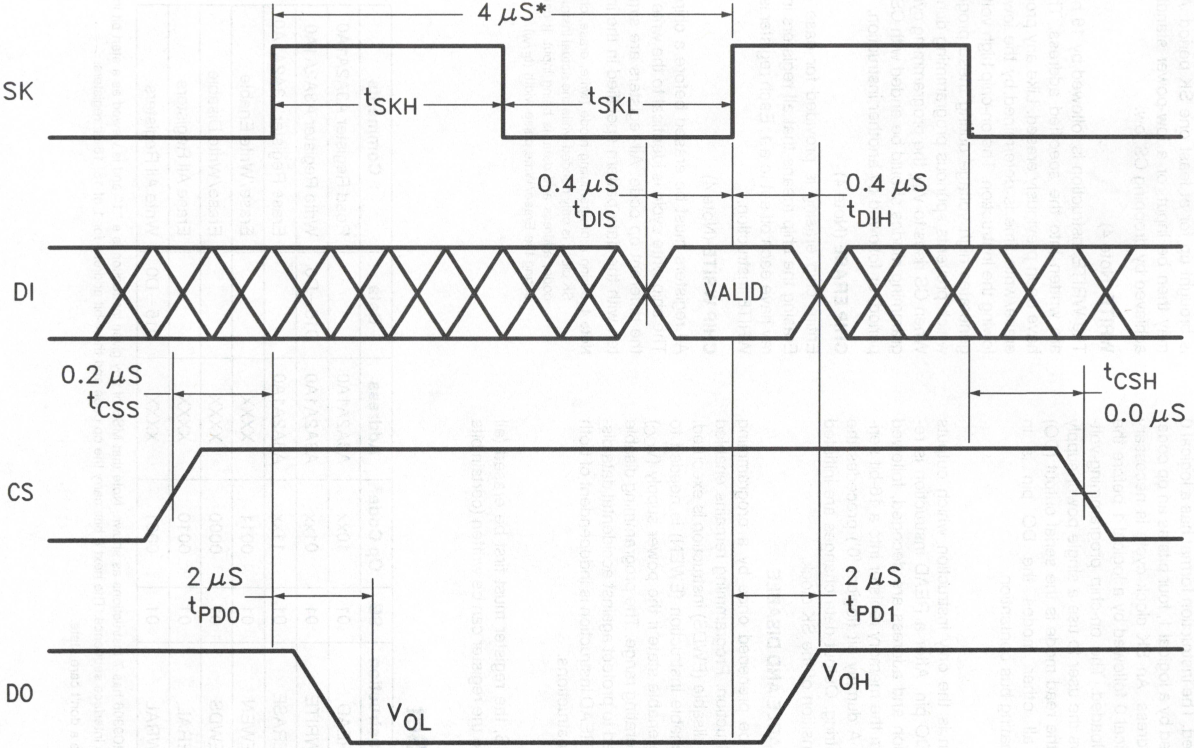
Instruction	SB	Op Code	Address	Data	Comments
READ	01	10xx	A3A2A1A0		Read Register A3A2A1A0
WRITE	01	01xx	A3A2A1A0	D15–D0	Write Register A3A2A1A0
ERASE	01	11xx	A3A2A1A0		Erase Register A3A2A1A0
EWEN	01	0011	XXXX		Erase/Write Enable
EWDS	01	0000	XXXX		Erase/Write Disable
ERAL	01	0010	XXXX		Erase All Registers
WRAL	01	0001	XXXX	D15–D0	Write All Registers

NMC9306 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

Timing Diagrams

Synchronous Data Timing

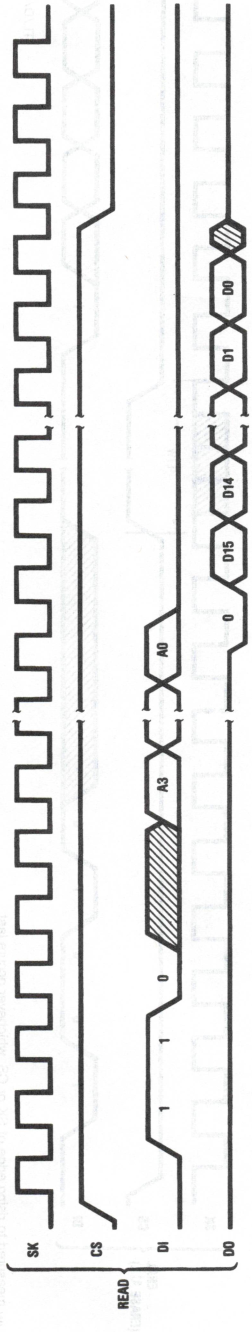

SK
DI
CS
DO
4 μS*
tSKH
tSKL
0.4 μS
tDIS
0.4 μS
tDIH
VALID
0.2 μS
tCSS
tCSH
0.0 μS
2 μS
tPD0
2 μS
tPD1
VOL
VOH

TL/D/5029–13

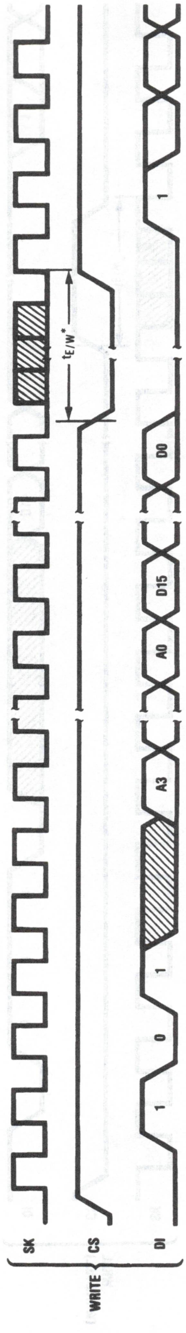
*This is the minimum SK period and is 5μ for NMC9306M

Timing Diagrams (Continued)

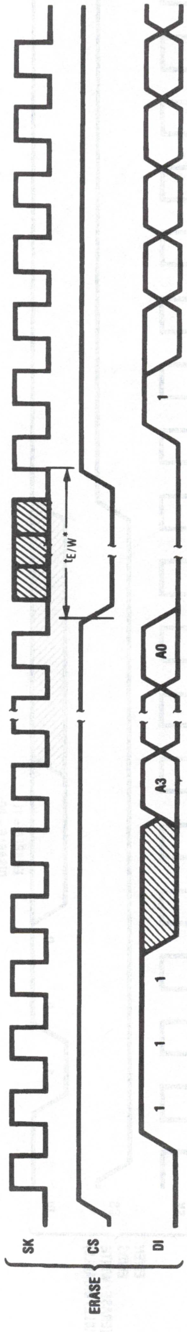
Instruction Timing


READ
SK
CS
DI
DO
1
1
0
A3
A0
0
D15
D14
D1
D0

TL/D/5029-14


WRITE
SK
CS
DI
1
0
1
A3
A0
D15
D0
$t_{E/W}$*
1

TL/D/5029-15

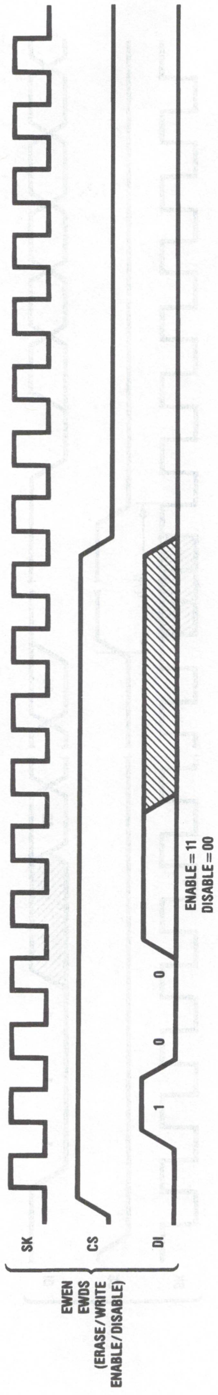

ERASE
SK
CS
DI
1
1
1
A3
A0
$t_{E/W}$*
1

TL/D/5029-16

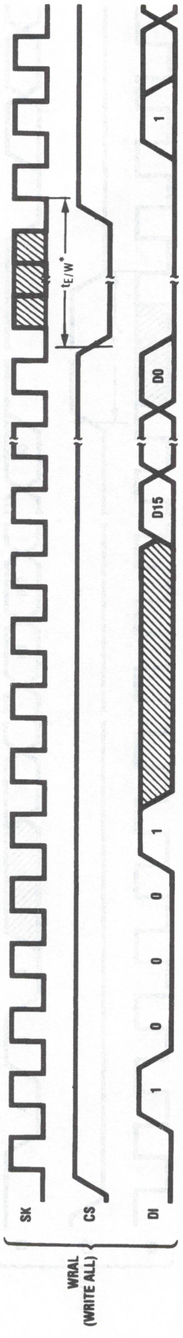
*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Timing Diagrams (Continued)

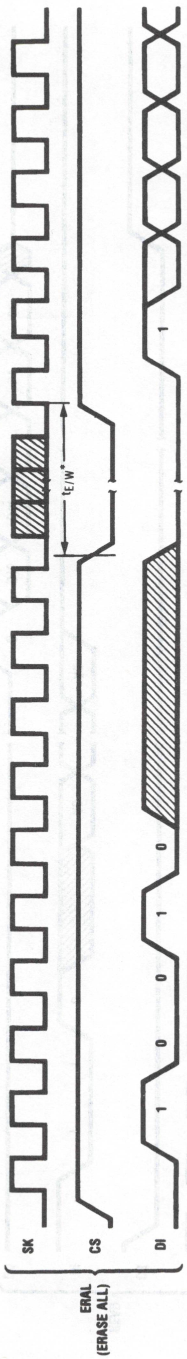
Instruction Timing (Continued)


SK
CS
DI
1
0
0
ENABLE = 11
DISABLE = 00
EWEN
EWDS
(ERASE/WRITE
ENABLE/DISABLE)

TL/D/5029-17


SK
CS
DI
1
0
0
0
1
D15
D0
1
$t_{E/W}$*
WRAL
(WRITE ALL)

TL/D/5029-18


SK
CS
DI
1
0
0
1
0
1
$t_{E/W}$*
ERAL
(ERASE ALL)

TL/D/5029-19

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

National Semiconductor

NMC93C06/C46 256-Bit/1024-Bit Serial Electrically Erasable Programmable Memory

General Description

The NMC93C06/NMC93C46 are 256/1024 bits of CMOS electrically erasable memory divided into 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high speed and low power. They operate from a single 5V supply since V_{PP} is generated on-board. The serial organization allows the NMC93C06/NMC93C46 to be packaged in an 8-pin DIP or 8-pin SO package to save board space.

The memories feature a serial interface with the instruction, address, and write data, input on the Data-In (DI) pin. All read data and device status is output on the Data-Out (DO) pin. A low-to-high transition of shift clock (SK) shifts all data in and out. This serial interface is MICROWIRE™ compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, Erase/Write Disable. The NMC93C06/NMC93C46 do not require an erase cycle prior to the Write and Write All instructions. The Erase and Erase All instructions are available to maintain complete read and programming compatibility with the NMOS NMC9346. All programming cycles are completely self-timed for simplified operation. The busy status is available on the DO pin to indicate the completion of a programming cycle. EEPROMs are shipped in the erased state where all bits are logical 1's.

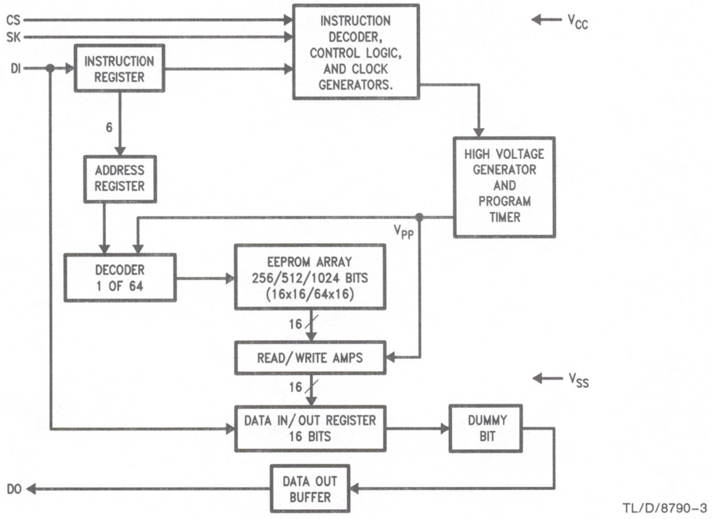
Compatibility with Other Devices

These memories are pin compatible to National Semiconductor's NMOS EEPROMs, NMC9306 and NMC9346. The NMC93C06/NMC93C46 are both pin and function compatible with the NMC93C56 2048-bit EEPROM and the NMC93C66 4096-bit EEPROM with the one exception that both of these larger devices require two additional address bits.

Features

- Typical active current 400 μA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 5V only operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Over 40 years data retention
- Designed for 100,000 write cycles

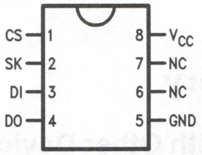
Block Diagram


CS
SK
DI
INSTRUCTION REGISTER
INSTRUCTION DECODER, CONTROL LOGIC, AND CLOCK GENERATORS.
V_{CC}
6
ADDRESS REGISTER
HIGH VOLTAGE GENERATOR AND PROGRAM TIMER
V_{PP}
DECODER 1 OF 64
EEPROM ARRAY 256/512/1024 BITS (16x16/64x16)
16
READ/WRITE AMPS
16
V_{SS}
DATA IN/OUT REGISTER 16 BITS
DUMMY BIT
DO
DATA OUT BUFFER

TL/D/8790-3

Connection Diagrams

Dual-In-Line Package (N)



TL/D/8790-1

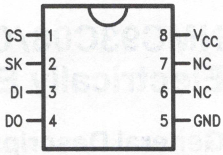
Top View

See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

SO Package (M8)



TL/D/8790-2

Top View

See NS Package Number M08A

Ordering Information

Commercial Temp. Range (0°C to +70°C)
V_{CC} = 5V ±10%

Order Number
NMC93C06N/NMC93C46N NMC93C06M8/NMC93C46M8

Extended Temp. Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Order Number
NMC93C06EN/NMC93C46EN NMC93C06EM8/NMC93C46EM8

Military Temp. Range (−55°C to +125°C)

Order Number
NMC93C06MN/NMC93C46MN NMC93C06MM8/NMC93C46MM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC93C06/46	0°C to +70°C
NMC93C06/46E	−40°C to +85°C
NMC93C06/46M	−55°C to +125°C
Positive Supply Voltage	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93C06/46	CS = V_{IH}, SK = 1 MHz		2	mA
		NMC93C06/46E	SK = 0.5 MHz		2	
		NMC93C06/46M*	SK = 0.5 MHz		2	
I_{CC2}	Operating Current TTL Input Levels	NMC93C06/46	CS = V_{IH}, SK = 1 MHz		3	mA
		NMC93C06/46E	SK = 0.5 MHz		3	
		NMC93C06/46M	SK = 0.5 MHz		4	
I_{CC3}	Standby Current	NMC93C06/46	CS = 0V		50	µA
		NMC93C06/46E			100	
		NMC93C06/46M			100	
I_{IL}	Input Leakage	NMC93C06/46	V_{IN} = 0V to V_{CC}	−2.5	2.5	µA
		NMC93C06/46E		−10	10	
		NMC93C06/46M		−10	10	
I_{OL}	Output Leakage	NMC93C06/46	V_{OUT} = 0V to V_{CC}	−2.5	2.5	µA
		NMC93C06/46E		−10	10	
		NMC93C06/46M		−10	10	
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} + 1	
V_{OL1}	Output Low Voltage	NMC93C06/46	I_{OL} = 2.1 mA		0.4	V
		NMC93C06/46E	I_{OL} = 2.1 mA		0.4	
		NMC93C06/46M	I_{OL} = 1.8 mA		0.4	
V_{OH1}	Output High Voltage		I_{OH} = −400 µA	2.4		
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = −10 µA	V_{CC} − 0.2		
f_{SK}	SK Clock Frequency	NMC93C06/46		0	1	MHz
		NMC93C06/46E		0	0.5	
		NMC93C06/46M		0	0.5	
t_{SKH}	SK High Time	NMC93C06/46	(Note 2)	250		ns
		NMC93C06/46E	(Note 3)	500		
		NMC93C06/46M	(Note 3)	500		
t_{SKL}	SK Low Time	NMC93C06/46	(Note 2)	250		ns
		NMC93C06/46E	(Note 3)	500		
		NMC93C06/46M	(Note 3)	500		
t_{CS}	Minimum CS Low Time	NMC93C06/46	(Note 4)	250		ns
		NMC93C06/46E	(Note 5)	500		
		NMC93C06/46M	(Note 5)	500		
t_{CSS}	CS Setup Time	NMC93C06/46	Relative to SK	50		ns
		NMC93C06/46E		100		
		NMC93C06/46M		100		

***Note:** Thruout this table "M" refers to temperature range (−55°C to +125°C), not package.

DC and AC Electrical Characteristics V_{CC} = 5V ±10% (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NMC93C06/46 NMC93C06/46E NMC93C06/46M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93C06/46 NMC93C06/46E NMC93C06/46M	Relative to SK	100 200 200		ns
t_{PD1}	Output Delay to "1"	NMC93C06/46 NMC93C06/46E NMC93C06/46M	AC Test		500 1000 1000	ns
t_{PD0}	Output Delay to "0"	NMC93C06/46 NMC93C06/46E NMC93C06/46M	AC Test		500 1000 1000	ns
t_{SV}	CS to Status Valid	NMC93C06/46 NMC93C06/46E NMC93C06/46M	AC Test		500 1000 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93C06/46 NMC93C06/46E NMC93C06/46M	CS = V_{IL} AC Test	100 200 200		ns
t_{WP}	Write Cycle Time				10	ms

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 µs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 µs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 µs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 µs. For example, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 µs in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Capacitance (Note 6)

T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

The NMC93C06/NMC93C46 has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for selection of 1 of 16 or 64 16-bit registers.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical "0") precedes the 16-bit data output string. Output data changes are initiated by a low-to-high transition of the SK clock.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it "powers up" in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE)

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is clocked in on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL)

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. The Erase All cycle is identical to the ERASE cycle except for the different op-code.

As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write All (WRAL):

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 50 ns (t_{CS}).

Erase/Write Disable (EWDS):

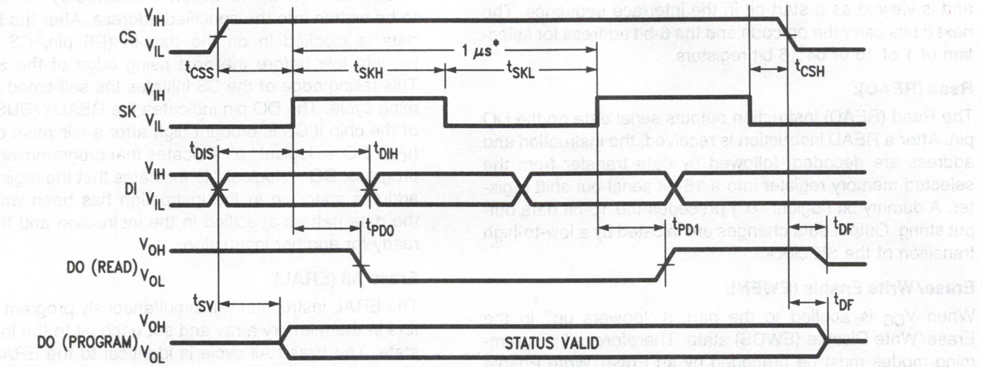
To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Instruction Set for the NMC93C06/46

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erase all registers.
WRAL	1	00	01XXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXX		Disables all programming instructions.

Timing Diagrams

Synchronous Data Timing

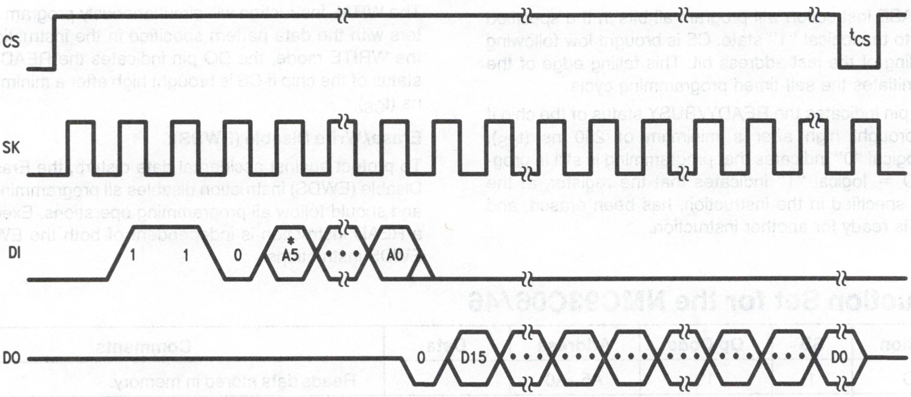

CS
V_{IH}
V_{IL}
t_{CSS}
t_{SKH}
1 μs*
t_{SKL}
t_{CSH}
SK
V_{IH}
V_{IL}
t_{DIS}
t_{DIH}
DI
V_{IH}
V_{IL}
t_{PD0}
t_{PD1}
t_{DF}
DO (READ)
V_{OH}
V_{OL}
t_{SV}
t_{DF}
DO (PROGRAM)
V_{OH}
V_{OL}
STATUS VALID

*This is the minimum SK period (Note 2).

TL/D/8790-4

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 μs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

READ:

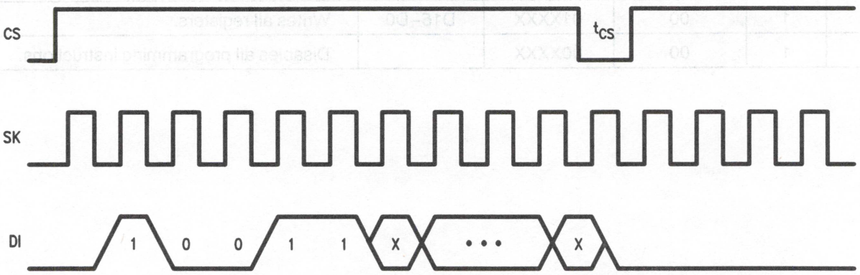

CS
t_{CS}
SK
DI
1
1
0
*
A5
• • •
A0
DO
0
D15
• • •
• • •
• • •
• • •
• • •
D0

TL/D/8790-5

*Address bits A5 and A4 become "don't care" for NMC93C06.

WEN:

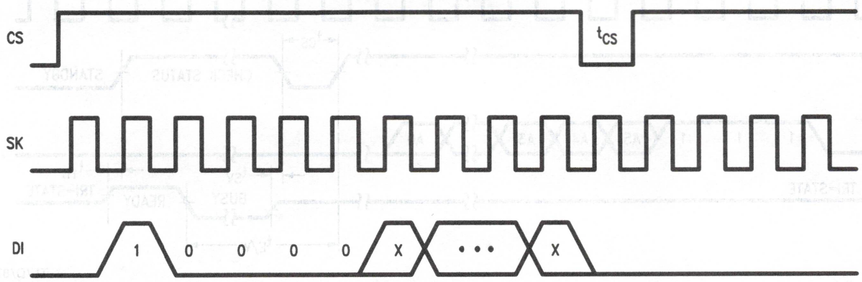
DO = TRI-STATE


CS
t_{CS}
SK
DI
1
0
0
1
1
X
• • •
X

TL/D/8790-6

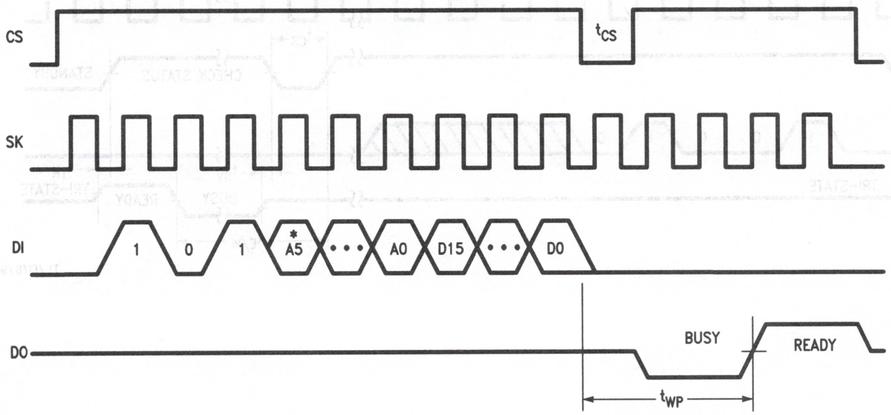
Timing Diagrams (Continued)

EWDS:
DO = TRI-STATE


CS
t_{CS}
SK
DI
1
0
0
0
0
X
• • •
X

TL/D/8790-7

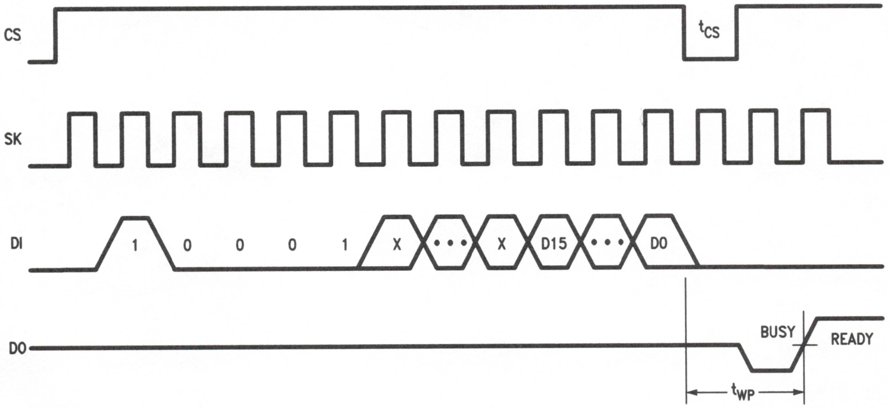
WRITE:


CS
t_{CS}
SK
DI
1
0
1
*
A5
• • •
A0
D15
• • •
D0
DO
BUSY
READY
t_{WP}

TL/D/8790-8

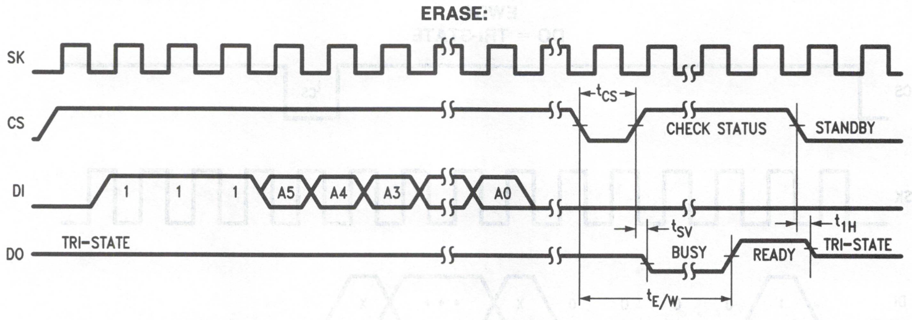
*Address bits A5 and A4 become "don't care" for NMC93C06.

WRAL:

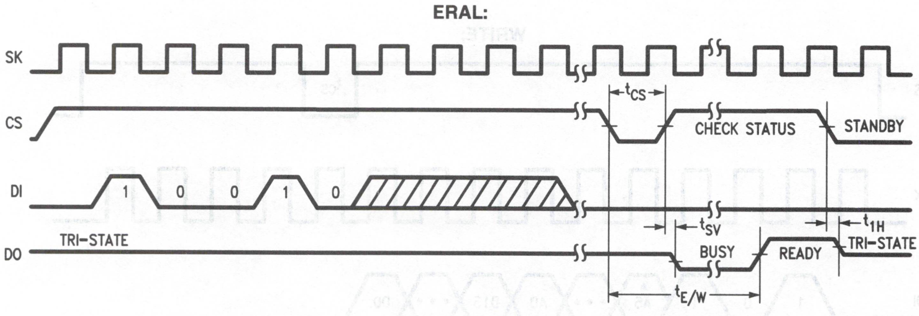

CS
t_{CS}
SK
DI
1
0
0
0
1
X
• • •
X
D15
• • •
D0
DO
BUSY
READY
t_{WP}

TL/D/8790-9

Timing Diagrams (Continued)


ERASE:
SK
CS
DI
DO
1
1
1
A5
A4
A3
A0
TRI-STATE
t_{CS}
CHECK STATUS
STANDBY
t_{SV}
t_{1H}
BUSY
READY
TRI-STATE
$t_{E/W}$

TL/D/8790–10


ERAL:
SK
CS
DI
DO
1
0
0
1
0
TRI-STATE
t_{CS}
CHECK STATUS
STANDBY
t_{SV}
t_{1H}
BUSY
READY
TRI-STATE
$t_{E/W}$

TL/D/8790–11

National Semiconductor

NMC93CS06/CS46 256-Bit/1024-Bit Serial Electrically Erasable Programmable Memories

General Description

The NMC93CS06/NMC93CS46 are 256/1024 bits of read/write memory divided into 16/64 registers of 16 bits each. N registers (N ≤ 16 or N ≤ 64) can be protected against data modification by programming into a special on-chip register called the memory protect register the address of the first register to be protected. This address can be locked into the device, so that these registers can be permanently protected. Thereafter, all attempts to alter data in a register whose address is equal to or greater than the address stored in the protect register will be aborted.

The read instruction loads the address of the first register to be read into a 6-bit address pointer. Then the data is clocked out serially on the D0 pin and automatically cycles to the next register to produce a serial data stream. In this way the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 256/1024 bits. Thus, the NMC93CS06/NMC93CS46 can be viewed as a non-volatile shift register.

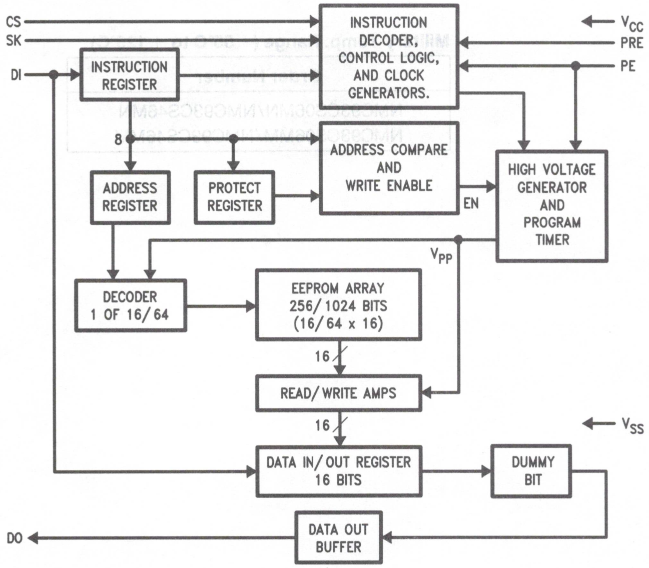
The write cycle is completely self-timed. No separate erase cycle is required before write. The write cycle is only enabled when pin 6 (program enable) is held high. If the address of the register to be written is less than the address in the protect register then the data is written 16 bits at a time into one of the 16/64 data registers. If CS is brought high following the initiation of a write cycle the D0 pin indicates the ready/busy status of the chip.

National Semiconductor's EEPROMs are designed and tested for applications requiring extended endurance. Refer to device operation for further endurance information. Data retention is specified to be greater than 40 years.

Features

- Write protection in user defined section of memory
- Typical active current 400 μA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 5 volt only operation in all modes
- Microwire compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential register read
- Over 40 years data retention
- Designed for 100,000 write cycles

Block Diagram

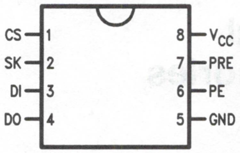

CS
SK
DI
INSTRUCTION REGISTER
INSTRUCTION DECODER, CONTROL LOGIC, AND CLOCK GENERATORS.
V_{CC}
PRE
PE
8
ADDRESS REGISTER
PROTECT REGISTER
ADDRESS COMPARE AND WRITE ENABLE
EN
HIGH VOLTAGE GENERATOR AND PROGRAM TIMER
V_{PP}
DECODER 1 OF 16/64
EEPROM ARRAY 256/1024 BITS (16/64 x 16)
16
READ/WRITE AMPS
16
V_{SS}
DATA IN/OUT REGISTER 16 BITS
DUMMY BIT
DO
DATA OUT BUFFER

TL/D/9208-3

Connection Diagrams

PIN OUT:

Dual-In-Line Package (N)


CS 1
SK 2
DI 3
DO 4
8 V$_{CC}$
7 PRE
6 PE
5 GND

TL/D/9208–1

Top View

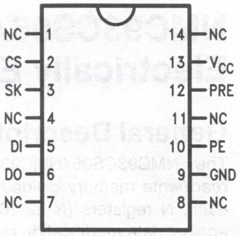
See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

PIN OUT:

SO Package (M)


NC 1
CS 2
SK 3
NC 4
DI 5
DO 6
NC 7
14 NC
13 V$_{CC}$
12 PRE
11 NC
10 PE
9 GND
8 NC

TL/D/9208–2

Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

$V_{CC} = 5V \pm 10\%$

Order Number
NMC93CS06N/NMC93CS46N
NMC93CS06M/NMC93CS46M

Extended Temp. Range (−40°C to +85°C)

$V_{CC} = 5V \pm 10\%$

Order Number
NMC93CS06EN/NMC93CS46EN
NMC93CS06EM/NMC93CS46EM

Military Temp. Range (−55°C to +125°C)

Order Number
NMC93CS06MN/NMC93CS46MN
NMC93CS06MM/NMC93CS46MM

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC93CS06/NMC93CS46	0°C to +70°C
NMC93CS06E/NMC93CS46E	−40°C to +85°C
NMC93CS06M/NMC93CS46M (Mil. Temp.)	−55°C to +125°C
Positive Power Supply	4.5V to 5.5V

DC and AC Electrical Characteristics

V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M*	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	CS = 0V		50 100 100	µA
I_{IL}	Input Leakage	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	µA
I_{OL}	Output Leakage	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	V_{OUT} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	I_{OL} = 2.1 mA I_{OL} = 2.1 mA I_{OL} = 1.8 mA		0.4 0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 µA	2.4		
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = −10 µA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M		0 0 0	1 0.5 0.5	MHz
t_{SKH}	SK High Time	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{SKL}	SK Low Time	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{CS}	Minimum CS Low Time	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	(Note 4) (Note 5) (Note 5)	250 500 500		ns
t_{CSS}	CS Setup Time	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	Relative to SK	50 100 100		ns
t_{PRES}	PRE Setup Time	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	Relative to SK	50 100 100		ns

*Throughout this table "M" refers to temperature range (−55°C to +125°C), not package.

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PES}	PE Setup Time	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	Relative to SK	50 100 100		ns
t_{DIS}	DI Setup Time	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	Relative to CS Relative to CS Relative to CS	250 500 500		ns
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	Relative to SK	100 200 200		ns
t_{PD1}	Output Delay to "1"	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	AC Test		500 1000 1000	ns
t_{PD0}	Output Delay to "0"	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	AC Test		500 1000 1000	ns
t_{SV}	CS to Status Valid	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	AC Test		500 1000 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93CS06/NMC93CS46 NMC93CS06E/NMC93CS46E NMC93CS06M/NMC93CS46M	CS = V_{IL} AC Test		100 200 200	ns
t_{WP}	Write Cycle Time				10	ms

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 microsecond. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Capacitance (Note 6)

T_A = 25°C, f = 1MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

The NMC93CS06 and NMC93CS46 have 10 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8-bits carry the op code and the 6-bit address for selection of 1 of 16 or 64 16-bit registers.

Read (READ):

The Read (READ) instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the NONVOLATILE SHIFT-REGISTER mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). D0 = logical 0 indicates that programming is still in progress. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction. Following the PRREAD instruction the 6-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Instruction Set for the NMC93CS06 and NMC93CS46

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses $\geq$ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Functional Description (Continued)

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

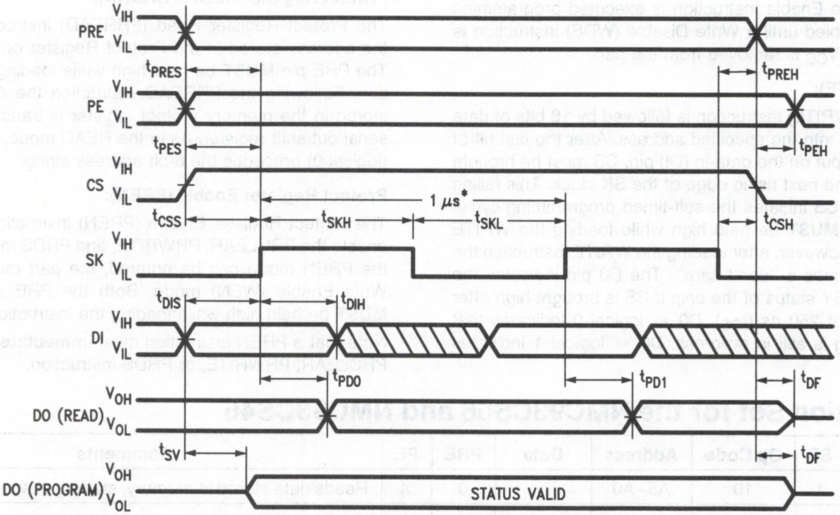
Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one** time only instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Timing Diagrams

Synchronous Data Timing

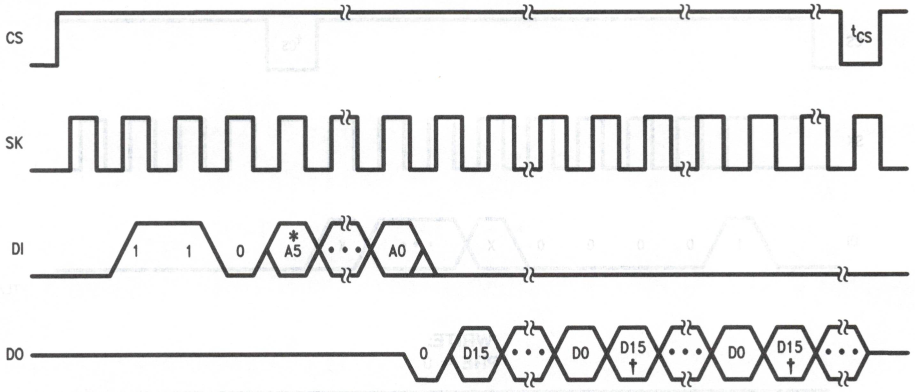


TL/D/9208-4

*This is the minimum SK period (See Note 2).

Timing Diagrams (Continued)

READ:
PRE = 0, PE = X

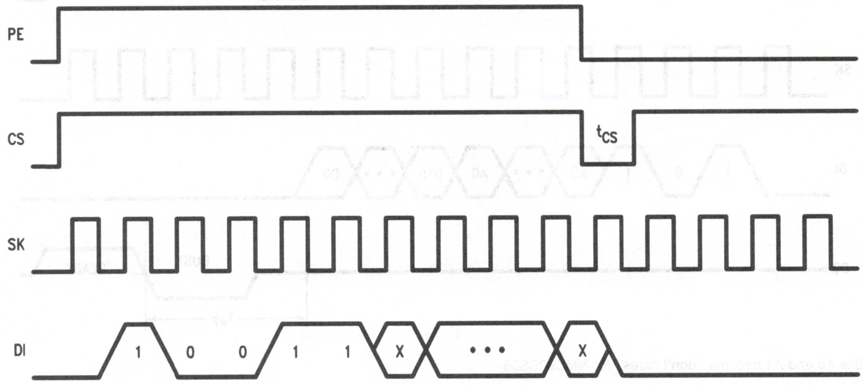

CS
t_{CS}
SK
DI
1
1
0
*
A5
• • •
A0
DO
0
D15
• • •
D0
D15
†
• • •
D0
D15
†
• • •

*Address bits A5 and A4 become "don't cares" for NMC93CS06

†The memory automatically cycles to the next register.

TL/D/9208–5

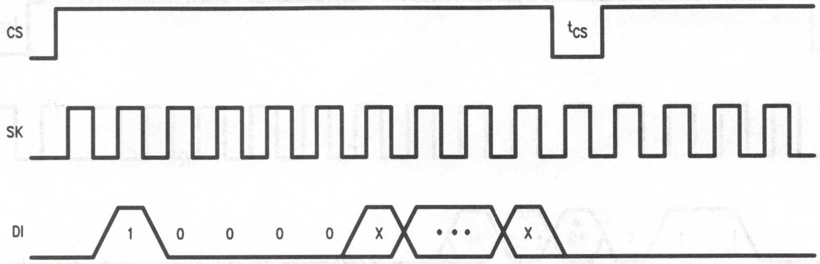
WEN:
PRE = 0, D0 = TRI-STATE


PE
CS
t_{CS}
SK
DI
1
0
0
1
1
X
• • •
X

TL/D/9208–6

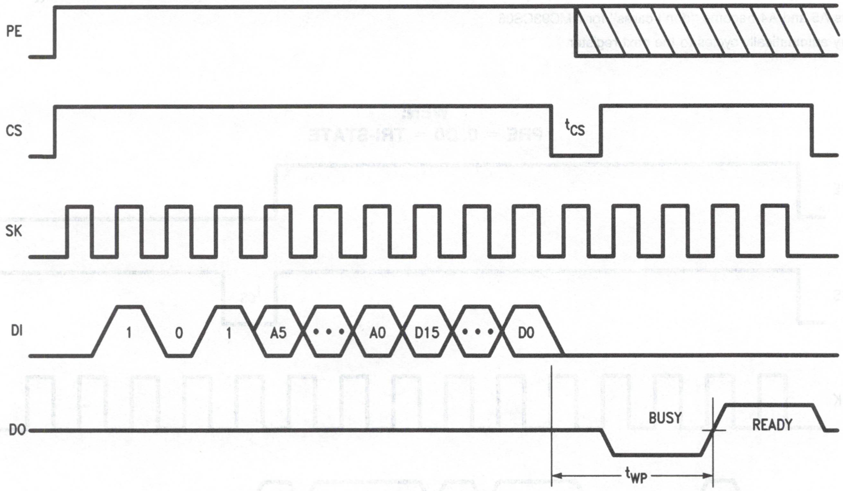
Timing Diagrams (Continued)

WDS:
PRE = 0, PE = X, DO = TRI-STATE


CS
t_{CS}
SK
DI
1
0
0
0
0
X
• • •
X

TL/D/9208-7

WRITE:
PRE = 0

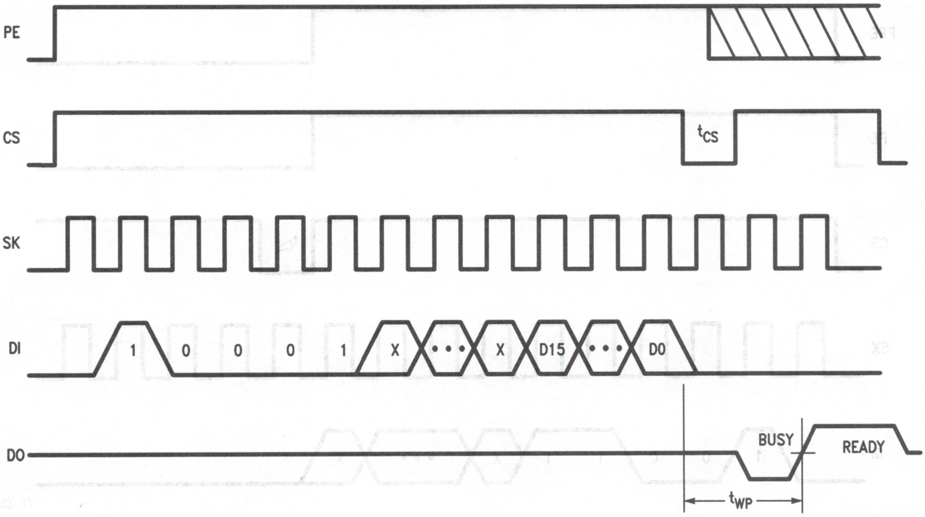

PE
CS
t_{CS}
SK
DI
1
0
1
A5
• • •
A0
D15
• • •
D0
DO
BUSY
READY
t_{WP}

TL/D/9208-8

- Address bits A5 and A4 become "don't cares" for NMC93CS06

Timing Diagrams (Continued)

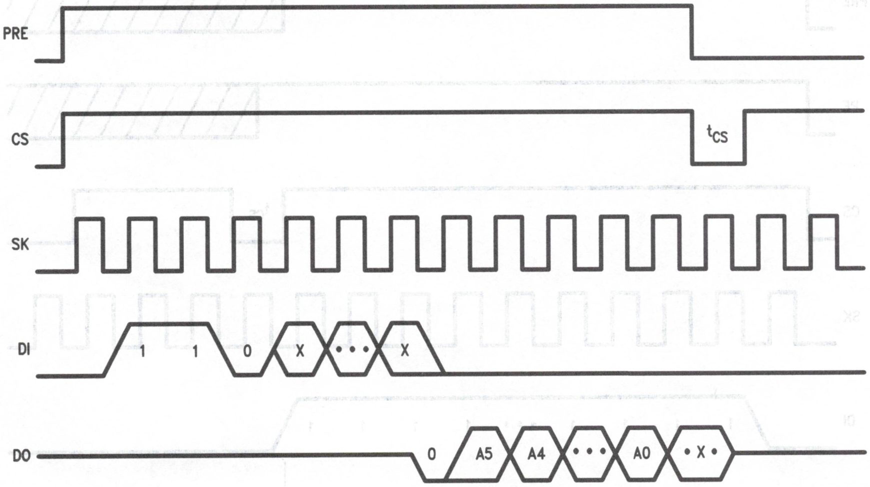
WRALL*:
PRE = 0


PE
CS
t_{CS}
SK
DI
1
0
0
0
1
X
• • •
X
D15
• • •
D0
DO
BUSY
READY
t_{WP}

*Protect Register **MUST** be cleared.

TL/D/9208-9

PRREAD:
PE = X

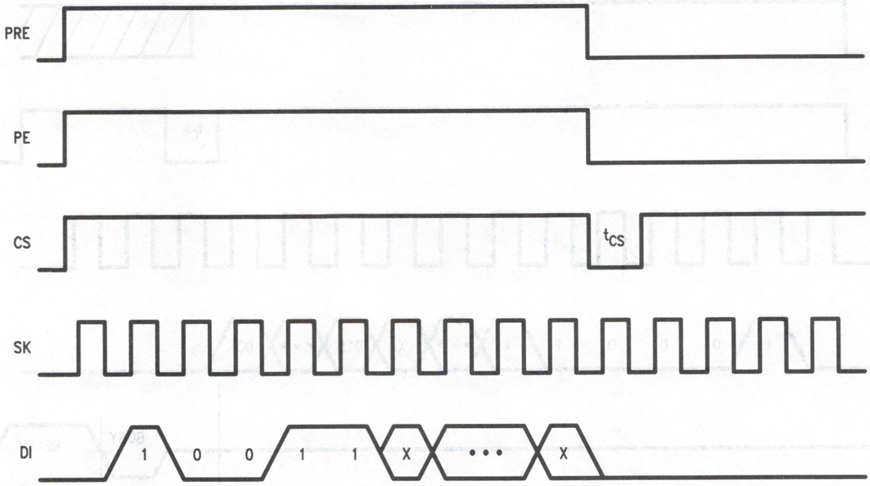

PRE
CS
t_{CS}
SK
DI
1
1
0
X
• • •
X
DO
0
A5
A4
• • •
A0
• X •

TL/D/9208-10

•Address bits A5 and A4 become "don't cares" for NMC93CS06

Timing Diagrams (Continued)

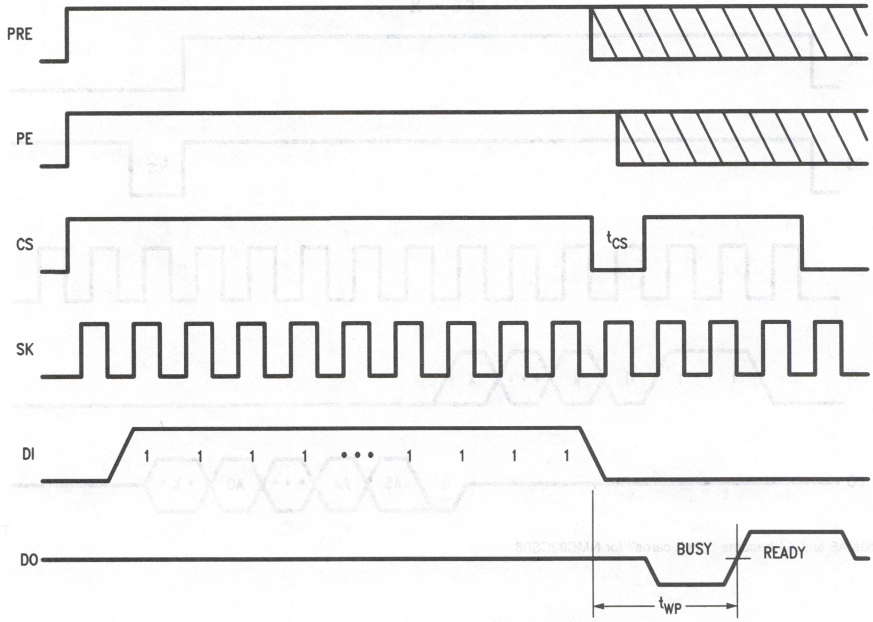
PREN*:
D0 = TRI-STATE


PRE
PE
CS
tCS
SK
DI
1
0
0
1
1
X
• • •
X

TL/D/9208–11

*A WEN cycle must precede a PREN cycle.

PRCLEAR*:

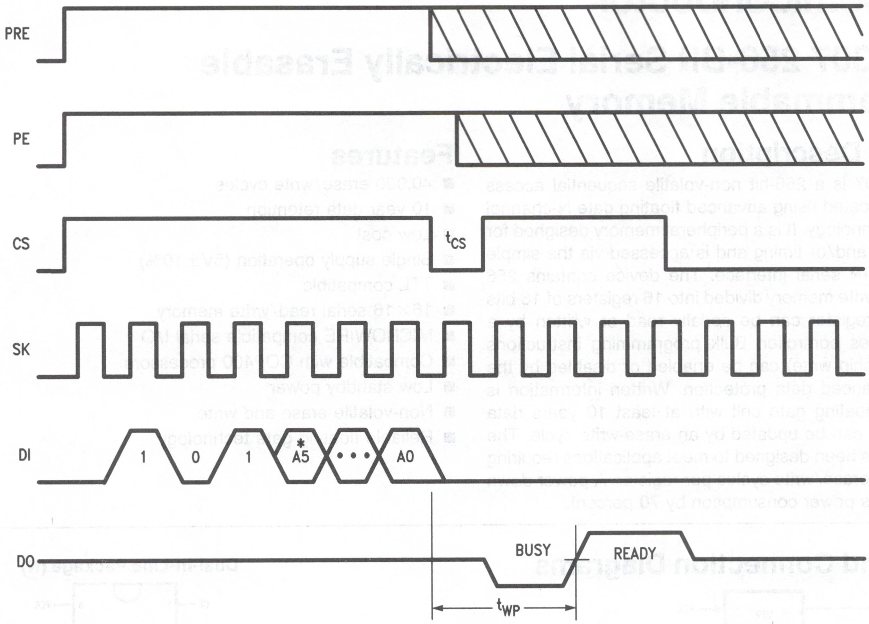

PRE
PE
CS
tCS
SK
DI
1
1
1
1
• • •
1
1
1
1
DO
BUSY
READY
tWP

*A PREN cycle must **immediately** precede a PRCLEAR cycle.

TL/D/9208–12

Timing Diagrams (Continued)

PRWRITE†:

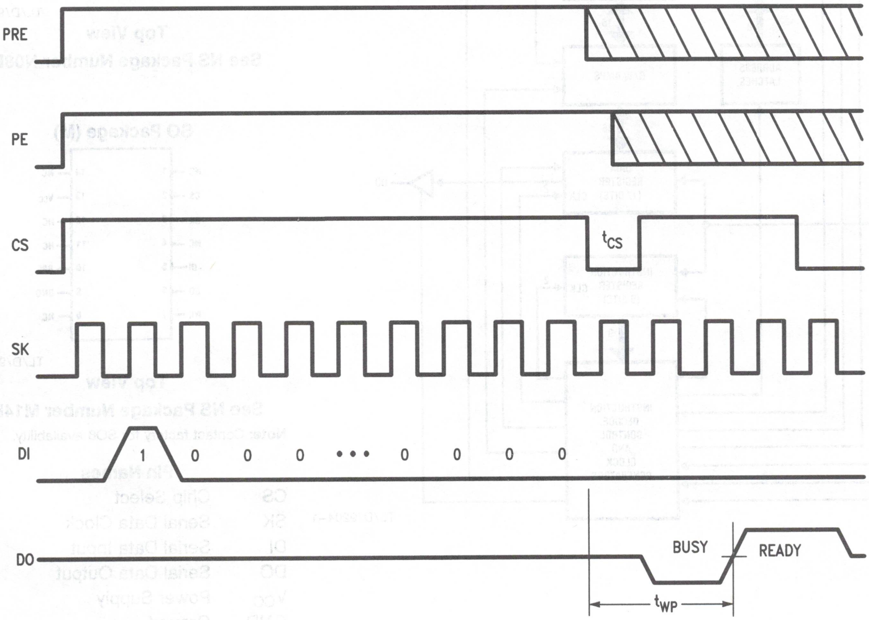

PRE
PE
CS
t_{CS}
SK
DI
1
0
1
*
A5
• • •
A0
DO
BUSY
READY
t_{WP}

TL/D/9208–13

*Address bits A5 and A4 become "don't cares" for NMC93CS06

†Protect Register **MUST** be cleared before a PRWRITE cycle. A PREN cycle must **immediately** precede a PRWRITE cycle.

PRDS*:


PRE
PE
CS
t_{CS}
SK
DI
1
0
0
0
• • •
0
0
0
0
DO
BUSY
READY
t_{WP}

TL/D/9208–14

***ONE TIME ONLY** instruction. A PREN cycle must **immediately** precede a PRDS cycle.

National Semiconductor

NMC9307 256-Bit Serial Electrically Erasable Programmable Memory

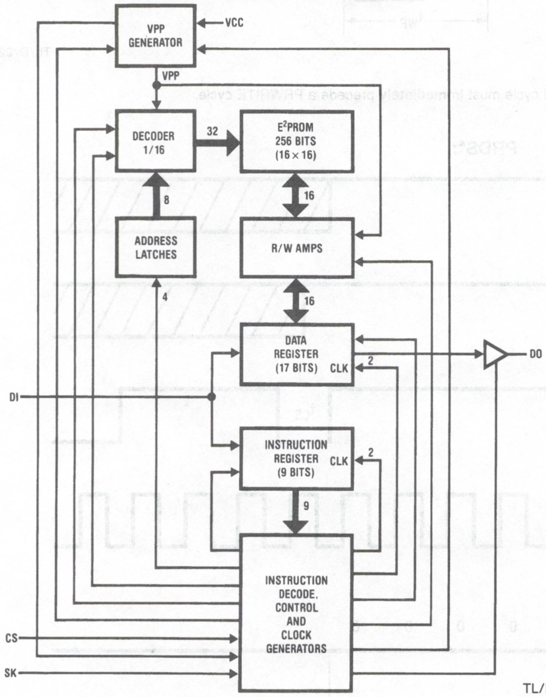
General Description

The NMC9307 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E²PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Bulk programming instructions (chip erase, chip write) can be enabled or disabled by the user for enhanced data protection. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9307 has been designed to meet applications requiring up to 40,000 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

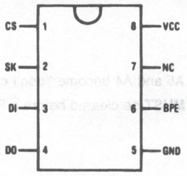
- 40,000 erase/write cycles
- 10 year data retention
- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16 × 16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams


VPP GENERATOR
VCC
VPP
DECODER 1/16
32
E²PROM 256 BITS (16 × 16)
8
16
ADDRESS LATCHES
R/W AMPS
4
16
DATA REGISTER (17 BITS)
CLK
2
DO
DI
INSTRUCTION REGISTER (9 BITS)
CLK
2
9
INSTRUCTION DECODE, CONTROL AND CLOCK GENERATORS
CS
SK

TL/D/9204-1

Dual-In-Line Package (N)

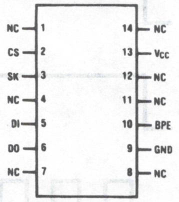

CS 1
SK 2
DI 3
DO 4
8 VCC
7 NC
6 BPE
5 GND

TL/D/9204-2

Top View

See NS Package Number N08E

SO Package (M)


NC 1
CS 2
SK 3
NC 4
DI 5
DO 6
NC 7
14 NC
13 Vcc
12 NC
11 NC
10 BPE
9 GND
8 NC

TL/D/9204-3

Top View

See NS Package Number M14B

Note: Contact factory for SO8 availability.

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage Relative to GND +6V to −0.3V

Ambient Operating Temperature

NMC9307 0°C to +70°C

NMC9307E −40°C to +85°C

Ambient Storage Temperature −65°C to +125°C

Lead Temperature (Soldering, 10 sec.) 300°C

ESD Rating 2000V

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics

Parameter	Conditions	Part No	Min	Max	Units
Operating Voltage (V_{CC})			4.5	5.5	V
Operating Current (I_{CC1})	$V_{CC}=5.5V$, CS=1	9307		10	mA
		9307E		12	
Standby Current (I_{CC2})	$V_{CC}=5.5V$, CS=0	9307		3	mA
		9307E		4	
Input Voltage Levels					
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	$V_{CC}+1$	V
Output Voltage Levels					
V_{OL}	$I_{OL}=2.1$ mA			0.4	V
V_{OH}	$I_{OH}=-400$ µA		2.4		V
Input Leakage Current	$V_{IN}=5.5V$			10	µA
Input Leakage Current	$V_{IN}=0$ to 5.5V				
PINS 1, 2, 3				±10	µA
PIN 6				±50	µA
Output Leakage Current	$V_{OUT}=5.5V$, CS=0			10	µA
SK Frequency			0	250	kHz
SK HIGH TIME t_{SKH} (Note 2)			1		µs
SK LOW TIME t_{SKL} (Note 2)			1		µs
Input Set-Up and Hold Times					
CS t_{CSS}			0.2		µs
t_{CSH}			0		µs
DI t_{DIS}			0.4		µs
t_{DIH}			0.4		µs
Output Delay	CL=100 pF				
DO t_{PD1}	$V_{OL}=0.8V$, $V_{OH}=2.0V$			2	µs
t_{PD0}	$V_{IL}=0.45V$, $V_{IH}=2.40V$			2	µs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)			10	30	ms
CS Low Time (t_{CS}) (Note 3)			1		µs
Endurance	Number of Data Changes per Bit		40, 000 Typical		

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 µs, therefore in an SK clock cycle, $t_{SKH} + t_{SKL}$ must be greater than or equal to 4 µs. e.g. if $t_{SKL} = 1$µs then the minimum $t_{SKH} = 3$ µs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 µs (t_{CS}) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	0, 1	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	0, 1	01xx	A3A2A1A0	D15–D0	Write register A3A2A1A0
ERASE	0, 1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	0, 1	0011	xxxx		Erase/write enable
EWDS	0, 1	0000	xxxx		Erase/write disable
ERAL	0, 1	0010	xxxx		Erase all registers
WRAL	0, 1	0001	xxxx	D15–D0	Write all registers

The NMC9307 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

Functional Description

The NMC9307 is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. The NMC9307 is organized as sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical "1" before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction. The chip erase (ERAL) instruction is ignored if the BPE pin is at V_{IL}, i.e., data is not changed.

CHIP WRITE (Note 4)

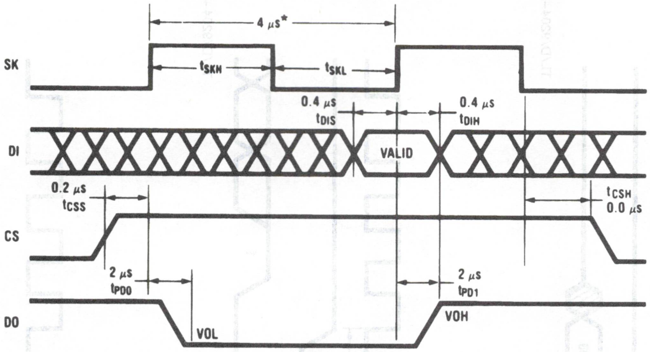
All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

The chip write (WRAL) instruction is ignored if the BPE pin is at V_{IL}, i.e., the array data is not changed.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

Timing Diagrams

Synchronous Data Timing

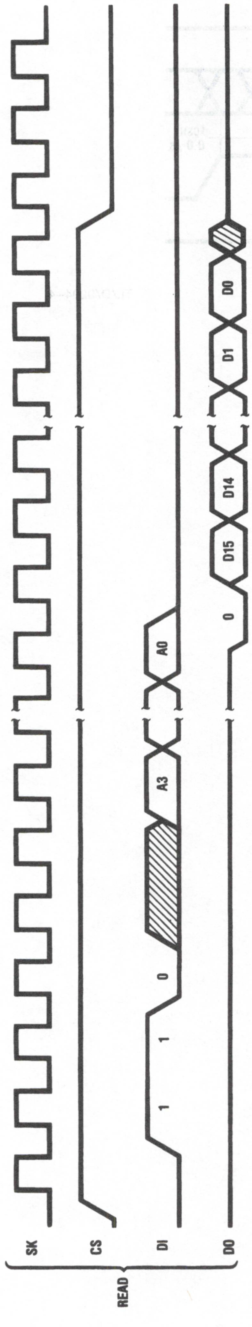

4 µs*
SK
tSKH
tSKL
0.4 µs
tDIS
0.4 µs
tDIH
DI
VALID
0.2 µs
tCSS
tCSH
0.0 µs
CS
2 µs
tPD0
2 µs
tPD1
DO
VOL
VOH

TL/D/9204-4

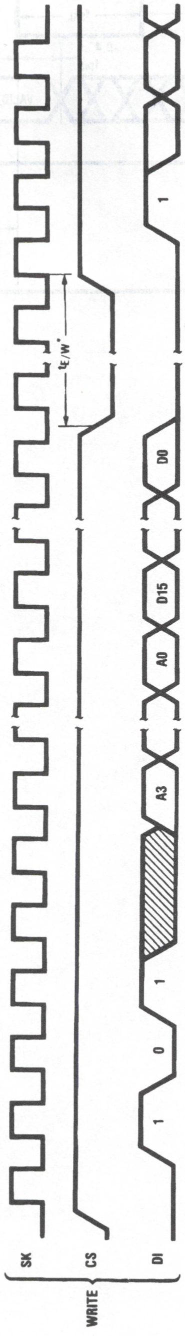
*This is the minimum SK period

Timing Diagrams (Continued)

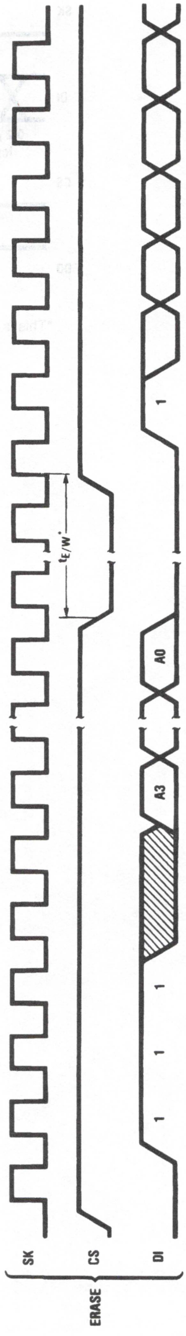
Instruction Timing


READ
SK
CS
DI
DO
1
1
0
A3
A0
0
D15
D14
D1
D0

TL/D/9204–5


WRITE
SK
CS
DI
1
0
1
A3
A0
D15
D0
1
$t_{E/W}$*

TL/D/9204–6

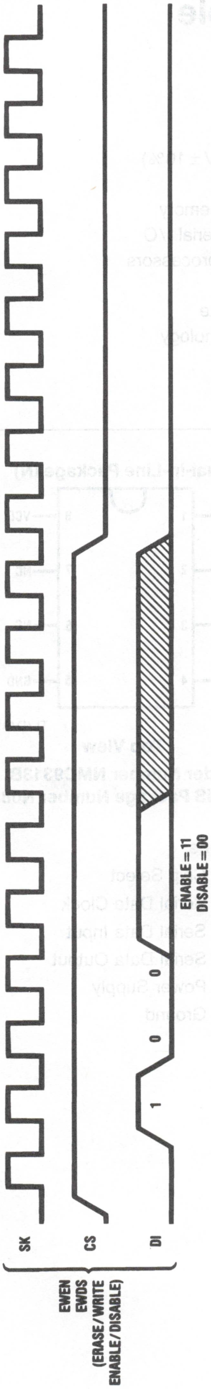

ERASE
SK
CS
DI
1
1
1
A3
A0
1
$t_{E/W}$*

TL/D/9204–7

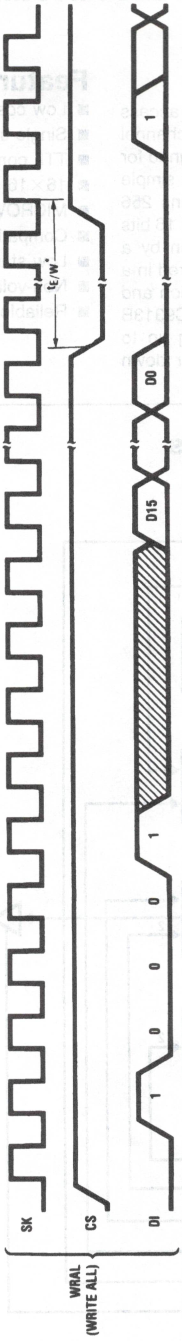
*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Timing Diagrams (Continued)

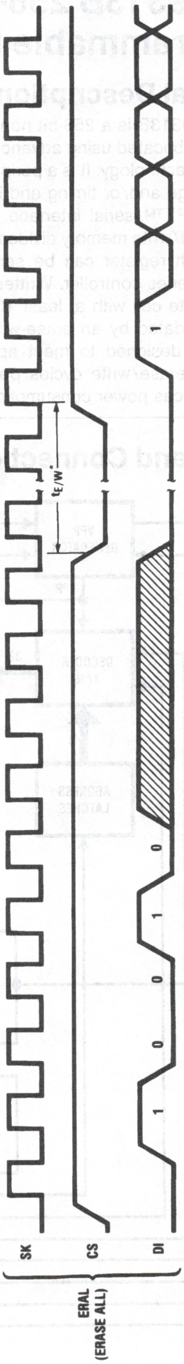
Instruction Timing (Continued)


SK
CS
DI
1
0
0
ENABLE=11
DISABLE=00
EWEN
EWDS
(ERASE/WRITE
ENABLE/DISABLE)

TL/D/9204-8


SK
CS
DI
1
0
0
0
1
D15
D0
1
t_E/W*
WRAL
(WRITE ALL)

TL/D/9204-9


SK
CS
DI
1
0
0
1
0
t_E/W*
ERAL
(ERASE ALL)

TL/D/9204-10

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

National Semiconductor

NMC9313B 256-Bit Serial Electrically Erasable Programmable Memory

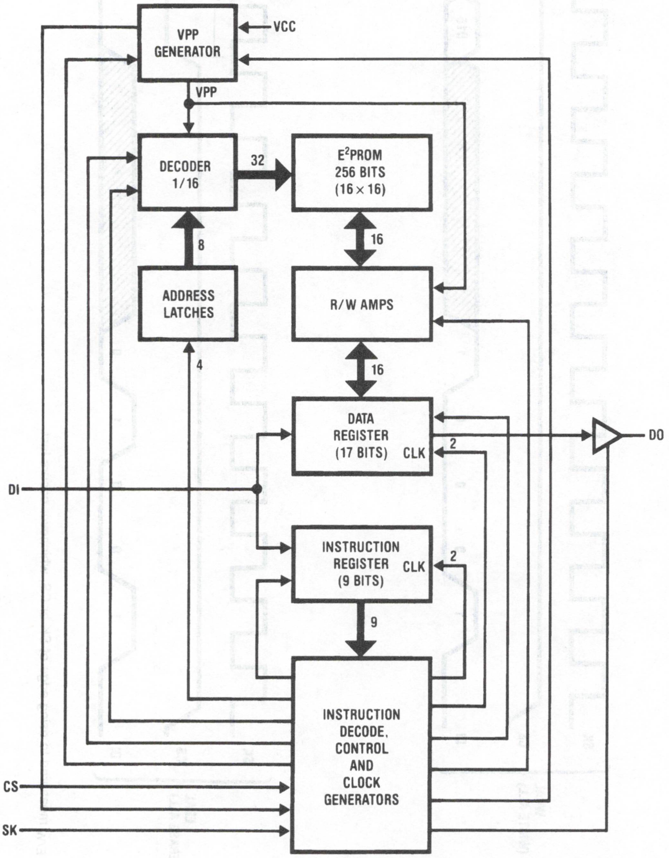
General Description

The NMC9313B is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^{2}PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9313B has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 67 percent.

Features

- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16×16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

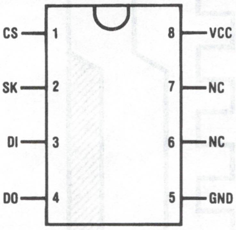
Block and Connection Diagrams



VPP GENERATOR
VCC
VPP
DECODER 1/16
32
E²PROM 256 BITS (16×16)
8
16
ADDRESS LATCHES
R/W AMPS
4
16
DATA REGISTER (17 BITS) CLK
2
DO
DI
INSTRUCTION REGISTER (9 BITS) CLK
2
9
INSTRUCTION DECODE, CONTROL AND CLOCK GENERATORS
CS
SK

TL/D/9145–1

Dual-In-Line Package (N)



CS
1
SK
2
DI
3
DO
4
8
VCC
7
NC
6
NC
5
GND

TL/D/9145–2

Top View

Order Number NMC9313B

See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature NMC9313B/COP494	0°C to +70°C
Ambient Storage Temperature with Data Retention	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	2000V

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics $0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})		4.5		5.5	V
Operating Current (I_{CC1})	$V_{CC} = 5.5V$, CS = 1			15	mA
Standby Current (I_{CC2})	$V_{CC} = 5.5V$, CS = 0			5	mA
Input Voltage Levels					
V_{IL}		−0.1		0.8	V
V_{IH}		2.0		$V_{CC} + 0.5$	V
Output Voltage Levels					
V_{OL}	$I_{OL} = 2.1$ mA			0.4	V
V_{OH}	$I_{OH} = -400\ \mu A$	2.4			V
Input Leakage Current	$V_{IN} = 5.5V$			10	µA
Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0			10	µA
SK Frequency		0		200	kHz
SK HIGH TIME t_{SKH} (Note 2)		3			µs
SK LOW TIME t_{SKL} (Note 2)		2			µs
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			µs
t_{CSH}		0			µs
DI t_{DIS}		0.4			µs
t_{DIH}		0.4			µs
Output Delay	CL = 100 pF				
DO t_{PD1}	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$			2	µs
t_{PD0}	$V_{IL} = 0.45V$, $V_{IH} = 2.40V$			2	µs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)		10		30	ms
CS Low Time (t_{CS}) (Note 3)		1			µs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 5 µs, therefore in an SK clock cycle, $t_{SKH} + t_{SKL}$ must be greater than or equal to 5 µs. e.g. if $t_{SKL} = 2$ µs then the minimum $t_{SKH} = 3$ µs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 µs (t_{CS}) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	01	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	01	01xx	A3A2A1A0	D15–D0	Write register A3A2A1A0
ERASE	01	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	01	0011	xxxx		Erase/write enable
EWDS	01	0000	xxxx		Erase/write disable
ERAL	01	0010	xxxx		Erase all registers
WRAL	01	0001	xxxx	D15–D0	Write all registers

NMC9313B has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

Functional Description

The NMC9313B is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 10-bit instructions can be executed. The instruction format has a logical 0, 1 as start bits, four bits as an op code, and four bits of address. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

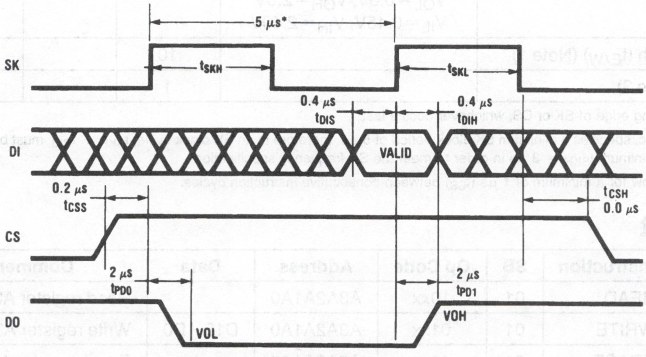
Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

Timing Diagrams

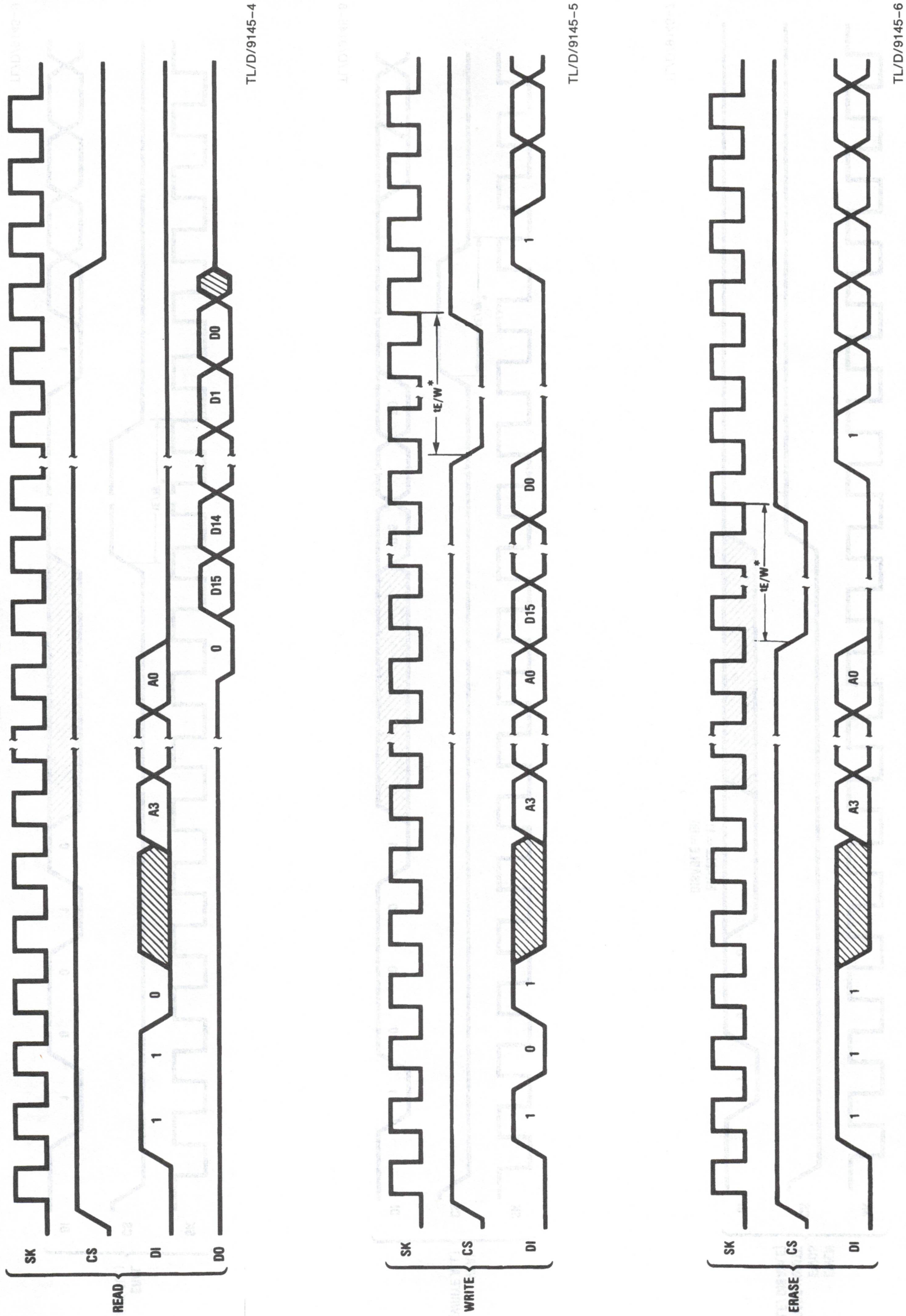


*This is the minimum SK period

TL/D/9145-3

Synchronous Data Timing

Timing Diagrams (Continued)


READ
SK
CS
DI
DO
1
1
0
A3
A0
0
D15
D14
D1
D0
WRITE
SK
CS
DI
1
0
1
A3
A0
D15
D0
1
tE/W*
ERASE
SK
CS
DI
1
1
1
A3
A0
1
tE/W*

TL/D/9145–4

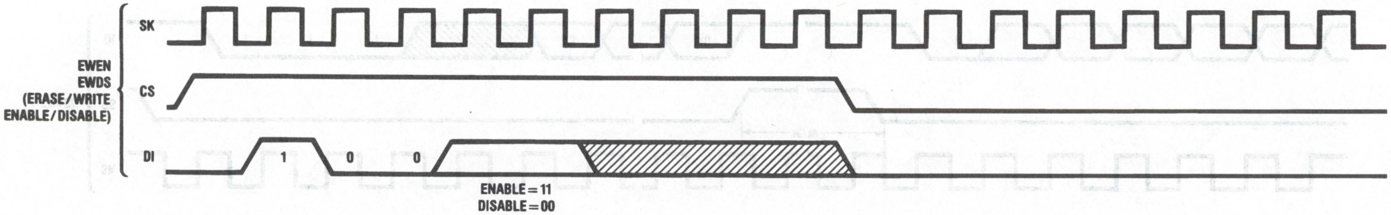
TL/D/9145–5

TL/D/9145–6

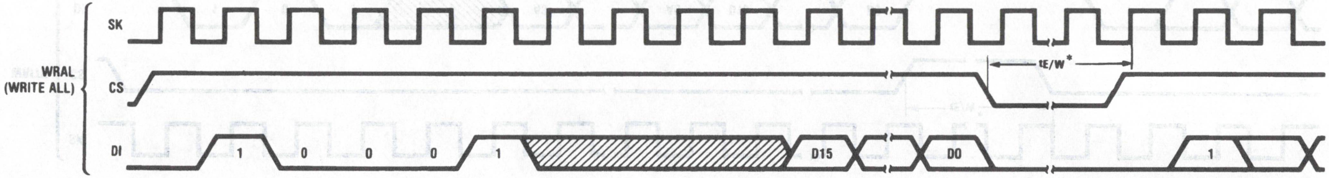
Instruction Timing

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

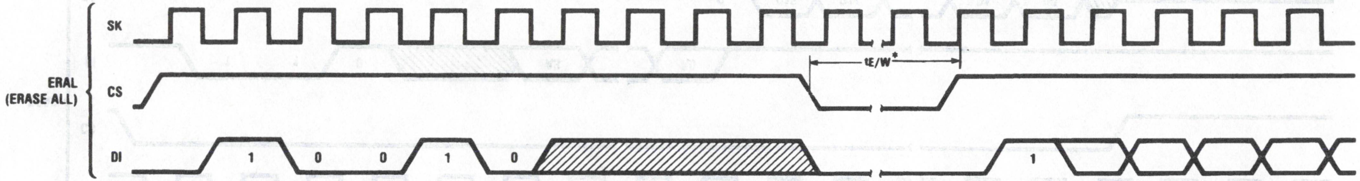
Timing Diagrams (Continued)


EWEN
EWDS
(ERASE/WRITE
ENABLE/DISABLE)
SK
CS
DI
1
0
0
ENABLE = 11
DISABLE = 00

TL/D/9145–7


WRAL
(WRITE ALL)
SK
CS
DI
1
0
0
0
1
D15
D0
1
tE/W*

TL/D/9145–8


ERAL
(ERASE ALL)
SK
CS
DI
1
0
0
1
0
1
tE/W*

TL/D/9145–9

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Timing (Continued)

National Semiconductor

NMC9346 1024-Bit Serial Electrically Erasable Programmable Memory

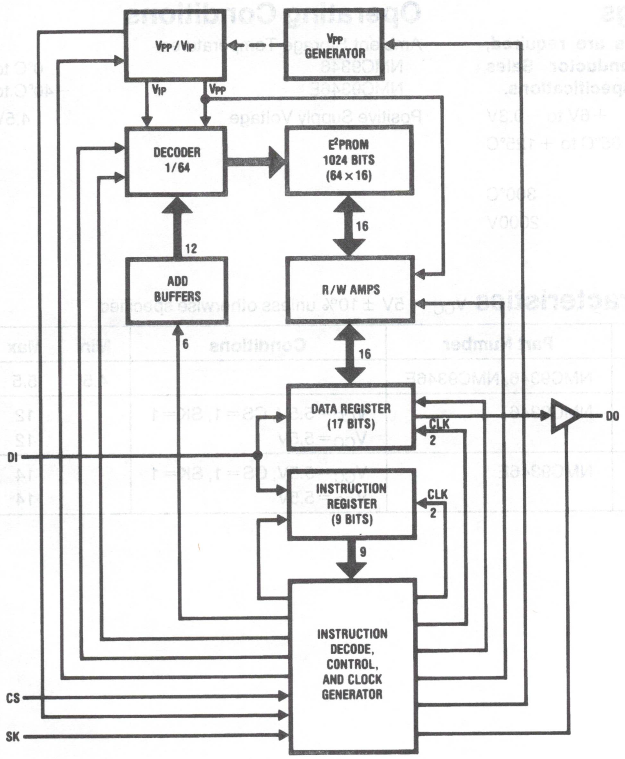
General Description

The NMC9346 is a 1024-bit non-volatile, sequential E²PROM, fabricated using advanced N-channel E²PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9346 has been designed for applications requiring up to 4 x 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

- Designed for 40,000 erase/write cycles
- 10 year data retention
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 x 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block Diagram



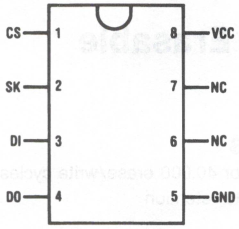
VPP / VIP
VPP GENERATOR
VIP
VPP
DECODER 1/64
E²PROM 1024 BITS (64 x 16)
16
12
ADD BUFFERS
R/W AMPS
6
16
DATA REGISTER (17 BITS)
CLK
2
DO
DI
INSTRUCTION REGISTER (9 BITS)
CLK
2
9
INSTRUCTION DECODE, CONTROL, AND CLOCK GENERATOR
CS
SK

TL/D/9205-1

Pin Names	
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	No Connection

Connection Diagrams

Dual-In-Line Package (N)

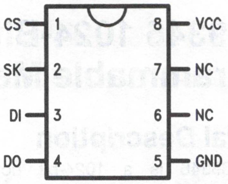


TL/D/9205-2

Top View

See NS Package Number N08E

8-Pin SO Package (M8)



TL/D/9205-7

Top View

See NS Package Number M08A

Device Marking: 9346, 9346E

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NMC9346N NMC9346M8

Extended Temp. Range (−40°C to +85°C)

Order Number
NMC9346EN NMC9346EM8

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage Relative to GND	+6V to −0.3V
Ambient Storage Temperature	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD rating.	2000V

Operating Conditions

Ambient Storage Temperatures	
NMC9346	0°C to +70°C
NMC9346E	−40°C to +85°C
Positive Supply Voltage	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
V_{CC}	Operating Voltage	NMC9346, NMC9346E		4.5	5.5	V
I_{CC1}	Operating Current	NMC9346	V_{CC}=5.5V, CS=1, SK=1		12	mA
	Erase/Write Operating Current		V_{CC}=5.5V		12	mA
	Operating Current	NMC9346E	V_{CC}=5.5V, CS=1, SK=1		14	mA
	Erase/Write Operating Current		V_{CC}=5.5V		14	mA

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC2}	Standby Current	NMC9346	$V_{CC}=5.5V$, $CS=0$		3	mA
	Standby Current	NMC9346E	$V_{CC}=5.5V$, $CS=0$		4	mA
	Input Voltage Levels	NMC9346, NMC9346E				
V_{IL}				−0.1	0.8	V
V_{IH}				2.0	$V_{CC}+1$	V
	Output Voltage Levels	NMC9346, NMC9346E				
V_{OL}			$I_{OL}=2.1$ mA		0.4	V
V_{OH}			$I_{OH}=-400$ μA	2.4		V
I_{LI}	Input Leakage Current	NMC9346, NMC9346E	$V_{IN}=5.5V$		10	μA
I_{LO}	Output Leakage Current	NMC9346, NMC9346E	$V_{OUT}=5.5V$, $CS=0$		10	μA
	SK Frequency	MMC9346		0	250	kHz
t_{SKH}	SK High Time (Note 2)			1		μs
t_{SKL}	SK Low Time (Note 2)			1		μs
	SK Frequency	MMC9346E		0		kHz
	SK High Time (Note 2)			1	250	μs
	SK Low Time (Note 2)			1		μs
	Inputs	NMC9346, NMC9346E				
t_{CSS}	CS			0.2		μs
t_{CSH}				0		μs
t_{DIS}	DI			0.4		μs
t_{DIH}				0.4		μs
	Output	NMC9346, NMC9346E	$C_L=100$ pF			
$t_{pd}1$	DO		$V_{OL}=0.8V$, $V_{OH}=2.0V$		2	μs
$t_{pd}0$						
$t_{E/W}$	Self-Timed Program Cycle	NMC9346			10	ms
	Self-Timed Program Cycle	NMC9346E			10	ms
t_{CS}	Min CS Low Time (Note 3)	NMC9346, NMC9346E		1		μs
t_{SV}	Rising Edge of CS to Status Valid	NMC9346, NMC9346E	$C_L=100$ pF		1	μs
t_{OH}, t_{IH}	Falling Edge of CS to DO TRI-STATE®	NMC9346, NMC9346E			0.4	μs

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 4 μs. e.g., if $t_{SKL} = 1$ μs then the minimum $t_{SKH} = 3$ μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

*Thruout this table "M" refers to temperature range (−55°C to +125°C), not package.

Functional Description

The NMC9346 is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. The NMC9346 is organized as sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase, chip write) to prevent spurious programming during other modes. The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming enable instruction (EWEN) is needed to keep the part in the enable state if the power supply (V_{CC}) noise falls below operating range. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E^{2}PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 4)

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μS (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

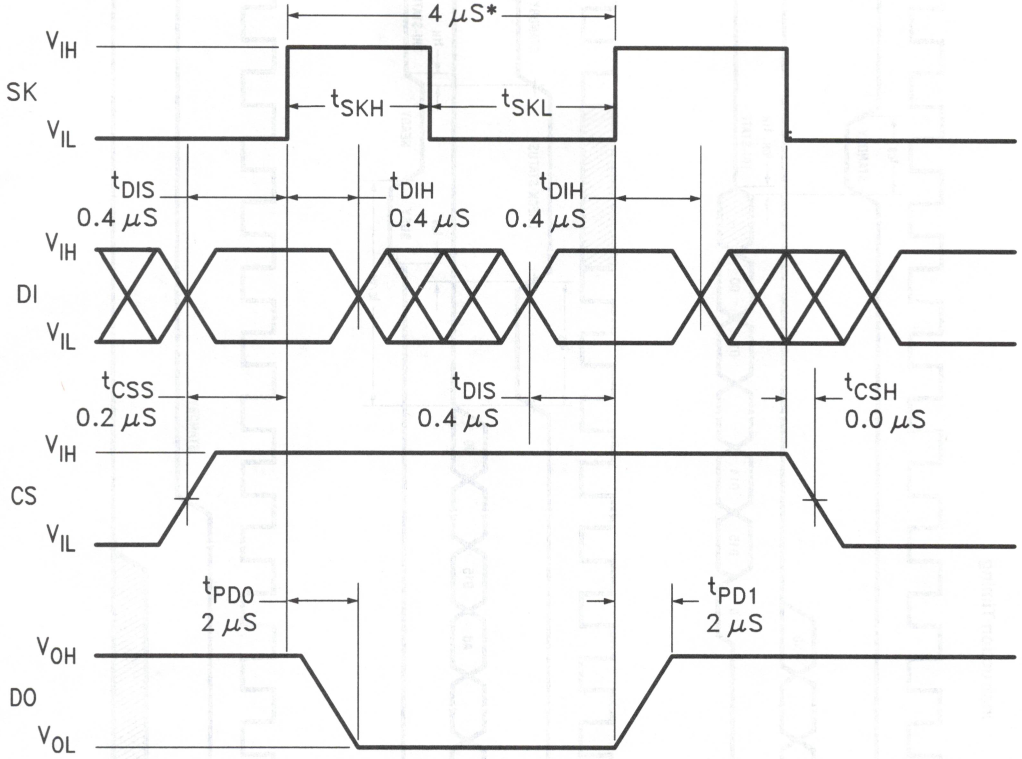
Instruction Set for NMC9346

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read Register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15–D0	Write Register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase Register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/Write Enable
EWDS	1	00	00xxxx		Erase/Write Disable
ERAL	1	00	10xxxx		Erase All Registers
WRAL	1	00	01xxxx	D15–D0	Write All Registers

NMC9346 has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Timing Diagrams

Synchronous Data Timing

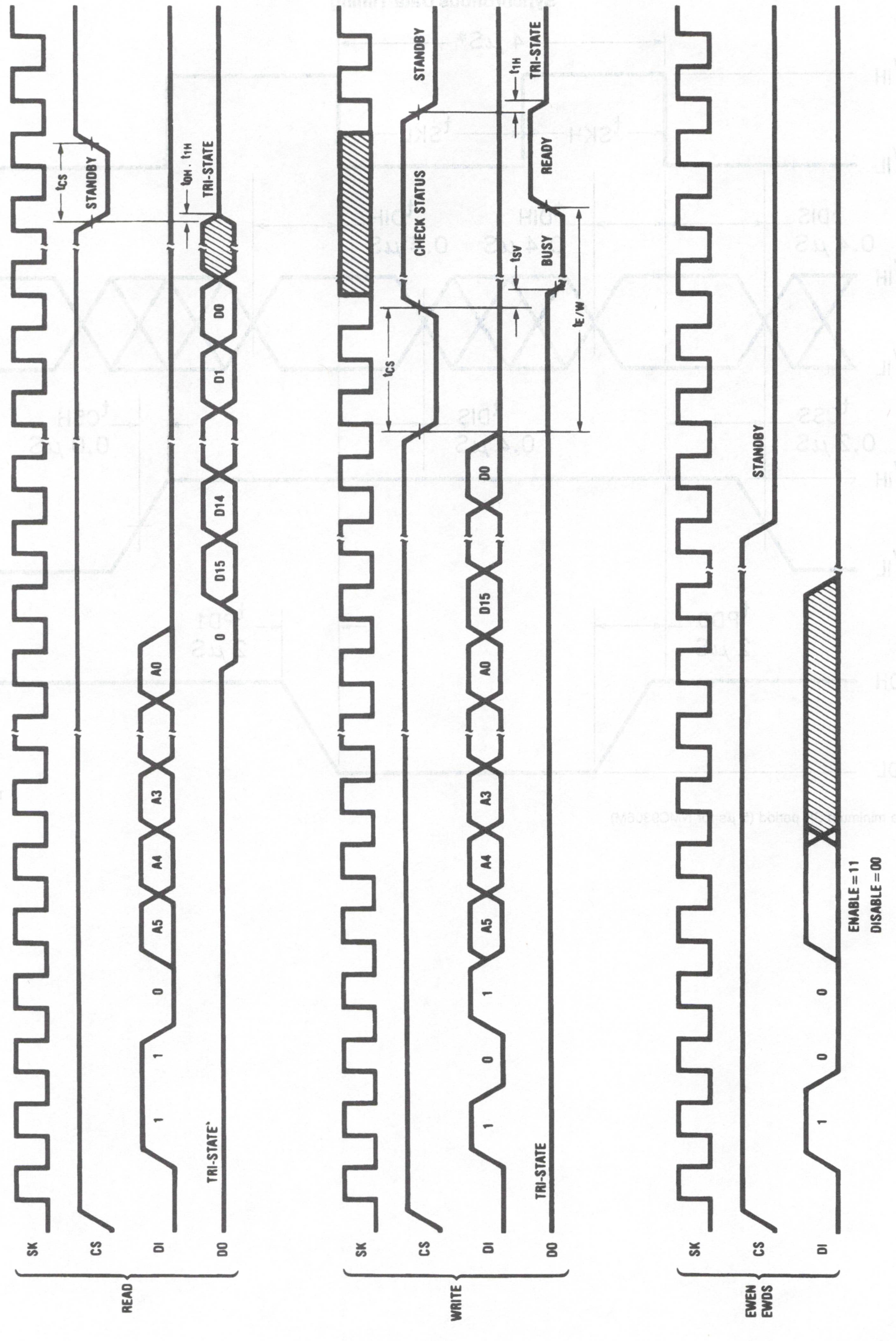

4 μS*
SK
V_{IH}
V_{IL}
t_{SKH}
t_{SKL}
t_{DIS} 0.4 μS
t_{DIH} 0.4 μS
t_{DIH} 0.4 μS
DI
V_{IH}
V_{IL}
t_{CSS} 0.2 μS
t_{DIS} 0.4 μS
t_{CSH} 0.0 μS
CS
V_{IH}
V_{IL}
t_{PD0} 2 μS
t_{PD1} 2 μS
DO
V_{OH}
V_{OL}

TL/D/9205-4

*This is the minimum SK period (5 μs for NMC9306M)

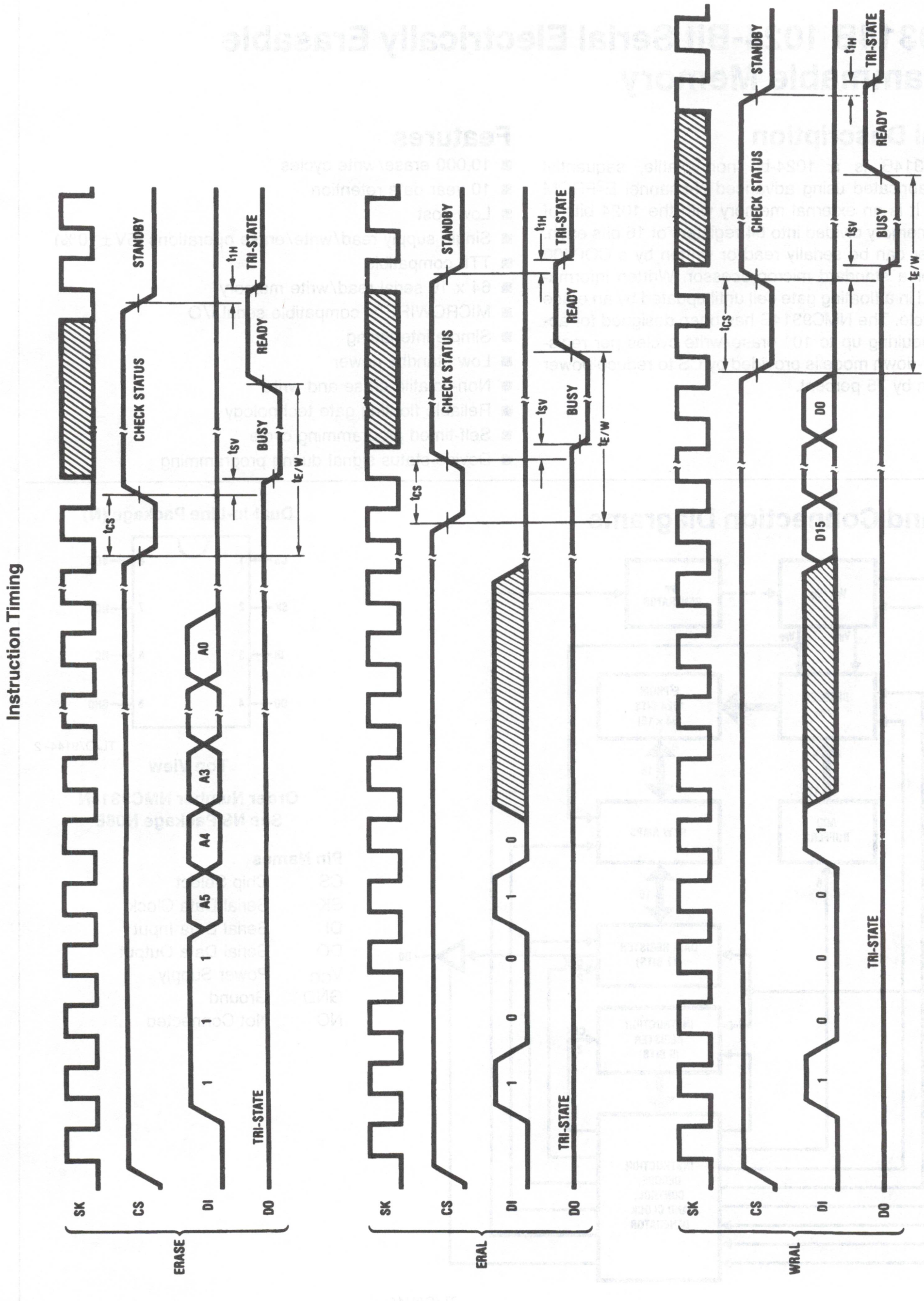
Timing Diagrams (Continued)

Instruction Timing


READ
SK
CS
DI
DO
TRI-STATE*
1
1
0
A5
A4
A3
A0
0
D15
D14
D1
D0
tCS
STANDBY
tDH, tIH
TRI-STATE
WRITE
SK
CS
DI
DO
TRI-STATE
1
0
1
A5
A4
A3
A0
D15
D0
tCS
CHECK STATUS
STANDBY
tSV
BUSY
READY
tE/W
tIH
TRI-STATE
EWEN
EWDS
SK
CS
DI
1
0
0
ENABLE = 11
DISABLE = 00
STANDBY

TL/D/9205-5

Timing Diagrams (Continued)


Instruction Timing
ERASE
SK
CS
DI
DO
1
1
1
A5
A4
A3
A0
TRI-STATE
tCS
CHECK STATUS
STANDBY
tSV
BUSY
READY
tE/W
tIH
TRI-STATE
ERAL
SK
CS
DI
DO
1
0
0
1
0
TRI-STATE
tCS
CHECK STATUS
STANDBY
tSV
BUSY
READY
tE/W
tIH
TRI-STATE
WRAL
SK
CS
DI
DO
1
0
0
0
1
D15
D0
TRI-STATE
CHECK STATUS
STANDBY
tCS
tSV
BUSY
READY
tE/W
tIH
TRI-STATE

TL/D/9205-6

National Semiconductor

NMC9314B 1024-Bit Serial Electrically Erasable Programmable Memory

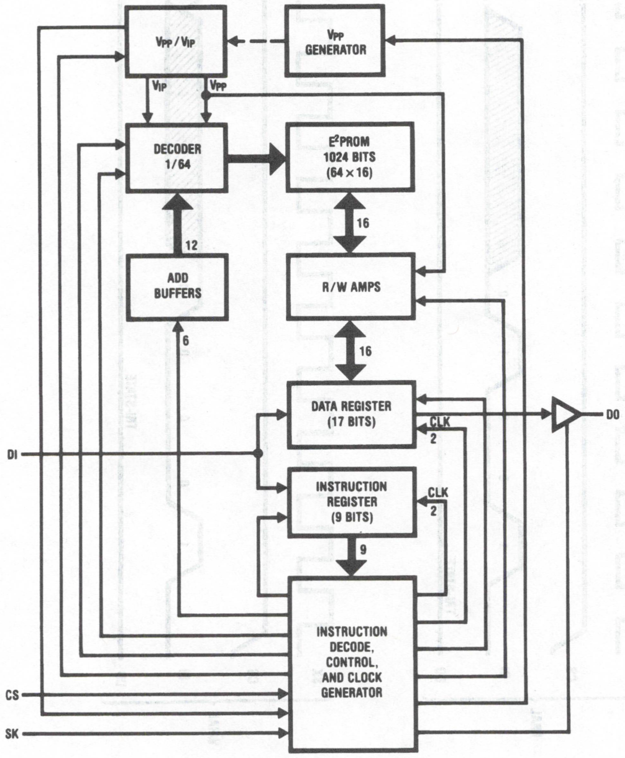
General Description

The NMC9314B is a 1024-bit non-volatile, sequential E^{2}PROM, fabricated using advanced N-channel E^{2}PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9314B has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

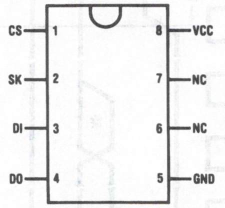
- 10,000 erase/write cycles
- 10 year data retention
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 x 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block and Connection Diagrams


VPP / VIP
VPP GENERATOR
VIP
VPP
DECODER 1/64
E²PROM 1024 BITS (64 × 16)
16
12
ADD BUFFERS
R/W AMPS
6
16
DATA REGISTER (17 BITS)
CLK 2
DO
DI
INSTRUCTION REGISTER (9 BITS)
CLK 2
9
INSTRUCTION DECODE, CONTROL, AND CLOCK GENERATOR
CS
SK

TL/D/9144-1

Dual-In-Line Package (N)


CS 1
SK 2
DI 3
DO 4
8 VCC
7 NC
6 NC
5 GND

TL/D/9144-2

Top View

Order Number NMC9314N
See NS Package N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temp.	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	>2000V

DC and AC Electrical Characteristics $0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$ unless specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Operating Voltage		4.5	5.5	V
I_{CC1}	Operating Current	$V_{CC} = 5.5V$, CS = 1, SK = 1		17	mA
	Erase/Write Operating Current	$V_{CC} = 5.5V$		17	mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		5	mA
	Input Voltage Levels				
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	$V_{CC} + 0.5$	V
	Output Voltage Levels				
V_{OL}		$I_{OL} = 2.1$ mA		0.4	V
V_{OH}		$I_{OH} = -400$ µA	2.4		V
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$		10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0		10	µA
	SK Frequency		0	200	kHz
t_{SKH}	SK High Time (Note 2)		3		µs
t_{SKL}	SK Low Time (Note 2)		2		µs
	Inputs				
t_{CSS}	CS		0.2		µs
t_{CSH}			0		µs
t_{DIS}	DI		0.4		µs
t_{DIH}			0.4		µs
	Output	$C_L = 100$ pF			
t_{pd1}	DO	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$		2	µs
t_{pd0}		$V_{IL} = 0.45V$, $V_{IH} = 2.40V$		2	µs
$t_{E/W}$	Self-Timed Program Cycle			15	ms
t_{CS}	Min CS Low Time (Note 3)		1		µs
t_{SV}	Rising Edge of CS to Status Valid	$C_L = 100$ pF		1	µs
t_{OH}, t_{IH}	Falling Edge of CS to DO TRI-STATE®			0.4	µs

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 5 µs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 5 µs. e.g., if $t_{SKL} = 2$ µs then the minimum $t_{SKH} = 3$ µs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 µs (t_{CS}) between consecutive instruction cycles.

Instruction Set for NMC9314B

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15–D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/write enable
EWDS	1	00	00xxxx		Erase/write disable
ERAL	1	00	10xxxx		Erase all registers
WRAL	1	00	01xxxx	D15–D0	Write all registers

NMC9314B has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Functional Description

The NMC9314B is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. Its organization is sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase, chip write). The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 4)

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 µS (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

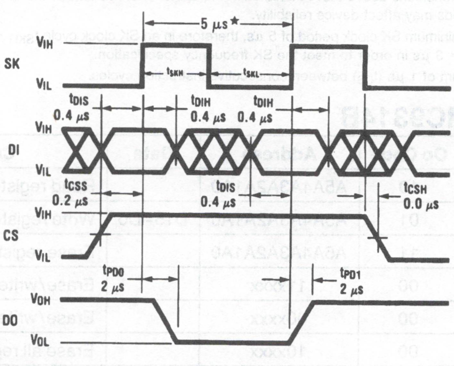
CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

Timing Diagrams

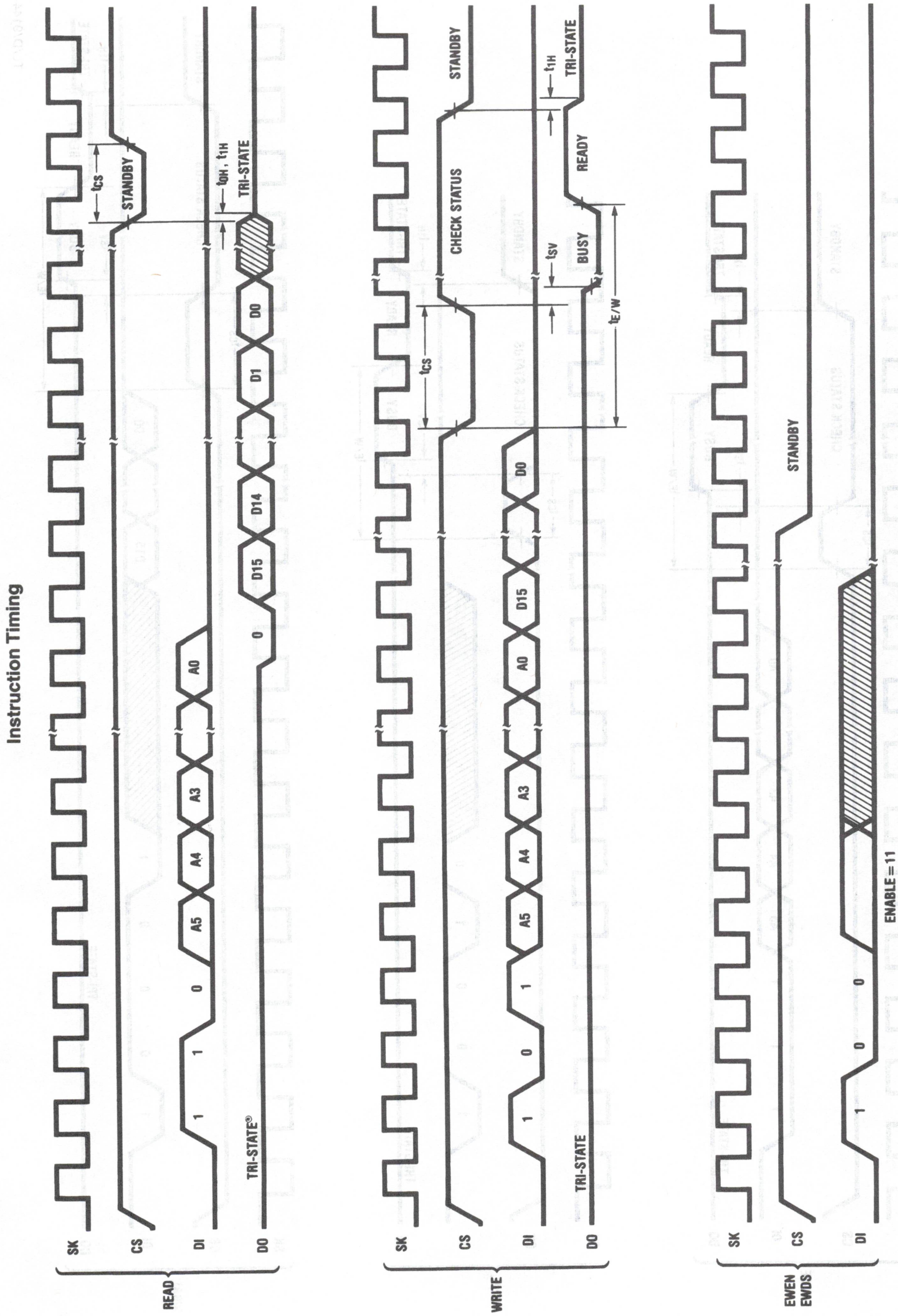
Synchronous Data Timing



*This is the minimum SK period.

TL/D/9144-3

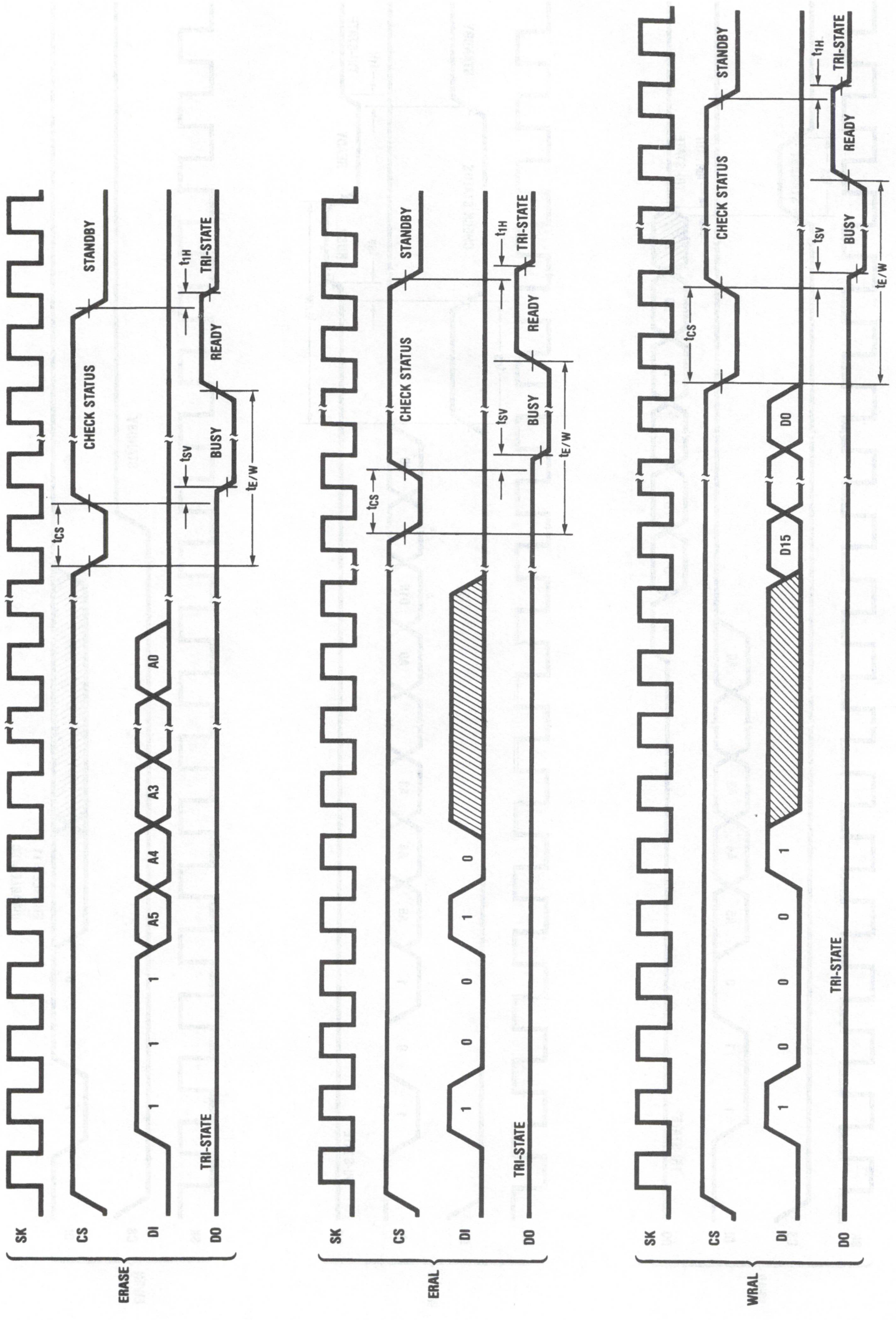
Timing Diagrams (Continued)


Instruction Timing
READ
SK
CS
DI
DO
tCS
STANDBY
1
1
0
A5
A4
A3
A0
TRI-STATE®
0
D15
D14
D1
D0
tDH, t1H
TRI-STATE
WRITE
SK
CS
DI
DO
tCS
CHECK STATUS
STANDBY
1
0
1
A5
A4
A3
A0
D15
D0
TRI-STATE
tSV
BUSY
READY
t1H
TRI-STATE
tE/W
EWEN
EWDS
SK
CS
DI
STANDBY
1
0
0
ENABLE=11
DISABLE=00

TL/D/9144-4

Timing Diagrams (Continued)

Instruction Timing


ERASE
SK
CS
DI
DO
1
1
1
A5
A4
A3
A0
TRI-STATE
tCS
CHECK STATUS
STANDBY
tSV
BUSY
READY
t1H
TRI-STATE
tE/W
ERAL
SK
CS
DI
DO
1
0
0
1
0
TRI-STATE
tCS
CHECK STATUS
STANDBY
tSV
BUSY
READY
t1H
TRI-STATE
tE/W
WRAL
SK
CS
DI
DO
1
0
0
0
1
D15
D0
TRI-STATE
tCS
CHECK STATUS
STANDBY
tSV
BUSY
READY
t1H
TRI-STATE
tE/W

TL/D/9144-5

National Semiconductor

NMC93C56/C66 2048-Bit/4096-Bit Serial Electrically Erasable Programmable Memories

General Description

The NMC93C56/NMC93C66 are 2048/4096 bits of CMOS electrically erasable memory divided into 128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high speed and low power. They operate from a single 5V supply since V_{PP} is generated on-board. The serial organization allow the NMC93C56/66 to be packaged in an 8-pin DIP or 14-pin SO package to save board space.

The memories feature a serial interface with the instruction, address, and write data, input on the Data-In (DI) pin. All read data and device status come out on the Data-Out (DO) pin. A low-to-high transition of shift clock (SK) shifts all data in and out. This serial interface is MICROWIRE™ compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The NMC93C56/66 do not require an erase cycle prior to the Write and Write All instructions. The Erase and Erase All instructions are available to maintain complete read and programming capability with the NMOS NMC9346. All programming cycles are completely self-timed for simplified operation. The busy status is available on the DO pin to indicate the completion of a programming cycle. EEPROMs are shipped in the erased state where all bits are logical 1's.

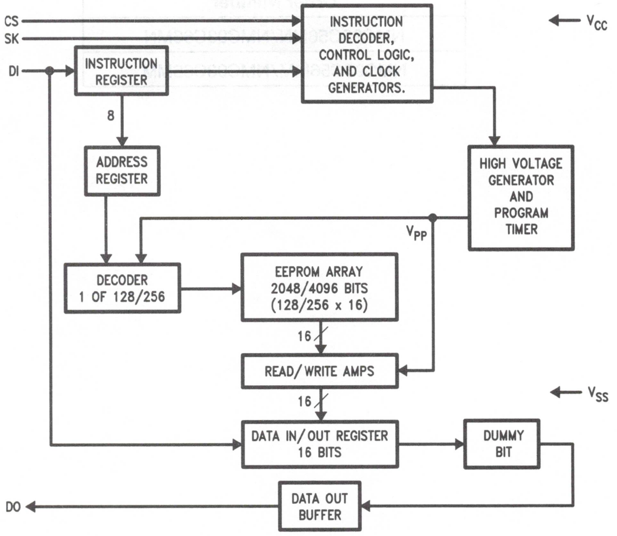
Compatibility with Other Devices

These memories are pin compatible to National Semiconductor's NMOS EEPROMs, NMC9306 and NMC9346 and CMOS EEPROMs NMC93C06/46. The NMC93C56/66 are both pin and function compatible with the NMC93C06/46, 256/1024-bit EEPROM with the one exception that the NMC93C56/66 require 2 additional address bits.

Features

- Typical active current 400 μA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 5V only operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential register read
- Over 40 years data retention
- Designed for 100,000 write cycles

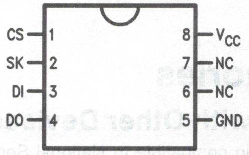
Block Diagram


CS
SK
DI
INSTRUCTION REGISTER
8
INSTRUCTION DECODER, CONTROL LOGIC, AND CLOCK GENERATORS.
V_{CC}
ADDRESS REGISTER
HIGH VOLTAGE GENERATOR AND PROGRAM TIMER
V_{PP}
DECODER 1 OF 128/256
EEPROM ARRAY 2048/4096 BITS (128/256 x 16)
16
READ/WRITE AMPS
V_{SS}
16
DATA IN/OUT REGISTER 16 BITS
DUMMY BIT
DO
DATA OUT BUFFER

TL/D/9617-1

Connection Diagrams

Dual-In-Line Package (N)


CS
1
SK
2
DI
3
DO
4
8
VCC
7
NC
6
NC
5
GND

TL/D/9617–2

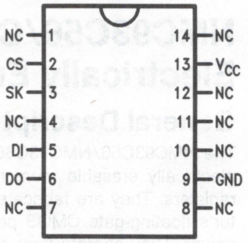
Top View

See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

SO Package (M)


NC
1
CS
2
SK
3
NC
4
DI
5
DO
6
NC
7
14
NC
13
VCC
12
NC
11
NC
10
NC
9
GND
8
NC

TL/D/9617–3

Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NMC93C56N/NMC93C66N
NMC93C56M/NMC93C66M

Extended Temp. Range (−40°C to +85°C)

Order Number
NMC93C56EN/NMC93C66EN
NMC93C56EM/NMC93C66EM

Military Temp. Range (−55°C to +125°C)

Order Number
NMC93C56MN/NMC93C66MN
NMC93C56MM/NMC93C66MM

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC93C56/NMC93C66	0°C to +10°C
NMC93C56E/NMC93C66E	−40°C to +85°C
NMC93C56M/NMC93C66M (Mil. Temp.)	−55°C to +125°C
Positive Power Supply	4.5V to 5.5V

DC and AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93C56/NMC93C66	CS = V_{IH}, SK = 1 MHz		2	
		NMC93C56E/NMC93C66E	SK = 0.5 MHz		2	mA
		NMC93C56M/NMC93C66M*	SK = 0.5 MHz		2	
I_{CC2}	Operating Current TTL Input Levels	NMC93C56/NMC93C66	CS = V_{IH}, SK = 1 MHz		3	
		NMC93C56E/NMC93C66E	SK = 0.5 MHz		3	mA
		NMC93C56M/NMC93C66M	SK = 0.5 MHz		4	
I_{CC3}	Standby Current	NMC93C56/NMC93C66	CS = 0V		50	
		NMC93C56E/NMC93C66E			100	µA
		NMC93C56M/NMC93C66M			100	
I_{IL}	Input Leakage	NMC93C56/NMC93C66	V_{IN} = 0V to V_{CC}	−2.5	2.5	
		NMC93C56E/NMC93C66E		−10	10	µA
		NMC93C56M/NMC93C66M		−10	10	µA
I_{OL}	Output Leakage	NMC93C56/NMC93C66	V_{IN} = 0V to V_{CC}	−2.5	2.5	
		NMC93C56E/NMC93C66E		−10	10	µA
		NMC93C56M/NMC93C66M		−10	10	µA
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NMC93CS56/NMC93C566	I_{OL} = 2.1 mA		0.4	
		NMC93CS56E/NMC93C566E	I_{OL} = 2.1 mA		0.4	V
		NMC93CS56M/NMC93C566M	I_{OL} = 1.8 mA		0.4	
V_{OH1}	Output High Voltage		I_{OH} = 400 µA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = −10 µA	V_{CC} − 0.2		V
f_{SK}	SK Clock Frequency	NMC93C56/NMC93C66		0	1	
		NMC93C56E/NMC93C66E		0	0.5	MHz
		NMC93C56M/NMC93C66M		0	0.5	
t_{SKH}	SK High Time	NMC93C56/NMC93C66	(Note 2)	250		
		NMC93C56E/NMC93C66E	(Note 3)	500		ns
		NMC93C56M/NMC93C66M	(Note 3)	500		
t_{SKL}	SK Low Time	NMC93C56/NMC93C66	(Note 2)	250		
		NMC93C56E/NMC93C66E	(Note 3)	500		ns
		NMC93C56M/NMC93C66M	(Note 3)	500		
t_{CS}	Minimum CS Low Time	NMC93C56/NMC93C66	(Note 4)	250		
		NMC93C56E/NMC93C66E	(Note 5)	500		ns
		NMC93C56M/NMC93C66M	(Note 5)	500		
t_{CSS}	CS Setup Time	NMC93C56/NMC93C66	Relative to SK	50		
		NMC93C56E/NMC93C66E		100		ns
		NMC93C56M/NMC93C66M		100		

***Note:** Throughout this table "M" refers to temperature range (−55°C to +125°C), not package type.

DC and AC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NMC93C56/NMC93C66	Relative to SK	100		ns
		NMC93C56E/NMC93C66E		200		
		NMC93C56M/NMC93C66M		200		
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93C56/NMC93C66	Relative to SK	100		ns
		NMC93C56E/NMC93C66E		200		
		NMC93C56M/NMC93C66M		200		
t_{PD1}	Output Delay to "1"	NMC93C56/NMC93C66	AC Test		500	ns
		NMC93C56E/NMC93C66E			1000	
		NMC93C56M/NMC93C66M			1000	
t_{PD0}	Output Delay to "0"	NMC93C56/NMC93C66	AC Test		500	ns
		NMC93C56E/NMC93C66E			1000	
		NMC93C56M/NMC93C66M			1000	
t_{SV}	CS to Status Valid	NMC93C56/NMC93C66	AC Test		500	ns
		NMC93C56E/NMC93C66E			1000	
		NMC93C56M/NMC93C66M			1000	
t_{DF}	CS to DO in TRI-STATE®	NMC93C56/NMC93C66	AC Test CS = V_{IL}		100	ns
		NMC93C56E/NMC93C66E			200	
		NMC93C56M/NMC93C66M			200	
t_{WP}	Write Cycle Time				10	ms

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 μs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Capacitance (Note 6)

T_A = 25°C f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

The NMC93C56 and NMC93C66 have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 10-bits carry the op code and the 8-bit address for register selection.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write All (WRAL):

The (WRAL) instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Erase/Write Disable (EWDS):

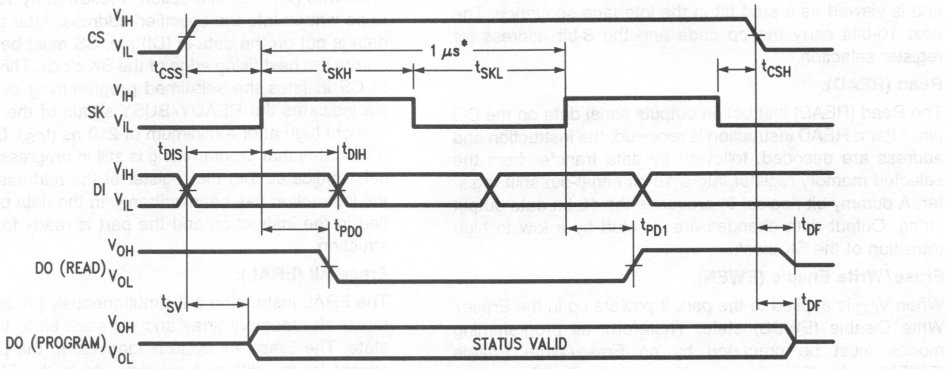
To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Instruction Set for the NMC93C56 and NMC93C66

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
ERASE	1	11	A7–A0		Erase register A7A6A5A4A3A2A1A0.
ERAL	1	00	10XXXXXX		Erases all registers.
WRITE	1	01	A7–A0	D15–D0	Writes register if address is unprotected.
WRAL	1	00	01XXXXXX	D15–D0	Writes all registers. Valid only when Protect Register is cleared.
EWDS	1	00	00XXXXXX		Disables all programming instructions.

Timing Diagrams

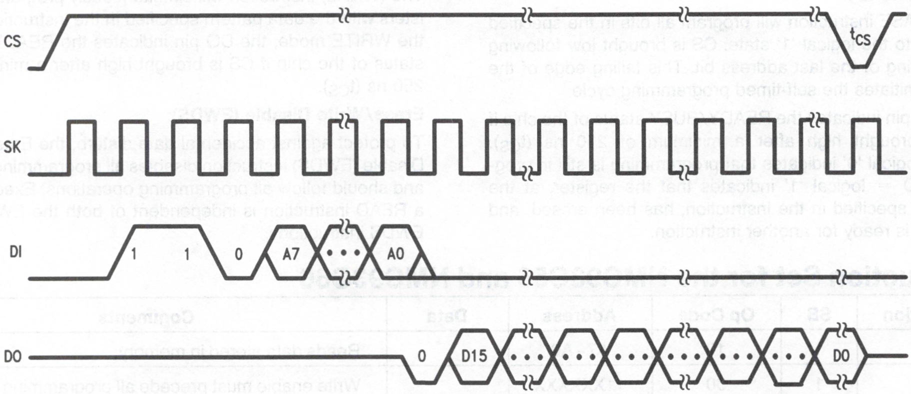
Synchronous Data Timing


CS
V_IH
V_IL
t_CSS
t_SKH
1 μs*
t_SKL
t_CSH
SK
V_IH
V_IL
t_DIS
t_DIH
DI
V_IH
V_IL
t_PDO
t_PD1
t_DF
DO (READ)
V_OH
V_OL
t_SV
t_DF
DO (PROGRAM)
V_OH
V_OL
STATUS VALID

TL/D/9617-4

*This is the minimum SK period (Note 2).

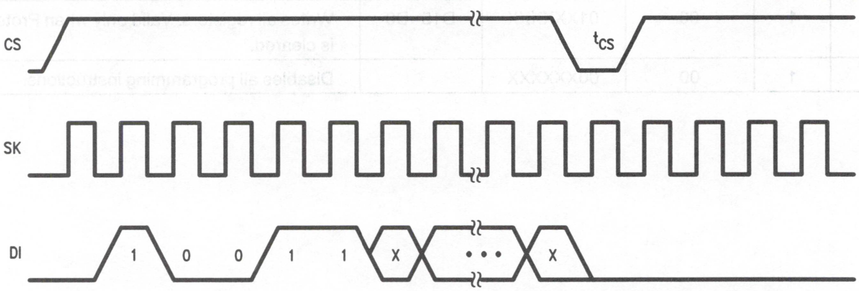
READ:


CS
t_CS
SK
DI
1
1
0
A7
• • •
A0
DO
0
D15
• • •
D0

TL/D/9617-5

*Address bit A_7 becomes a "don't care" for NMC93C56.

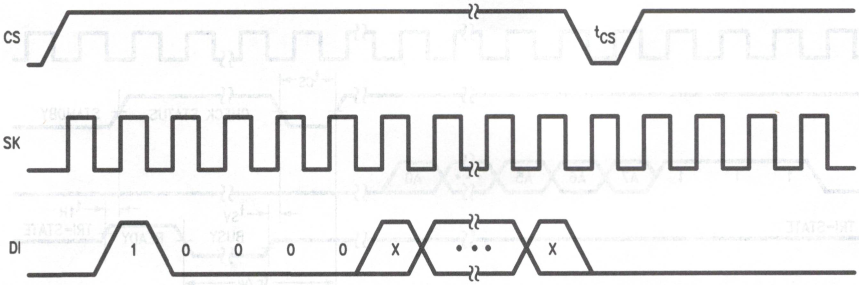
EWEN:


CS
t_CS
SK
DI
1
0
0
1
1
X
• • •
X

TL/D/9617-6

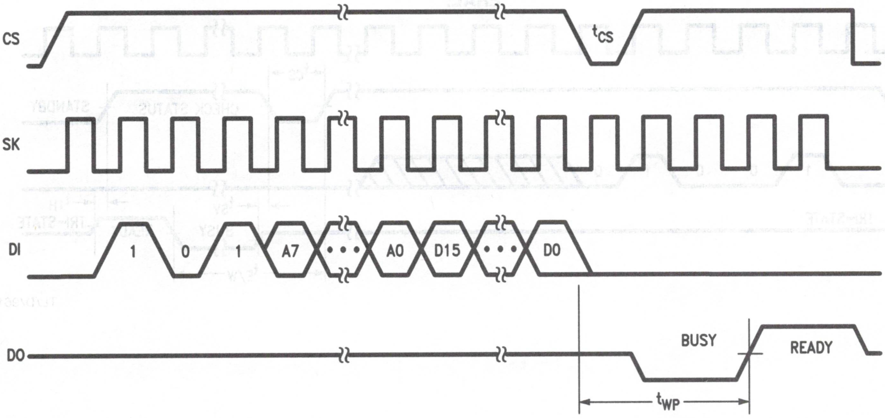
Timing Diagrams (Continued)

EWDS:


CS
tCS
SK
DI
1
0
0
0
0
X
• • •
X

TL/D/9617-7

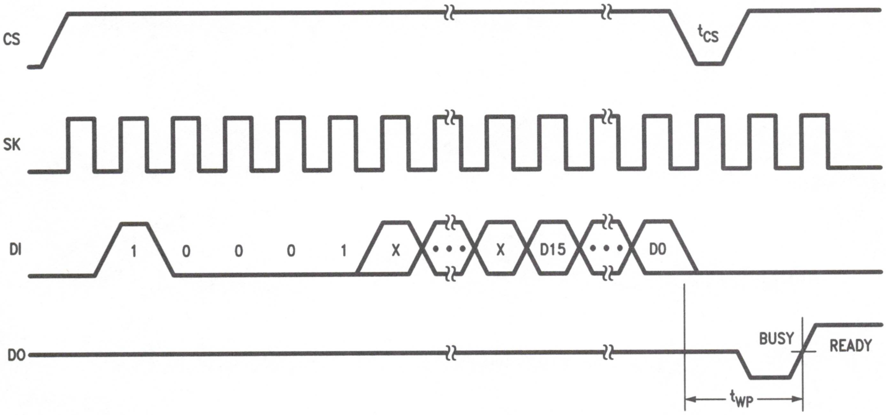
WRITE:


CS
tCS
SK
DI
1
0
1
A7
• • •
A0
D15
• • •
D0
DO
BUSY
READY
tWP

TL/D/9617-8

*Address bit A_7 becomes a "don't care" for NMC93C56.

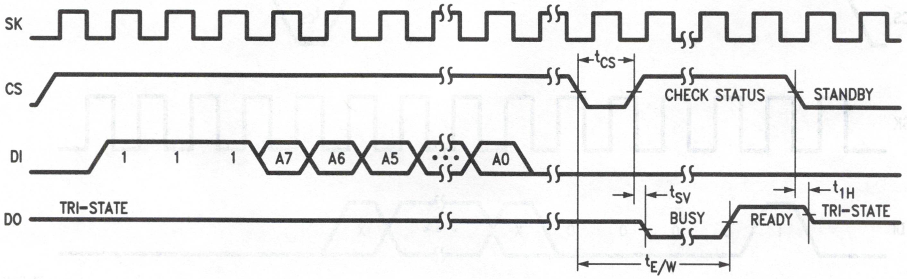
WRAL:


CS
tCS
SK
DI
1
0
0
0
1
X
• • •
X
D15
• • •
D0
DO
BUSY
READY
tWP

TL/D/9617-9

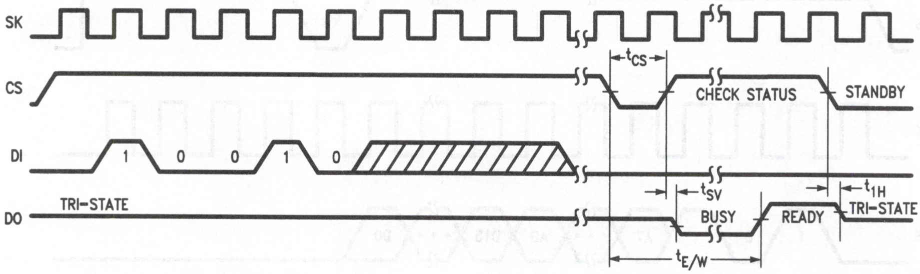
Timing Diagrams (Continued)

ERASE:


SK
CS
DI
DO
t_{CS}
CHECK STATUS
STANDBY
1
1
1
A7
A6
A5
• • •
A0
t_{SV}
t_{1H}
TRI-STATE
BUSY
READY
TRI-STATE
$t_{E/W}$

TL/D/9617–10

ERAL:


SK
CS
DI
DO
t_{CS}
CHECK STATUS
STANDBY
1
0
0
1
0
t_{SV}
t_{1H}
TRI-STATE
BUSY
READY
TRI-STATE
$t_{E/W}$

TL/D/9617–11

National Semiconductor

NMC93CS56/CS66 2048-Bit/4096-Bit Serial Electrically Erasable Programmable Memories

General Description

The NMC93CS56/NMC93CS66 are 2048/4096 bits of read/write memory divided into 128/256 registers of 16 bits each. N registers (N ≤ 128 or N ≤ 256) can be protected against data modification by programming into a special on-chip register, called the memory "protect register", the address of the first register to be protected. This address can be "locked" into the device, so that these registers can be permanently protected. Thereafter, all attempts to alter data in a register whose address is equal to or greater than the address stored in the "protect register" will be aborted.

The "read" instruction loads the address of the first register to be read into an 8-bit address pointer. Then the data is clocked out serially on the "DO" pin and automatically cycles to the next register to produce a serial data stream. In this way the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 2048/4096 bits. Thus, the NMC93CS56/NMC93CS66 can be viewed as a non-volatile shift register.

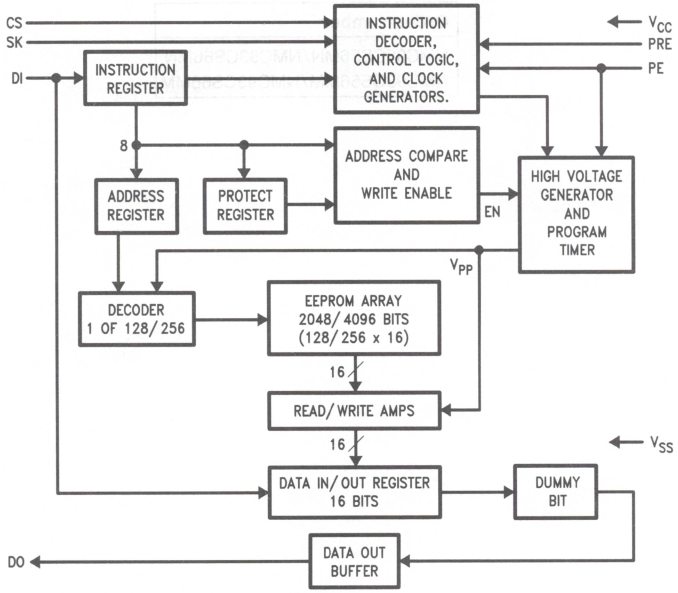
The "write" cycle is completely self-timed. No separate erase cycle is required before write. The "write" cycle is only enabled when pin 6 (program enable) is held "high". If the address of the register to be written is less than the address in the "protect register" then the data is written 16 bits at a time into one of the 128/256 data registers. If "CS" is brought "high" following the initiation of a "write" cycle, the "DO" pin indicates the ready/busy status of the chip.

National Semiconductor's EEPROMs are designed and tested for applications requiring extended endurance. Refer to device operation for further endurance information. Data retention is specified to be greater than 40 years.

Features

- Write protection in user defined section of memory
- Typical active current 400 μA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 5 volt only operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential register read
- Over 40 years data retention
- Designed for 100,000 write cycles

Block Diagram

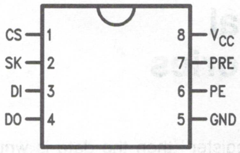

CS
SK
DI
INSTRUCTION REGISTER
INSTRUCTION DECODER, CONTROL LOGIC, AND CLOCK GENERATORS.
VCC
PRE
PE
8
ADDRESS COMPARE AND WRITE ENABLE
ADDRESS REGISTER
PROTECT REGISTER
EN
HIGH VOLTAGE GENERATOR AND PROGRAM TIMER
VPP
DECODER 1 OF 128/256
EEPROM ARRAY 2048/4096 BITS (128/256 x 16)
16
READ/WRITE AMPS
16
VSS
DATA IN/OUT REGISTER 16 BITS
DUMMY BIT
DO
DATA OUT BUFFER

TL/D/9209–3

Connection Diagrams

PIN OUT:

Dual-In-Line Package (N)


CS 1
SK 2
DI 3
DO 4
8 V$_{CC}$
7 PRE
6 PE
5 GND

TL/D/9209-1

Top View

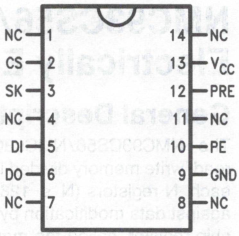
See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V$_{CC}$	Power Supply

PIN OUT:

SO Package (M)


NC 1
CS 2
SK 3
NC 4
DI 5
DO 6
NC 7
14 NC
13 V$_{CC}$
12 PRE
11 NC
10 PE
9 GND
8 NC

TL/D/9209-2

Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NMC93CS56N/NMC93CS66N
NMC93CS56M/NMC93CS66M

Extended Temp. Range (−40°C to +85°C)

Order Number
NMC93CS56EN/NMC93CS66EN
NMC93CS56EM/NMC93CS66EM

Military Temp. Range (−55°C to +125°C)

Order Number
NMC93CS56MN/NMC93CS66MN
NMC93CS56MM/NMC93CS66MM

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Storage Temperature	
NMC93CS56/MNC93CS66	0°C to +70°C
NMC93CS56E/NMC93CS66E	−40°C to +85°C
NMC93CS56M/NMC93CS66M (Mil. Temp.)	−55°C to +125°C
Positive Power Supply	4.5V to 5.5V

DC and AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93CS56/NMC93CS66	CS = V_{IH}, SK = 1 MHz		2	mA
		NMC93CS56E/NMC93CS66E	SK = 0.5 MHz		2	
		NMC93CS56M/NMC93CS66M*	SK = 0.5 MHz		2	
I_{CC2}	Operating Current TTL Input Levels	NMC93CS56/NMC93CS66	CS = V_{IH}, SK = 1 MHz		3	mA
		NMC93CS56E/NMC93CS66E	SK = 0.5 MHz		3	
		NMC93CS56M/NMC93CS66M	SK = 0.5 MHz		4	
I_{CC3}	Standby Current	NMC93CS56/NMC93CS66	CS = 0V		50	µA
		NMC93CS56E/NMC93CS66E			100	
		NMC93CS56M/NMC93CS66M			100	
I_{IL}	Input Leakage	NMC93CS56/NMC93CS66	V_{IN} = 0V to V_{CC}	−2.5	2.5	µA
		NMC93CS56E/NMC93CS66E		−10	10	µA
		NMC93CS56M/NMC93CS66M		−10	10	
I_{OL}	Output Leakage	NMC93CS56/NMC93CS66	V_{OUT} = 0V to V_{CC}	−2.5	2.5	µA
		NMC93CS56E/NMC93CS66E		−10	10	µA
		NMC93CS56M/NMC93CS66M		−10	10	
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NMC93CS56/NMC93CS66	I_{OL} = 2.1 mA		0.4	V
		NMC93CS56E/NMC93CS66E	I_{OL} = 2.1 mA		0.4	
		NMC93CS56M/NMC93CS66M	I_{OL} = 1.8 mA		0.4	
V_{OH1}	Output High Voltage		I_{OH} = −400 µA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = −10 µA	V_{CC} − 0.2		V
f_{SK}	SK Clock Frequency	NMC93CS56/NMC93CS66		0	1	MHz
		NMC93CS56E/NMC93CS66E		0	0.5	
		NMC93CS56M/NMC93CS66M		0	0.5	
t_{SKH}	SK High Time	NMC93CS56/NMC93CS66	(Note 2)	250		ns
		NMC93CS56E/NMC93CS66E	(Note 3)	500		
		NMC93CS56M/NMC93CS66M	(Note 3)	500		
t_{SKL}	SK Low Time	NMC93CS56/NMC93CS66	(Note 2)	250		ns
		NMC93CS56E/NMC93CS66E	(Note 3)	500		
		NMC93CS56M/NMC93CS66M	(Note 3)	500		
t_{CS}	Minimum CS Low Time	NMC93CS56/NMC93CS66	(Note 4)	250		ns
		NMC93CS56E/NMC93CS66E	(Note 5)	500		
		NMC93CS56M/NMC93CS66M	(Note 5)	500		
t_{CSS}	CS Setup Time	NMC93CS56/NMC93CS66	Relative to SK	50		ns
		NMC93CS56E/NMC93CS66E		100		
		NMC93CS56M/NMC93CS66M		100		
t_{PRES}	PRE Setup Time	NMC93CS56/NMC93CS66	Relative to SK	50		ns
		NMC93CS56E/NMC93CS66E		100		
		NMC93CS56M/NMC93CS66M		100		

*Thruout this table "M" refers to temperature range (−55°C to +125°C) not package.

DC and AC Electrical Characteristics

V_{CC} = 5V ±10% (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PES}	PE Setup Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	50 100 100		ns
t_{DIS}	DI Setup Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to CS Relative to CS Relative to CS	250 500 500		ns
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	100 200 200		ns
t_{PD1}	Output Delay to "1"	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test		500 1000 1000	ns
t_{PD0}	Output Delay to "0"	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test		500 1000 1000	ns
t_{SV}	CS to Status Valid	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test		500 1000 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test CS = V_{IL}		100 200 200	ns
t_{WP}	Write Cycle Time				10	ms

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 microsecond. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Capacitance (Note 6)

T_A = 25°C, f = 1MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

The NMC93CS56 and NMC93CS66 have 10 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 10-bits carry the op code and the 8-bit address for register selection.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the NONVOLATILE SHIFT-REGISTER mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it powers up in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The PE pin **MUST** be held "high" while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the "protect register" has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held "high" while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address stored in the "protect register" on the DO pin. The PRE pin **MUST** be held "high" while loading the instruction. Following the PRREAD instruction the 8-bit address stored in the memory Protect Register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 8-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before

Instruction Set for the NMC93CS56 and NMC93CS66

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Functional Description (Continued)

the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held "high" while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held "high" while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held "high" while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must *immediately* precede a PRWRITE instruction.

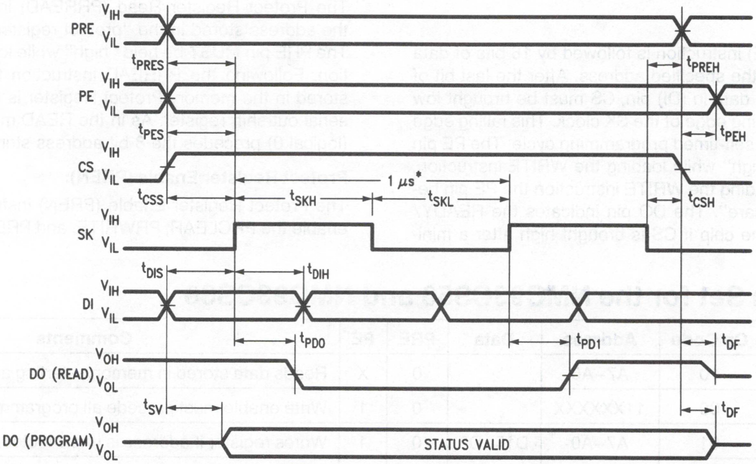
Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one time only** instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held "high" while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Timing Diagrams

Synchronous Data Timing

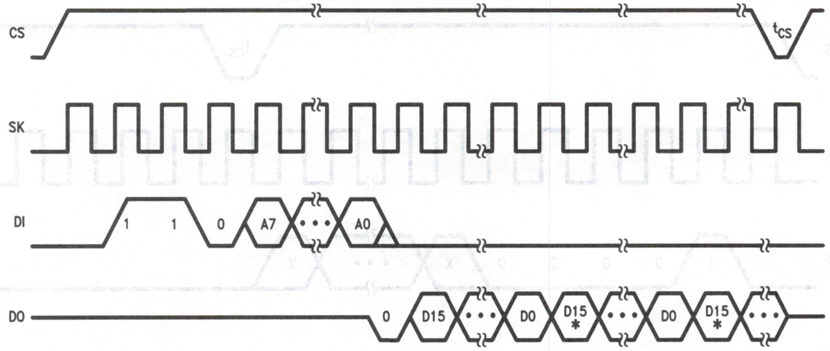


TL/D/9209-4

*This is the minimum SK period (See Note 2).

Timing Diagrams (Continued)

READ:*
PRE = 0, PE = X

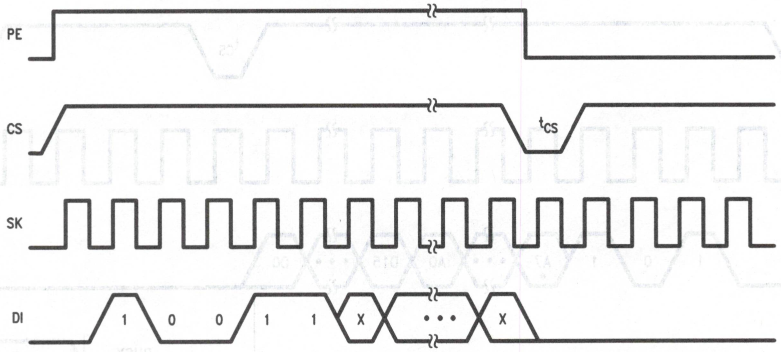

CS
tCS
SK
DI
1
1
0
A7
• • •
A0
DO
0
D15
• • •
D0
D15
*
• • •
D0
D15
*
• • •

TL/D/9209-5

*Address bit A_7 becomes a "don't care" for NMC93CS56.

*The memory automatically cycles to the next register.

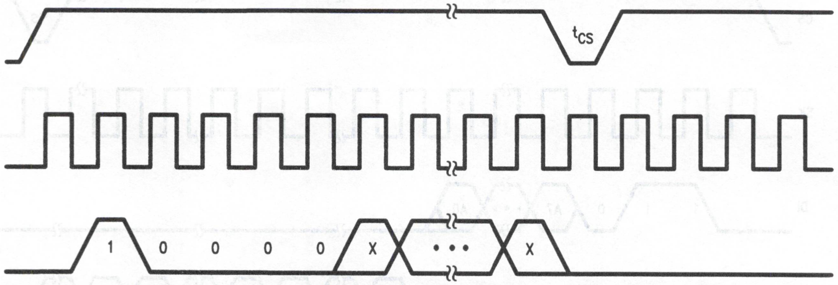
WEN:
PRE = 0, D0 = TRI-STATE


PE
CS
tCS
SK
DI
1
0
0
1
1
X
• • •
X

TL/D/9209-6

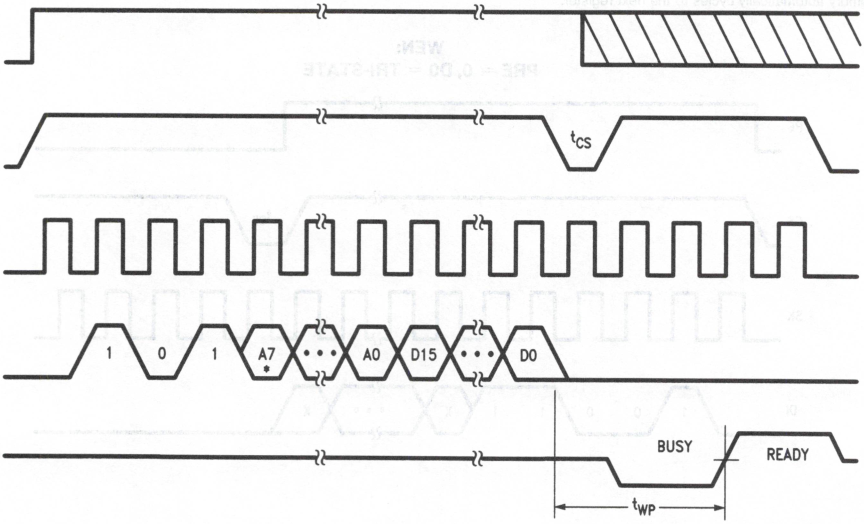
Timing Diagrams (Continued)

WDS:
PRE = 0, PE = X, DO = TRI-STATE


CS
tCS
SK
DI
1
0
0
0
0
X
• • •
X

TL/D/9209-7

WRITE:*
PRE = 0

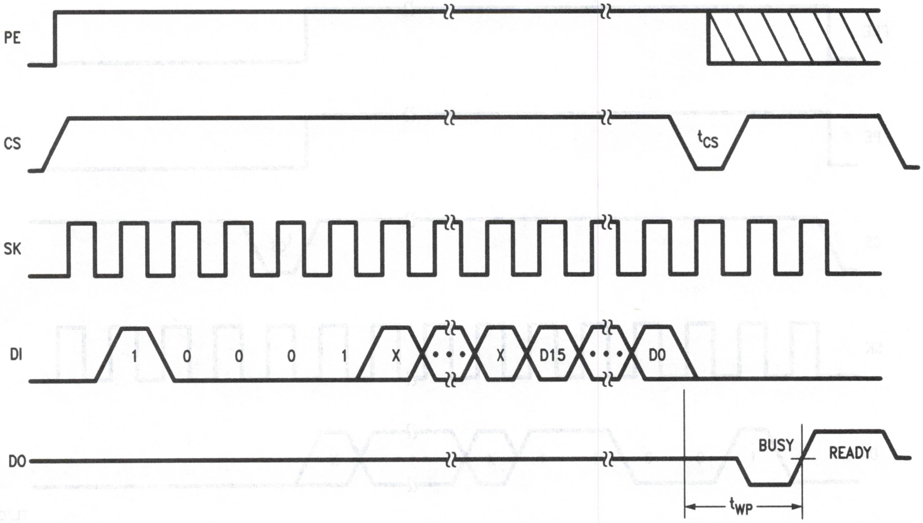

PE
CS
tCS
SK
DI
1
0
1
A7
*
• • •
A0
D15
• • •
D0
DO
BUSY
READY
tWP

TL/D/9209-8

*Address bit A_7 becomes a "don't care" for NMC93CS56.

Timing Diagrams (Continued)

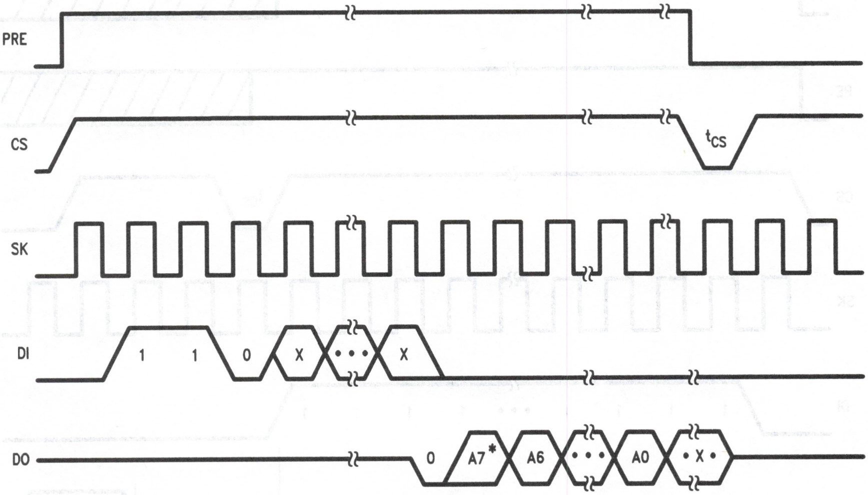
WRALL:*
PRE = 0


PE
CS
SK
DI
DO
t_{CS}
1
0
0
0
1
X
• • •
X
D15
• • •
D0
BUSY
READY
t_{WP}

TL/D/9209-9

*Protect Register **MUST** be cleared.

PRREAD:*
PE = X

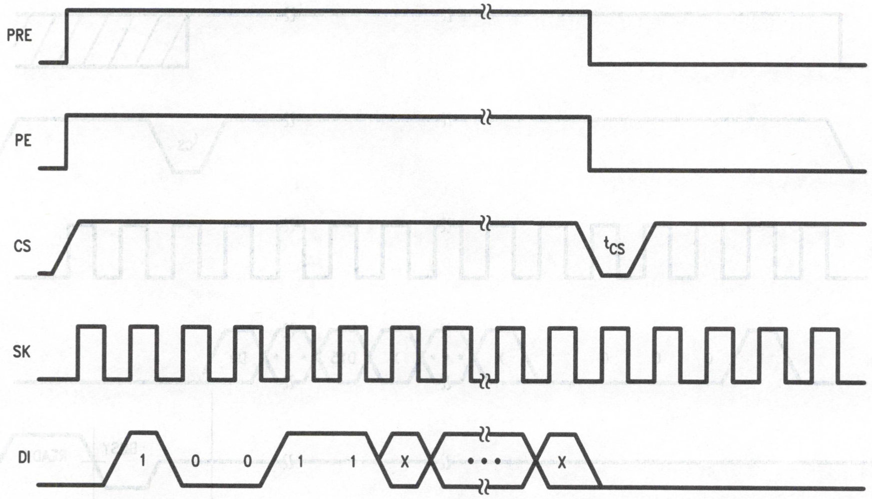

PRE
CS
SK
DI
DO
t_{CS}
1
1
0
X
• • •
X
0
A7*
A6
• • •
A0
• X •

TL/D/9209-10

*Address bit A_7 becomes a "don't care" for NMC93CS56.

Timing Diagrams (Continued)

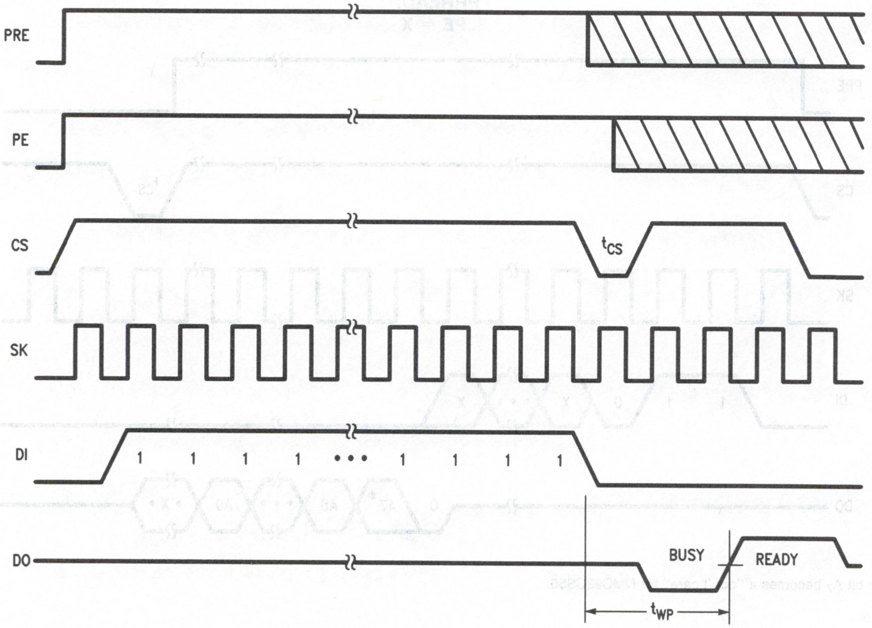
PREN:*
DO = TRI-STATE


PRE
PE
CS
t_{CS}
SK
DI
1
0
0
1
1
X
• • •
X

TL/D/9209–11

*A WEN cycle must precede a PREN cycle.

PRCLEAR:*

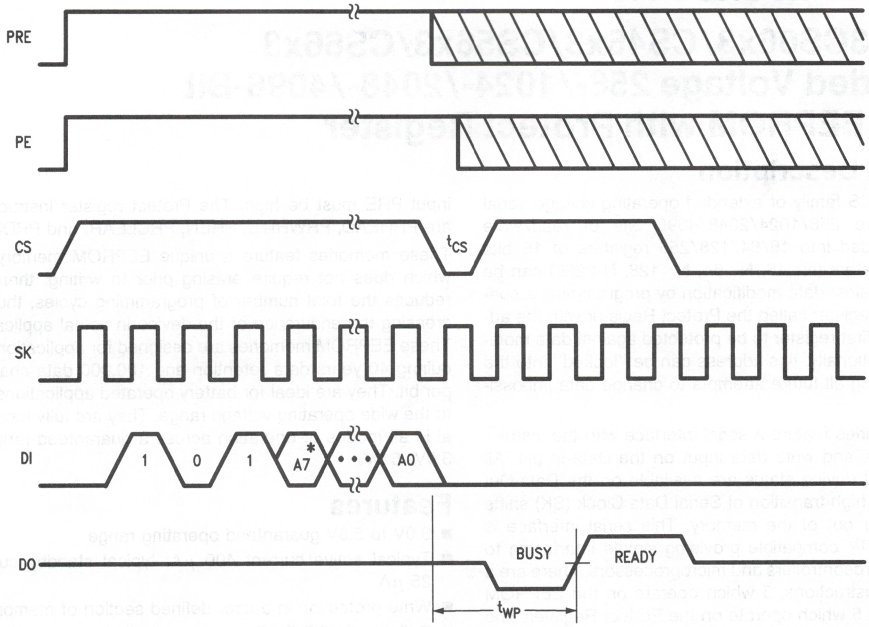

PRE
PE
CS
t_{CS}
SK
DI
1
1
1
1
• • •
1
1
1
1
DO
BUSY
READY
t_{WP}

TL/D/9209–12

*A PREN cycle must **immediately** precede a PRCLEAR cycle.

Timing Diagrams (Continued)

PRWRITE:†

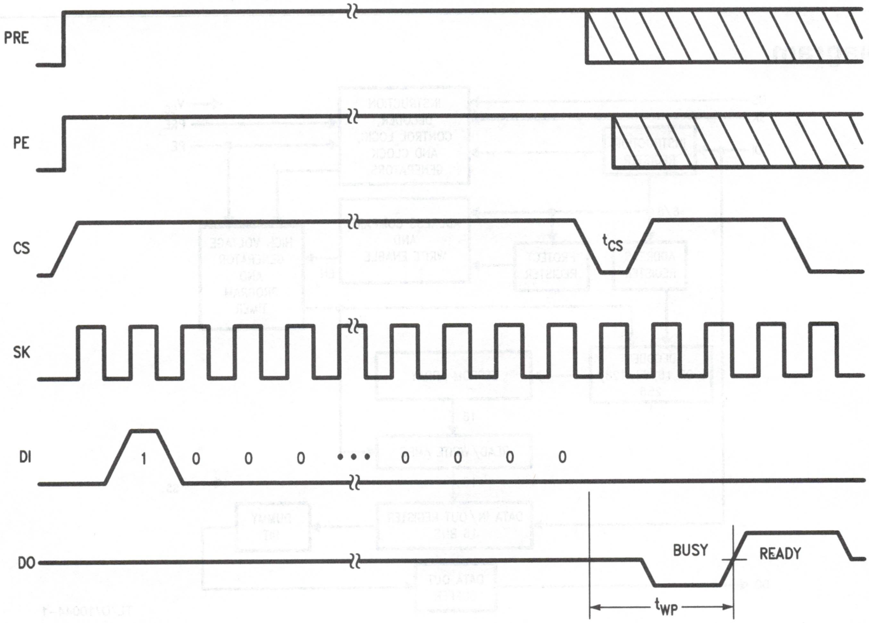

PRE
PE
CS
tCS
SK
DI
1
0
1
*
A7
• • •
A0
DO
BUSY
READY
tWP

TL/D/9209–13

*Address bit A_7 becomes a "don't care" for NMC93CS56.

†Protect Register **MUST** be cleared before a PRWRITE cycle. A PREN cycle must **immediately** precede a PRWRITE cycle.

PRDS:*


PRE
PE
CS
tCS
SK
DI
1
0
0
0
• • •
0
0
0
0
DO
BUSY
READY
tWP

TL/D/9209–14

***ONE TIME ONLY** instruction. A PREN cycle must **immediately** precede a PRDS cycle.

National Semiconductor

NMC93CS06x3/CS46x3/CS56x3/CS66x3 Extended Voltage 256-/1024-/2048-/4096-Bit Serial EEPROM with Protect Register

General Description

The NMC93CS family of extended operating voltage serial EEPROM are 256/1024/2048/4096 bits of read/write memory divided into 16/64/128/256 registers of 16 bits each. N registers (N≤16, N≤64, N≤128, N≤256) can be protected against data modification by programming a special on-chip register called the Protect Register with the address of the first register to be protected against data modification. Additionally, this address can be "locked" into the device, making all future attempts to change data impossible.

These memories feature a serial interface with the instruction, address, and write data input on the Data-In pin. All data-out, and device status are available on the Data-Out pin. A low to high transition of Serial Data Clock (SK) shifts all data in or out of the memory. This serial interface is MICROWIRE™ compatible providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory, and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL,* WRITE ENABLE, and WRITE DISABLE. To perform any of the memory instructions, the input PRE must be low. The instructions to the Protect Register are similar, except the input PRE must be high. The Protect register instructions are PRREAD, PRWRITE, PREN, PRCLEAR, and PRDS.

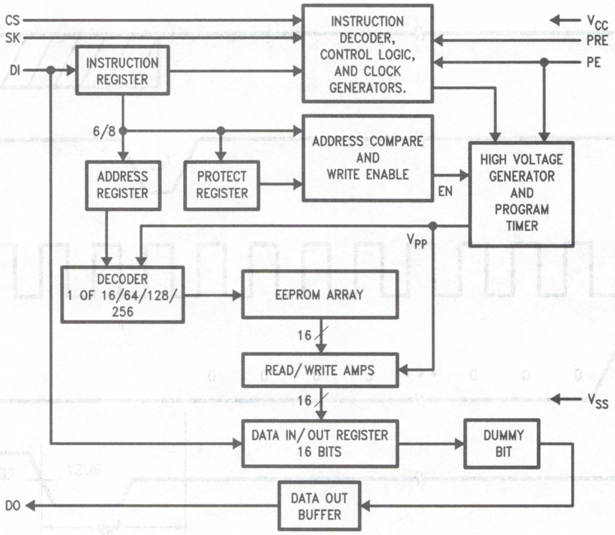
These memories feature a unique EEPROM memory cell which does not require erasing prior to writing, therefore reduces the total number of programming cycles, thus increasing the endurance of the device in actual application. These EEPROM memories are designed for applications requiring 40 years data retention and 100,000 data changes per bit. They are ideal for battery operated applications due to the wide operating voltage range. They are fully functional in all modes of operation across a guaranteed range of 3.0V–5.5V.

Features

- 3.0V to 5.5V guaranteed operating range
- Typical active current 400 μA; typical standby current 25 μA
- Write protection in a user defined section of memory
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during write mode
- 40 year data retention
- 100,000 data changes per bit

*The WRITE ALL instruction is only functional from 4.5V to 5.5V V_{CC}. Its primary purpose is as a test mode.

Block Diagram

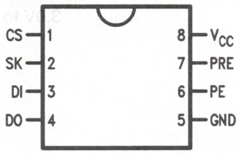

CS
SK
DI
INSTRUCTION REGISTER
INSTRUCTION DECODER, CONTROL LOGIC, AND CLOCK GENERATORS.
V_{CC}
PRE
PE
6/8
ADDRESS REGISTER
PROTECT REGISTER
ADDRESS COMPARE AND WRITE ENABLE
EN
HIGH VOLTAGE GENERATOR AND PROGRAM TIMER
V_{PP}
DECODER 1 OF 16/64/128/256
EEPROM ARRAY
16
READ/WRITE AMPS
16
V_{SS}
DATA IN/OUT REGISTER 16 BITS
DUMMY BIT
DATA OUT BUFFER
DO

TL/D/10044-1

Connection Diagrams

PIN OUT:

Dual-In-Line Package (N)


CS 1
SK 2
DI 3
DO 4
8 V_CC
7 PRE
6 PE
5 GND

TL/D/10044-2

Top View

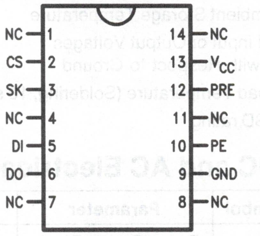
See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

PIN OUT:

SO Package (M)


NC 1
CS 2
SK 3
NC 4
DI 5
DO 6
NC 7
14 NC
13 V_CC
12 PRE
11 NC
10 PE
9 GND
8 NC

TL/D/10044-3

Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NMC93CS06N3/ NMC93CS46N3/NMC93CS56N3/NMC93CS66N3 NMC93CS06M3/ NMC93CS46M3/NMC93CS56M3/NMC93CS66M3

Extended Temp. Range (−40°C to +85°C)

Order Number
NMC93CS06EN3/ NMC93CS46EN3/NMC93CS56EN3/NMC93CS66EN3 NMC93CS06EM3/ NMC93CS46EM3/NMC93CS56EM3/NMC93CS66EM3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC93CSxx	0°C to +70°C
NMC93CSxxE	−40°C to +85°C
Positive Power Supply	3.0V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 3.0V to 5.5V unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
V_{RPP}	Power Supply Ripple		Peak-to-Peak (Note 7)		0.1 V_{CC}	V
I_{CC1}	Operating Current CMOS Input Levels	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	CS = V_{IH}, SK = 1.0 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CSS66E	CS = V_{IH}, SK = 1.0 MHz 4.5V ≤ V_{CC} ≤ 5.5V		3 3	mA
I_{CC3}	Standby Current	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	CS = 0V		50 100	μA
I_{IL}	Input Leakage	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CSS66E	V_{OUT} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V ≤ V_{CC} ≤ 5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		3V ≤ V_{CC} ≤ 4.5V	−0.1 2	0.6 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		3V ≤ V_{CC} ≤ 4.5V I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E		0 0	1 0.5	MHz
t_{SKH}	SK High Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	(Note 2) (Note 3)	500 500		ns
t_{SKL}	SK Low Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	(Note 2) (Note 3)	250 500		ns
t_{CS}	Minimum CS Low Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	(Note 4) (Note 5)	250 500		ns
t_{CSS}	CS Setup Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	Relative to SK	50 100		ns
t_{PRES}	PRE Setup Time	NMC93CS06-NMC93CS66 NMC93CS06E-NMC93CS66E	Relative to SK	50 100		ns
t_{PES}	PE Setup Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	Relative to SK	50 100		ns
t_{DIS}	DI Setup Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	Relative to SK	100 200		ns

DC and AC Electrical Characteristics V_{CC} = 3.0V to 5.5V unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	Relative to CS Relative to CS	250 500		ns
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	Relative to SK	100 200		ns
t_{PD1}	Output Delay to "1"	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	AC Test		500 1000	ns
t_{PD0}	Output Delay to "0"	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	AC Test		500 1000	ns
t_{SV}	CS to Status Valid	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	AC Test		500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	CS = V_{IL} AC Test		100 200	ns
t_{WP}	Write Cycle Time				15	ms
	Endurance		Number of Data Changes per Bit	Typical 100,000		Cycles

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 microsecond. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature parts specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Note 7: Rate of voltage change must be less than 0.5 V/ms.

Capacitance (Note 6)

T_A = 25°C, f = 1MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

The NMC93CSxx family of extended voltage EEPROM have 10 instructions as described below. Note that there is a difference in the length of the instruction for the NMC93CS06 and NMC93CS46 vs. the NMC93CS56 and NMC93CS66. This is due to the fact that the two larger devices require 2 additional address bits which are not required for the smaller devices. Within the two groups of devices the number of address bits remain constant even though in some cases the most significant bit(s) are not used. In every instruction, the first bit is always a "1" and is viewed as a start bit. The next 8 or 10 bits (depending on device size) carry the op code and address. The address is either 6 or 8 bits depending on the device size.

Read (READ):

The Read (READ) instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the NONVOLATILE SHIFT-REGISTER mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). D0 = logical 0 indicates that programming is still in progress. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. Additionally, it is only guaranteed at $V_{CC} = 5.0V \pm 10\%$. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction. Following the PRREAD instruction the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one** time only instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Instruction Set for the NMC93CS06x3 and NMC93CS46x3

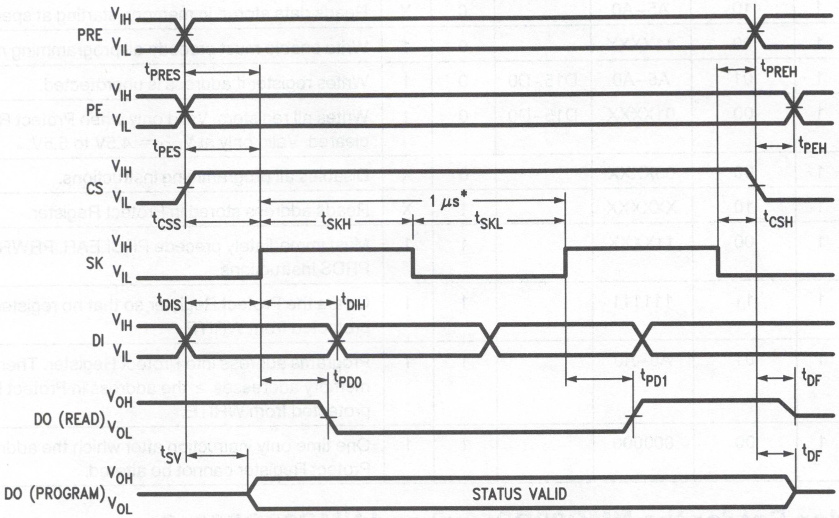
Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared. Valid only at V_{CC} = 4.5V to 5.5V.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Instruction Set for the NMC93CS56x3 and NMC93CS66x3

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared. Valid only at V_{CC} = 4.5V to 5.5V.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Timing Diagrams

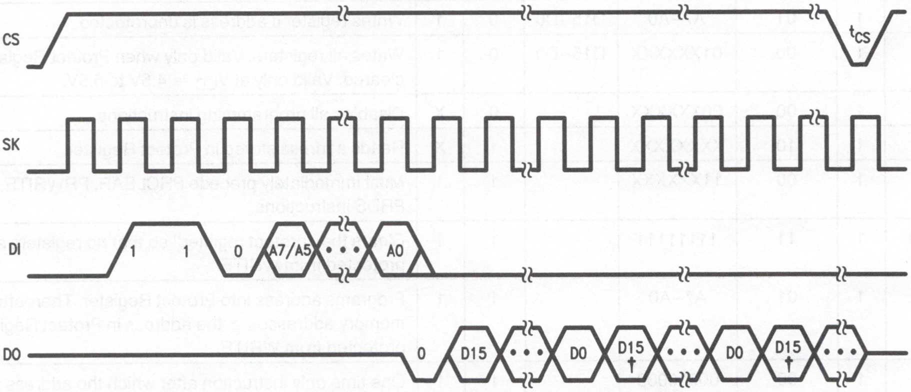
Synchronous Data Timing


PRE
V_{IH}
V_{IL}
t_{PRES}
t_{PREH}
PE
V_{IH}
V_{IL}
t_{PES}
t_{PEH}
CS
V_{IH}
V_{IL}
t_{CSS}
1 µs*
t_{SKH}
t_{SKL}
t_{CSH}
SK
V_{IH}
V_{IL}
t_{DIS}
t_{DIH}
DI
V_{IH}
V_{IL}
t_{PD0}
t_{PD1}
t_{DF}
DO (READ)
V_{OH}
V_{OL}
t_{SV}
t_{DF}
DO (PROGRAM)
V_{OH}
V_{OL}
STATUS VALID

TL/D/10044-4

*This is the minimum SK period (See Note 2).

READ:
PRE = 0, PE = X

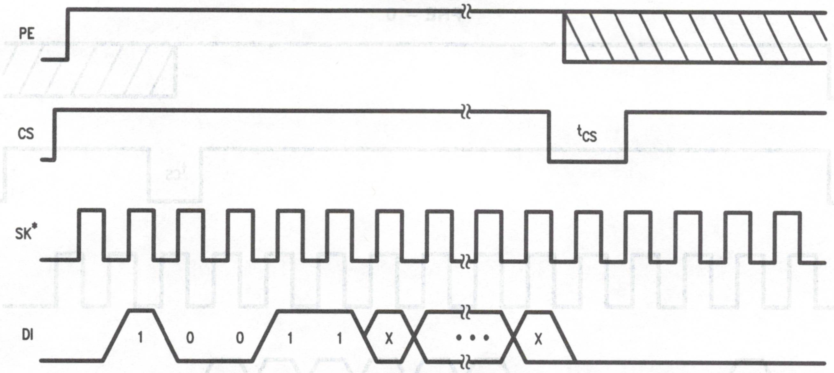

CS
t_{CS}
SK
DI
1
1
0
A7/A5
• • •
A0
DO
0
D15
• • •
D0
D15 †
• • •
D0
D15 †
• • •

TL/D/10044-5

*Address bit A7 becomes "don't care" for NMC93CS56
*Address bits A5 and A4 become "don't cares" for NMC93CS06
†The memory automatically cycles to the next register.

Timing Diagrams (Continued)

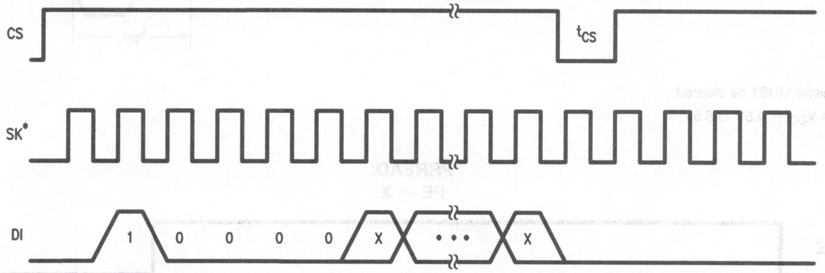
WEN:
PRE = 0, D0 = TRI-STATE


PE
CS
t_{CS}
SK*
DI
1
0
0
1
1
X
• • •
X

TL/D/10044-6

*The NMC93CS56 and NMC93CS66 require a minimum of 11 clocks. The NMC93CS06 and NMC93CS46 require a minimum of 9 clock cycles.

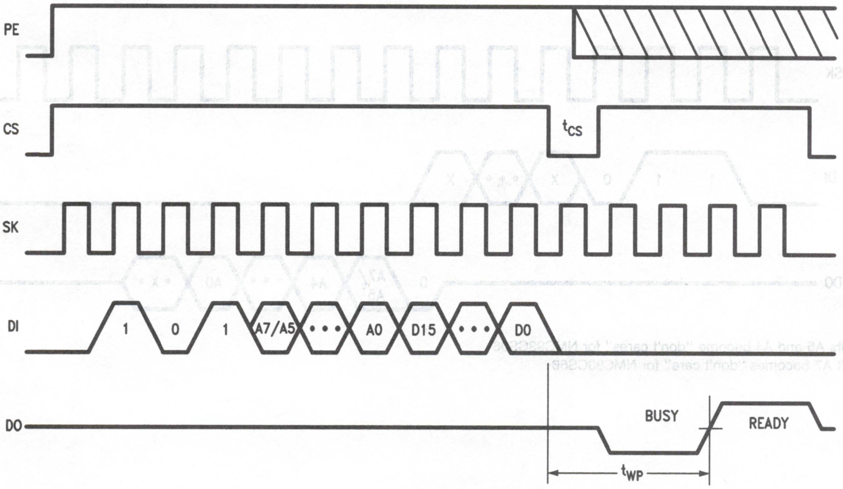
WDS:
PRE = 0, PE = X, DO = TRI-STATE


CS
t_{CS}
SK*
DI
1
0
0
0
0
X
• • •
X

TL/D/10044-7

*The NMC93CS56 and NMC93CS66 require a minimum of 11 clocks. The NMC93CS06 and NMC93CS46 require a minimum of 9 clock cycles.

WRITE:
PRE = 0

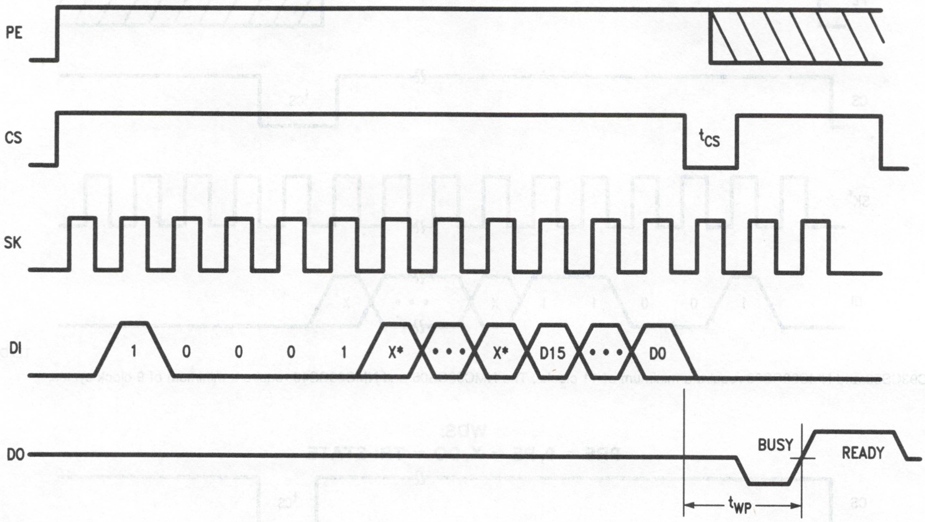

PE
CS
t_{CS}
SK
DI
1
0
1
A7/A5
• • •
A0
D15
• • •
D0
DO
BUSY
READY
t_{WP}

TL/D/10044-8

- Address bit A7 becomes a "don't care" for NMC93CS56
- Address bits A5 and A4 become "don't cares" for NMC93CS06

Timing Diagrams (Continued)

WRALL†:
PRE = 0


PE
CS
SK
DI
DO
1
0
0
0
1
X*
• • •
X*
D15
• • •
D0
t_{CS}
BUSY
READY
t_{WP}

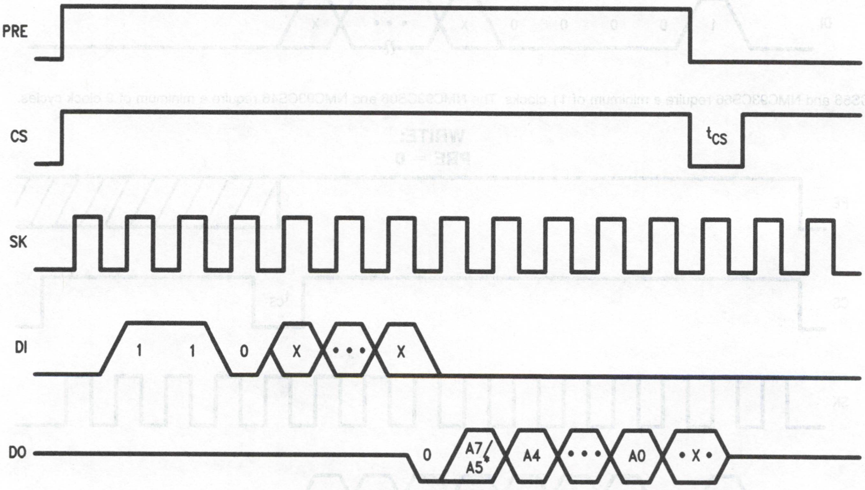
*Don't care

†Protect Register **MUST** be cleared.

†Valid only at V_{CC} = 4.5V to 5.5V.

TL/D/10044-9

PRREAD:
PE = X

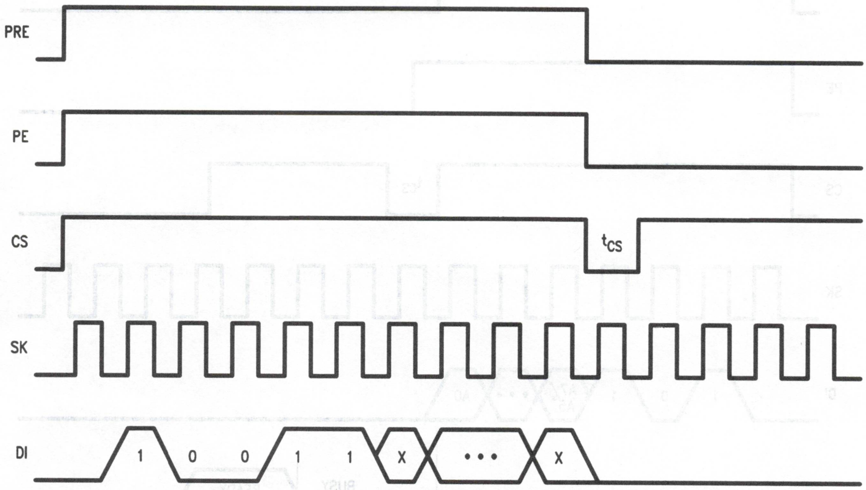

PRE
CS
SK
DI
DO
1
1
0
X
• • •
X
t_{CS}
0
A7/
A5•
A4
• • •
A0
• X •

TL/D/10044-10

•Address bits A5 and A4 become "don't cares" for NMC93CS06
•Address bit A7 becomes "don't care" for NMC93CS56

Timing Diagrams (Continued)

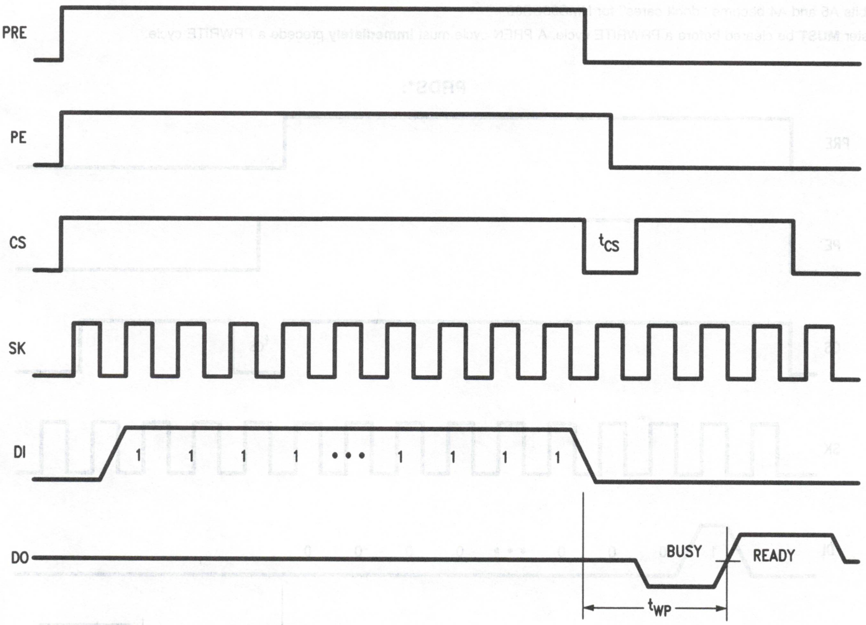
PREN*: D0 = TRI-STATE


PRE
PE
CS
tCS
SK
DI
1
0
0
1
1
X
•••
X

TL/D/10044–11

*A WEN cycle must precede a PREN cycle.

PRCLEAR*:

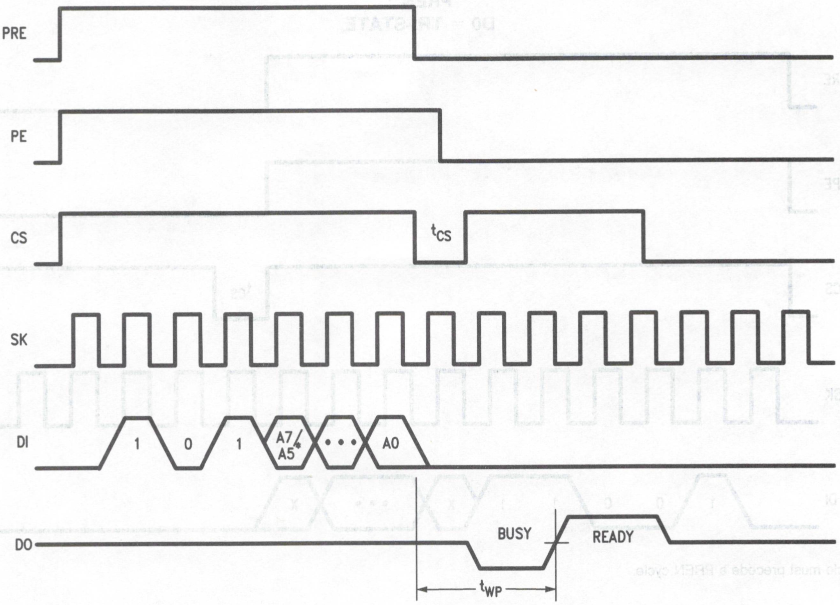

PRE
PE
CS
tCS
SK
DI
1
1
1
1
•••
1
1
1
1
DO
BUSY
READY
tWP

*A PREN cycle must **immediately** precede a PRCLEAR cycle.

TL/D/10044–12

Timing Diagrams (Continued)

PRWRITE†:


PRE
PE
CS
t_{CS}
SK
DI
1
0
1
A7/A5*
• • •
A0
DO
BUSY
READY
t_{WP}

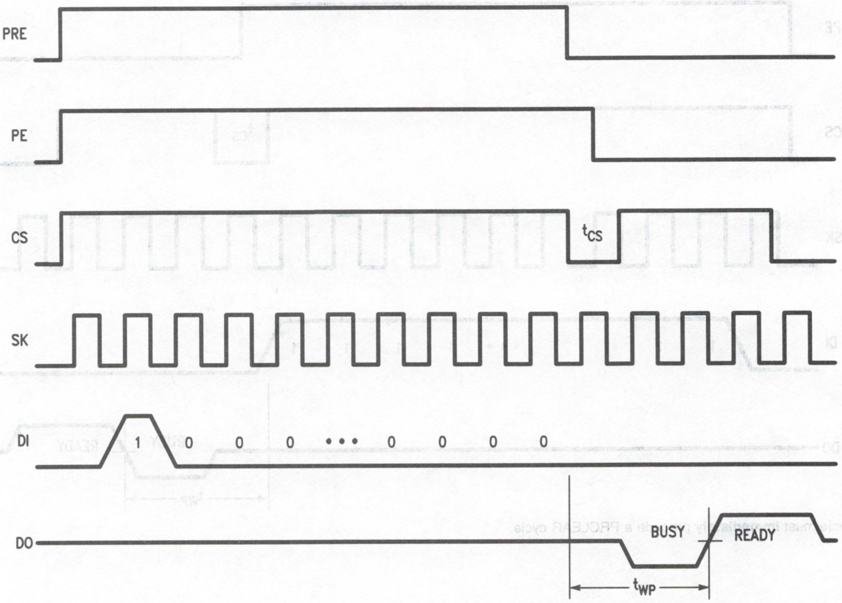
TL/D/10044–13

*Address bit A7 becomes a "don't care" for NMC93CS56

*Address bits A5 and A4 become "don't cares" for NMC93CS06

†Protect Register **MUST** be cleared before a PRWRITE cycle. A PREN cycle must **immediately** precede a PRWRITE cycle.

PRDS*:


PRE
PE
CS
t_{CS}
SK
DI
1
0
0
0
• • •
0
0
0
0
DO
BUSY
READY
t_{WP}

TL/D/10044–14

***ONE TIME ONLY** instruction. A PREN cycle must **immediately** precede a PRDS cycle.

National Semiconductor

PRELIMINARY

NMC93C06x3/C46x3/C56x3/C66x3 Extended Voltage 256-/1024/2048/4096-Bit Serial EEPROM

General Description

The NMC93C06x3/C46x3/C56x3/C66x3 are 256/1024/2048/4096 bits of CMOS electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high speed and low power. They operate from a single 3.0V to 5.5V supply since V_{PP} is generated on-board. The serial organization allow the NMC93C06x3/C46x3/C56x3/C66x3 to be packaged in an 8-pin DIP or 14-pin SO package to save board space.

The memories feature a serial interface with the instruction, address, and write data, input on the Data-In (DI) pin. All read data and device status come out on the Data-Out (DO) pin. A low-to-high transition of shift clock (SK) shifts all data in and out. This serial interface is MICROWIRE™ compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions: Read, Erase/Write Enable, Erase, Erase All*, Write, Write All*, and Erase/Write Disable. The NMC93C06x3/C46x3/C56x3/C66x3 do not require an erase cycle prior to the Write and Write All instructions. The Erase and Erase All instructions are available to maintain complete read and programming capability with the NMOS NMC9346. All programming cycles are completely self-timed for simplified operation. The busy status is available on the DO pin to indicate the completion of a programming cycle. EEPROMs are shipped in the erased state where all bits are logical 1's.

Compatibility with Other Devices

These memories are pin compatible to National Semiconductor's NMOS EEPROMs, NMC9306 and NMC9346 and CMOS EEPROMs NMC93C06x3/C46x3/C56x3/C66x3.

Features

- Typical active current 400 μA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 3.0V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential register read
- 40 years data retention
- 100,000 write cycles

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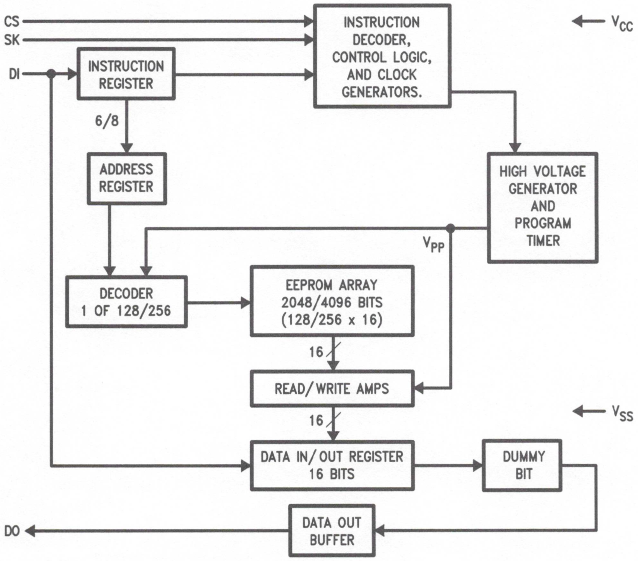
*The instructions Erase All and Write All are functional only from V_{CC} = 4.5V to 5.5V. Their primary purpose is as test modes.

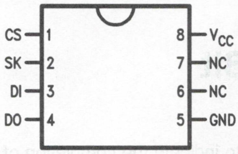
Block Diagram


CS
SK
DI
INSTRUCTION REGISTER
INSTRUCTION DECODER, CONTROL LOGIC, AND CLOCK GENERATORS.
V_{CC}
6/8
ADDRESS REGISTER
HIGH VOLTAGE GENERATOR AND PROGRAM TIMER
V_{PP}
DECODER 1 OF 128/256
EEPROM ARRAY 2048/4096 BITS (128/256 x 16)
16
READ/WRITE AMPS
V_{SS}
16
DATA IN/OUT REGISTER 16 BITS
DUMMY BIT
DO
DATA OUT BUFFER

TL/D/10045–1

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)


CS 1
SK 2
DI 3
DO 4
8 V_{CC}
7 NC
6 NC
5 GND

TL/D/10045-2

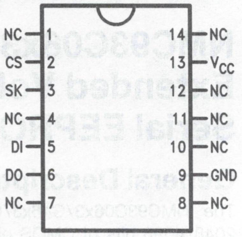
Top View

See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

14-Pin SO Package (M)


NC 1
CS 2
SK 3
NC 4
DI 5
DO 6
NC 7
14 NC
13 V_{CC}
12 NC
11 NC
10 NC
9 GND
8 NC

TL/D/10045-3

Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NMC93C06N3 NMC93C46N3/NMC93C56N3/NMC93C66N3 NMC93C46M3/NMC93C56M3/NMC93C66M3 NMC93C06M83/NMC93C46M83

Extended Temp. Range (−40°C to +85°C)

Order Number
NMC93C06EN3 NMC93C46EN3/NMC93C56EN3/NMC93C66EN3 NMC93C46EM3/NMC93C56EM3/NMC93C66EM3 NMC93C06EM83/NMC93C46EM83

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC93C56–NMC93C66	0°C to +10°C
NMC93C56E–NMC93C66E	−40°C to +85°C
Positive Power Supply	3.0V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 3.0V to 5.5V (unless otherwise specified)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	CS = V_{IH}, SK = 0.5 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	CS = V_{IH}, SK = 0.5 MHz		3 3	mA
I_{CC3}	Standby Current	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	CS = 0V		50 100	μA
I_{IL}	Input Leakage	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V ≤ V_{CC} ≤ 5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		3V ≤ V_{CC} ≤ 4.5V	−0.1 2	0.6 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	 0.4	 V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		3V ≤ V_{CC} ≤ 4.5V I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	 0.2	 V V
f_{SK}	SK Clock Frequency	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E		0 0	1 0.5	MHz
t_{SKH}	SK High Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	(Note 2) (Note 3)	500 500		ns
t_{SKL}	SK Low Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	(Note 2) (Note 3)	250 500		ns
t_{CS}	Minimum CS Low Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	(Note 4) (Note 5)	250 500		ns
t_{CSS}	CS Setup Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	Relative to SK	50 100		ns
t_{PRES}	PRE Setup Time	NMC93CS06-NMC93CS66 NMC93CS06E-NMC93CS66E	Relative to SK	50 100		ns
t_{PES}	PE Setup Time	NMC93CS06-NMC93CS66 NMC93CS06E-NMC93CS66E	Relative to SK	50 100		ns

DC and AC Electrical Characteristics V_{CC} = 3.0V to 5.5V (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	Relative to SK	100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	Relative to SK	100 200		ns
t_{PD1}	Output Delay to "1"	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	AC Test		500 1000	ns
t_{PD0}	Output Delay to "0"	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	AC Test		500 1000	ns
t_{SV}	CS to Status Valid	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	AC Test		500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	AC Test CS = V_{IL}		100 200	ns
t_{WP}	Write Cycle Time				15	ms
	Endurance		Number of Data Changes per Bit	Typical 100,000		Cycles

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 2 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 μs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 1750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature parts specifies a minimum SK clock period of 2 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Capacitance (Note 6)

T_A = 25°C f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

The NMC93C06/C46/C56/C66 have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 10-bits carry the op code and the 8-bit address for register selection.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

Write All (WRAL):

The (WRAL) instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

Erase/Write Disable (EWDS):

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Instruction Set for the NMC93C06 and NMC93C46

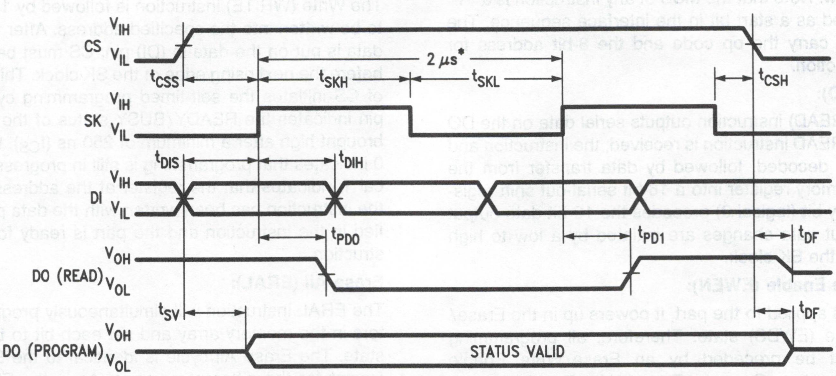
Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, at specified address.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erases all registers. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXX	D15–D0	Writes all registers. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXX		Disables all programming instructions.

Instruction Set for the NMC93C56 and NMC93C66

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
ERASE	1	11	A7–A0		Erase register A7A6A5A4A3A2A1A0.
ERAL	1	00	10XXXXXX		Erases all registers. Valid only at V_{CC} = 4.5V to 5.5V.
WRITE	1	01	A7–A0	D15–D0	Writes register if address is unprotected.
WRAL	1	00	01XXXXXX	D15–D0	Writes all registers. Valid only when Protect Register is cleared. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXXXX		Disables all programming instructions.

Timing Diagrams

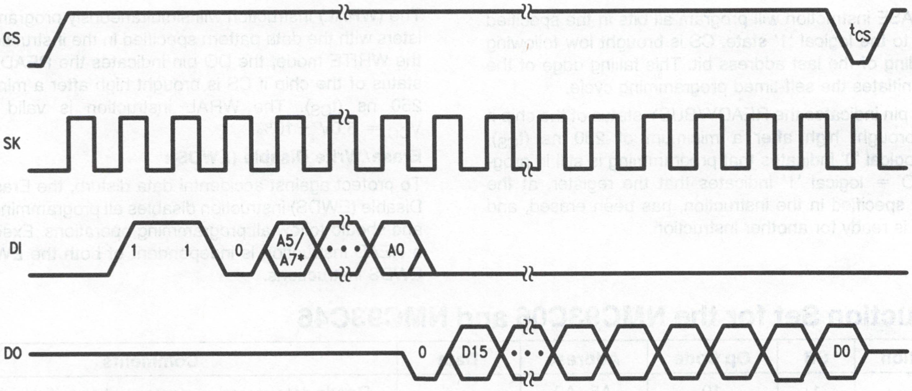
Synchronous Data Timing


V_{IH}
CS
V_{IL}
t_{CSS}
t_{SKH}
2 μs*
t_{SKL}
t_{CSH}
V_{IH}
SK
V_{IL}
t_{DIS}
t_{DIH}
V_{IH}
DI
V_{IL}
t_{PD0}
t_{PD1}
t_{DF}
V_{OH}
DO (READ)
V_{OL}
t_{SV}
t_{DF}
V_{OH}
DO (PROGRAM)
V_{OL}
STATUS VALID

TL/D/10045–4

*This is the minimum SK period (Note 2).

READ:

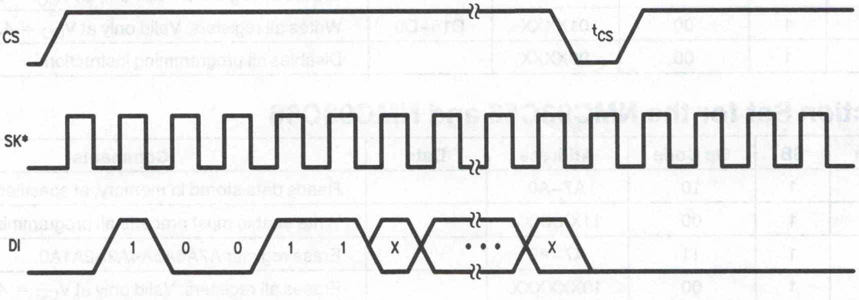

CS
t_{CS}
SK
DI
1
1
0
A5/
A7*
• • •
A0
DO
0
D15
• • •
D0

TL/D/10045–5

*Address bits A_5 and A_4 become "don't care" for NMC93C06.

*Address bit A_7 becomes a "don't care" for NMC93C56.

EWEN:

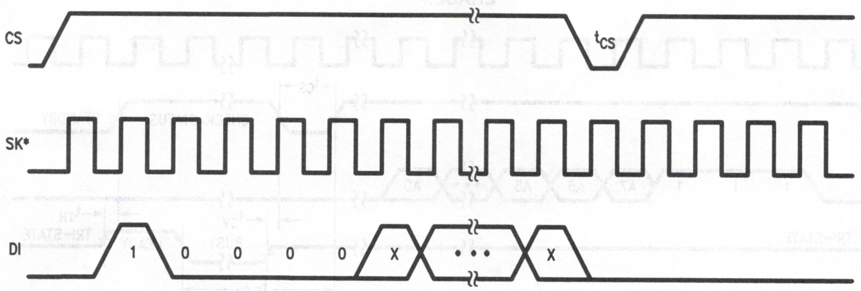

CS
t_{CS}
SK*
DI
1
0
0
1
1
X
• • •
X

TL/D/10045–6

*The NMC93C56 and NMC93C66 require a minimum of 11 clocks. The NMC93C06 and NMC93C46 require a minimum of 9 clock cycles.

Timing Diagrams (Continued)

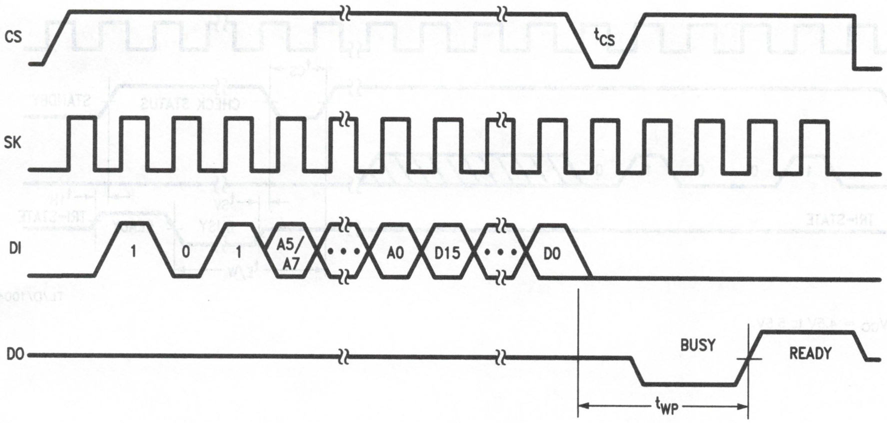
EWDS:


CS
t_{CS}
SK*
DI
1
0
0
0
0
X
• • •
X

TL/D/10045-7

*The NMC93C56 and NMC93C66 require a minimum of 11 clocks. The NMC93C06 and NMC93C46 require a minimum of 9 clock cycles.

WRITE:

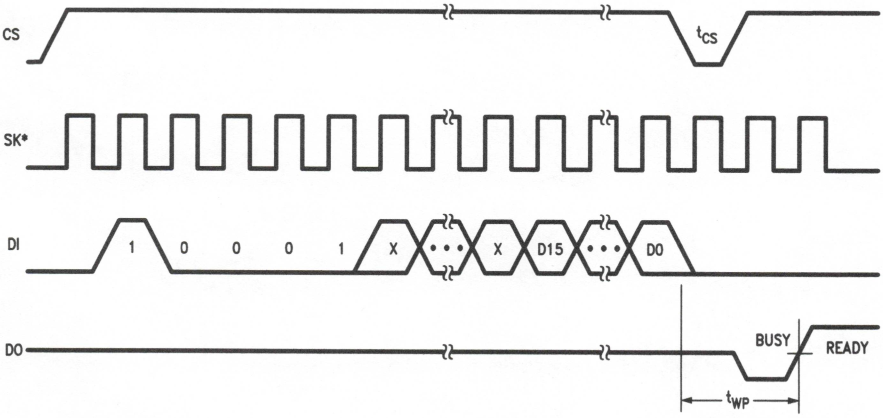

CS
t_{CS}
SK
DI
1
0
1
A5/
A7
• • •
A0
D15
• • •
D0
DO
BUSY
READY
t_{WP}

TL/D/10045-8

*Address bit A_5 and A_4 become "don't care" for NMC93C06.

*Address bit A_7 becomes a "don't care" for NMC93C56.

WRAL:†


CS
t_{CS}
SK*
DI
1
0
0
0
1
X
• • •
X
D15
• • •
D0
DO
BUSY
READY
t_{WP}

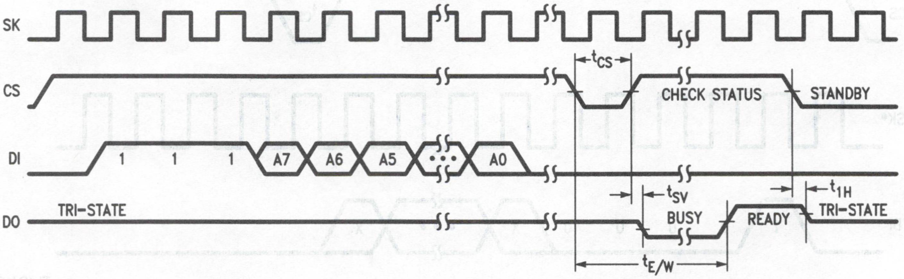
TL/D/10045-9

*The NMC93C56 and NMC93C66 require a minimum of 11 clocks. The NMC93C06 and NMC93C46 require a minimum of 9 clock cycles.

†Valid only at V_{CC} = 4.5V to 5.5V.

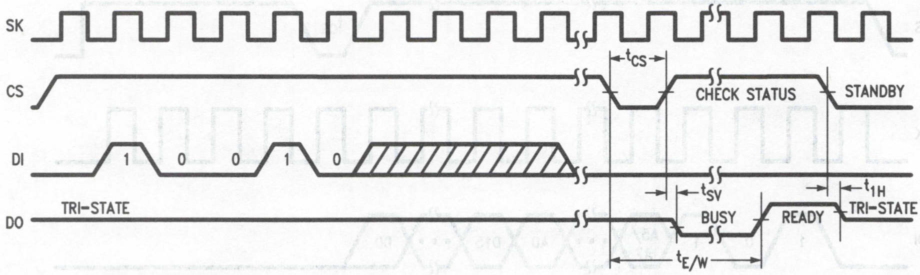
Timing Diagrams (Continued)

ERASE:


SK
CS
DI
DO
tCS
CHECK STATUS
STANDBY
1
1
1
A7
A6
A5
A0
tSV
t1H
TRI-STATE
BUSY
READY
TRI-STATE
tE/W

TL/D/10045–10

ERAL:†


SK
CS
DI
DO
tCS
CHECK STATUS
STANDBY
1
0
0
1
0
tSV
t1H
TRI-STATE
BUSY
READY
TRI-STATE
tE/W

TL/D/10045–11

†Valid only at V_{CC} = 4.5V to 5.5V.

National Semiconductor

PRELIMINARY

NMC95C12 1024-Bit CMOS EEPROM with DIP Switches

General Description

The NMC95C12 is a 1024-bit, CMOS EEPROM with 8 programmable outputs that can be used as DIP switches. The 1024 bits of memory are divided into 64 registers of 16 bits each and each register can be individually accessed. Registers 61–63 are dedicated to storing the switch settings.

In addition to the 1024 bits of EEPROM memory, the NMC95C12 contains eight individually programmable outputs which can be used as DIP switches. Each output may be programmed to provide either a High or Low level. These outputs may also be programmed to form four individual pairs of SPST switches.

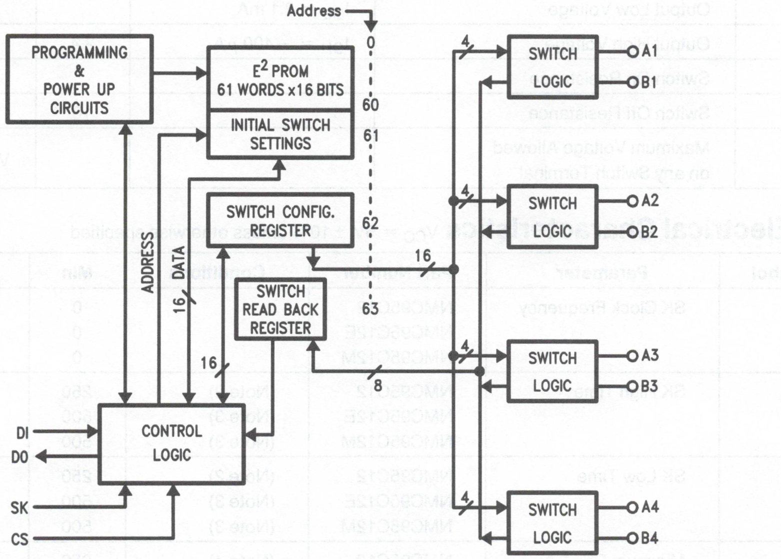
The switch configuration information is obtained from a non volatile register whenever power is first applied to the device. This ensures the switches will always have a user determined state upon power-up.

The NMC95C12 is designed to meet applications requiring 40,000 write cycles per register and at least 10 year data retention.

Features

- 1024 bits of CMOS EEPROM memory
- 8 DIP switch positions or 4 SPST switch positions
- 4 mA (max) operating current, 50 μA (max) standby current
- Software write protection
- Serial I/O interface fully MICROWIRE compatible
- Single +5V ±10% operation
- 14-pin DIP or SO package availability
- 40,000 write operations
- 10 year data retention
- Reliable floating gate technology
- Sequential register read
- Self-timed write cycle
- Erase cycles not necessary
- Compatible with COPS™ microcontrollers

Block Diagram


Address
0
60
61
62
63
PROGRAMMING & POWER UP CIRCUITS
E² PROM 61 WORDS x 16 BITS
INITIAL SWITCH SETTINGS
SWITCH CONFIG. REGISTER
SWITCH READ BACK REGISTER
ADDRESS
DATA
16
16
16
8
4
4
4
4
CONTROL LOGIC
DI
DO
SK
CS
SWITCH LOGIC
A1
B1
SWITCH LOGIC
A2
B2
SWITCH LOGIC
A3
B3
SWITCH LOGIC
A4
B4

TL/D/9632–1

FIGURE 1. Block Diagram

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	6.5V
Voltage at Any Pin	−0.3 to +6.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation @25°C	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature

NMC95C12	0°C to +70°C
NMC95C12E	−40°C to +85°C
NMC95C12M*	−55°C to +125°C
Power Supply Voltage	4.5V to 5.5V

*Contact factory for availability

DC Electrical Characteristics V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	$C_S = V_{IH}$, SK = 1 MHz		4	mA
I_{CC2}	Operating Current TTL Input Levels	$C_S = V_{IH}$, SK = 1 MHz		6	mA
I_{CC3}	Standby Current CMOS Input Levels on Switches	C_S = 0V		50	μA
I_{CC4}	Standby Current TTL Input Levels on Switches	C_S = 0V		800	μA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}	−2.5	+2.5	μA
I_{OL}	Output Leakage	V_{OUT} = 0V to V_{CC}	−2.5	2.5	μA
V_{IL}	Input Low Voltage		−0.1	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA	2.4		V
R_{ON}	Switch On Resistance			200	Ω
R_{OFF}	Switch Off Resistance		10		MΩ
V_S	Maximum Voltage Allowed on any Switch Terminal			V_{CC} + 1	V

AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
f_{SK}	SK Clock Frequency	NMC95C12 NMC95C12E NMC95C12M		0 0 0	1 0.5 0.5	MHz
t_{SKH}	SK High Time	NMC95C12 NMC95C12E NMC95C12M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{SKL}	SK Low Time	NMC95C12 NMC95C12E NMC95C12M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{CS}	Minimum CS Low Time	NMC95C12 NMC95C12E NMC95C12M	(Note 4) (Note 5) (Note 5)	250 500 500		ns
t_{CSS}	CS Setup Time	NMC95C12 NMC95C12E NMC95C12M	Relative to SK	50 100 100		ns

AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NMC95C12 NMC95C12E NMC95C12M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC95C12 NMC95C12E NMC95C12M	Relative to SK	100 200 200		ns
t_{PD1}	Output Delay to "1"	NMC95C12 NMC95C12E NMC95C12M	AC Test		500 1000 1000	ns
t_{PD0}	Output Delay to "0"	NMC95C12 NMC95C12E NMC95C12M	AC Test		500 1000 1000	ns
t_{SV}	CS to Status Valid	NMC95C12 NMC95C12E NMC95C12M	AC Test		500 1000 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC95C12 NMC95C12E NMC95C12M	CS = V_{IL} AC Test		100 200 200	ns
t_{ISWD}	Switch Delay from Switch Input	NMC95C12 NMC95C12E NMC95C12M	AC Test		250 500 500	ns
t_{SWPD0}	Switch Delay to 0 from Config. Change	NMC95C12 NMC95C12E NMC95C12M	AC Test		500 1000 1000	ns
t_{SWPD1}	Switch Delay to 1 from Config. Change	NMC95C12 NMC95C12E NMC95C12M	AC Test		500 1000 1000	ns
t_{SWS}	A1–A4, B1–B4 Setup Time	NMC95C12 NMC95C12E NMC95C12M		100 200 200		ns
t_{SWH}	A1–A4, B1–B4 Hold Time	NMC95C12 NMC95C12E NMC95C12M		100 200 200		ns
t_{WP}	Write Cycle Time				10	ms
	Endurance		Number of Data Changes per Bit	Typical 40,000		Cycles

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", the device should not be operated at these limits. The table of "Electrical Characteristics" provides actual operating limits.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 µs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 µs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 µs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 µs. For example, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 µs in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Note 7: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from +65°C to +85°C.

Capacitance (Note 6)

T_A = 25°C, f = 1 MHz

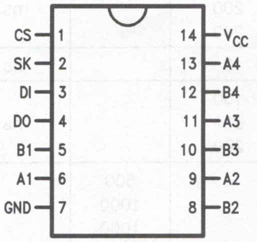
Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Connection Diagrams

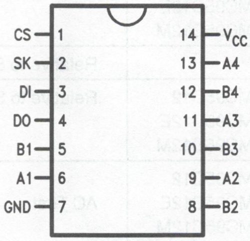
SO Package



TL/D/9632-3

Top View
Order Number NMC95C12M,
NMC95C12EM and NMC95C12MM
See NS Package M14A

Dual-In-Line Package



TL/D/9632-2

Top View
Order Number NMC95C12N,
NMC95C12EN and NMC95C12MN
See NS Package N14A

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
A1–A4	Switch Terminals
B1–B4	Switch Terminals

Pin Descriptions

Pin Name	Description
CS	Chip Select, Input—This input must be high while communicating with the NMC95C12. When this input is LOW, the chip is powered down into the standby mode. It should be noted that the CS does not control the A1 through A4 and B1 through B4 outputs and hence has no effect on them. The CS input must be made LOW after completing an instruction to prepare the control logic to accept the next instruction. If the CS input becomes LOW prematurely, the operation in progress is aborted. If programming the E^2 memory is in progress and the CS goes LOW, the programming is not aborted but will proceed to its normal completion.
SK	Serial Clock, Input—This input is used for clocking the serial I/O. The CS input must be high for clocking to have any effect. Information presented on the DI input will be shifted into the device on the LOW to HIGH transition of the clock. Information from the device will be available on the DO output serially, in response to the LOW to HIGH transition of the clock.
DI	Serial Data In, Input—All information needed for the operation of the device is entered serially from this input. HIGH represents logic '1' and LOW represents logic '0'. The entry order is most significant bit first and least significant bit last.
DO	Serial Data Out, Output, 3-state—When data is read, data from the addressed location will be available on this output serially, in sync with the LOW to HIGH transitions on the SK input. Normally the DO pin is in high impedance state. During a read instruction, when the last bit of the address is shifted in, the DO will go LOW indicating that data will follow. The data will follow in response to the clock transitions. The data will come out most significant bit first and least significant bit last. During E^2 programming operations, this output is also used as the status indicator. During programming operations, LOW indicates Busy (programming in progress) and HIGH indicates Ready. The DO output will be in the high impedance state if the CS input is LOW unconditionally.
A1–A4 B1–B4	Switch Terminals—These pins provide the simulated DIP switch features and hence are called terminals. The behavior of these pins is determined by the settings in the Switch Configuration Register and are independent of the CS input.
V_{CC}	+5V Power Supply.
GND	Ground.

Functional Description

Figure 1 is a block diagram of the NMC95C12. It consists of a 62-word X 16-bit E^{2}PROM array, a 16-bit Switch Configuration Register (SCR), a 16-bit Switch Readback Register (SRR), four identical blocks of switch logic, programming and power-up circuits and the necessary control logic. It may be noted that only eight bit positions of the SRR are used in the NMC95C12.

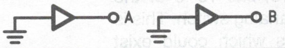
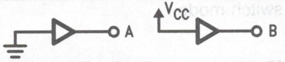
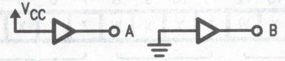
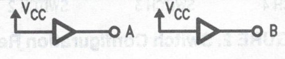
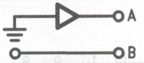
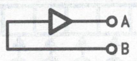
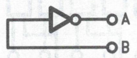
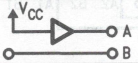
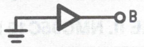
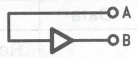
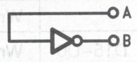
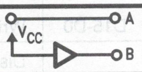
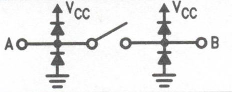
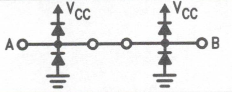
ADDRESS SPACE

Registers 0–60 of the E^{2}PROM are available to the user as general purpose non-volatile memory. Data may be read or programmed into this memory using the appropriate instructions. Address location 61 is an E^2 location which also can be read or programmed like any other E^2 location. However, address 61 is used in the NMC95C12 to provide the initial switch configuration information automatically on power-up. The SCR is located at address 62. The SCR is not an E^2 location and hence is volatile. It does not have endurance limits or programming time requirements associated with it, allowing the switches to be reconfigured an unlimited number of times.

The SCR is automatically loaded from address 61 on power-up. The SCR controls the switch logic and hence the behavior of the terminals A1 through A4 and B1 through B4.

Located at address 63 is the Switch Readback Register (SRR). This is a read only register.

TABLE I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = Tristate
5	0	1	0	1		A = B
6	0	1	1	0		A = B̄
7	0	1	1	1		A = 1 , B = Tristate
8	1	0	0	0		A = Tristate , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		B = Ā
11	1	0	1	1		A = Tristate , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

TL/D/9632–6

*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

Functional Description (Continued)

SWITCH CONFIGURATIONS

The 16-bit SCR format is shown in *Figure 2*. It consists of four 4-bit fields. Each field controls its corresponding switch control logic. The individual bits in each field are labelled W, X, Y, and Z. Table I shows the relationship between these bit values and the resulting behavior of the terminals. It should be remembered that the CS input has no effect on the behavior of the terminals.

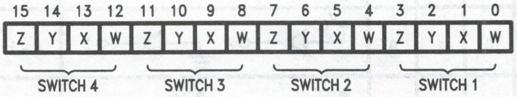
SWITCH READBACK REGISTER

The SRR allows the current logic level present at the switch terminals to be read back via the Microwire bus. The SRR is loaded by the rising edge of SK immediately after the last instruction bit is clocked in (The same clock edge that loads A0). The SRR is loaded on this clock edge only when register 63 (Switch Readback Register) is being read. In the case of switch mode 13 (Analog switch mode), the SRR will not report the actual levels present at the terminals due to this mode being analog levels. In mode 13, bits 15–8 of the SRR will be all 0's to indicate a closed analog switch. This is done to avoid ambiguous logic levels which could exist when the device is used in the analog switch mode.

The bit assignments and conceptual function of the SRR is shown in *Figure 3*. As shown, only bits 15 thru 8 are used, and bits 7 thru 0 are always read as logical 0. The SRR is a Read-Only register and if it is written, the device will not perform a write or generate a Ready/Busy status. The SRR is not implemented in EEPROM, allowing an infinite number of cycles in the register.

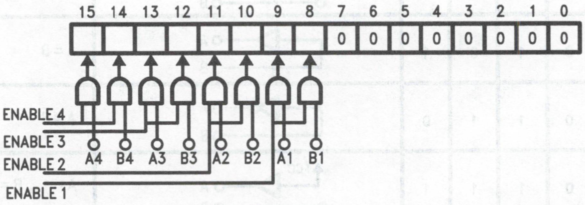
INSTRUCTION SET

The NMC95C12 instruction set contains five instructions, and each instruction is nine bits long. One SK clock cycle is necessary, after CS equals logical "1", before an instruction can be loaded. The first bit of the instruction is the start bit (SB) and is always a logical "1", followed by the op code (2 bits) and the address field (6 bits). The WRITE and WRALL instructions are followed by sixteen bits of data (D15–D0) which is written into the memory. Table II is a list of the instructions and their format.



TL/D/9632–4

FIGURE 2. Switch Configuration Register (SCR)



TL/D/9632–5

FIGURE 3. Switch Readback Register (SRR)

TABLE II. NMC95C12 Instructions

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	Writes register.
WRALL	1	00	01XXXX	D15-D0	Writes all registers.
WDS	1	00	00XXXX		Disables all programming instructions.

Functional Description (Continued)

WDS (Write Disable): When this instruction is issued, all subsequent writing into the NMC95C12 is locked out. Any attempt to write into a locked device is ignored. The NMC95C12 powers up in the locked state. The WEN is the only instruction that unlocks the device. The write disable operation has no effect on read operations. Thus reading will occur normally even from a locked device.

WRALL (Write All): When this instruction is executed, the NMC95C12 bulk-programs the same 16-bit data pattern into all of its E^2 memory locations (address 0 through 61). The SCR is unaffected since it is not an E^2 location. The data pattern must follow immediately after the last bit of this instruction. The chip enters into the self-timed program mode after CS is brought low, before the next rising edge of SK.

WEN (Write Enable): This instruction is used to unlock the write circuits. The circuits will remain unlocked until the WDS instruction locks them. The NMC95C12 powers up in the locked state and hence WEN must be executed prior to any programming instructions.

WRITE (Write/Program): This instruction writes a 16-bit data word into the address location specified by the A_0–A_5 bits of the instruction. The 16 data bits must follow the last bit of the instruction. After loading the WRITE instruction and the 16-bit data, the chip enters into the self-timed program mode when CS is brought low before the next rising edge of the SK clock. If the addressed location is the SCR, then the chip does not enter into the self-timed E^2 programming mode (the SCR is not an E^2 location) but loads the switch configuration data into the SCR. The WRITE instruction can only be aborted by deselecting the chip (CS LOW) before entering all the instruction bits. The NMC95C12 does not require erasing prior to writing.

READ (Read): This instruction reads the data from the addressed location. As before, the instruction also contains the address. The data will come out serially on the D0 output on the rising edge of the clock. A logical '0' precedes the 16-bit data (dummy bit).

The NMC95C12 has a convenient feature called sequential register read. Normally, the CS input is made LOW after the last data bit is shifted out. However, if the CS input is left HIGH and clocking continues, data from the next address location will be delivered on the D0 pin. This sequential read can continue indefinitely whereby the address is automatically incremented after delivering 16 bits of data. It should be noted that in the sequential register read mode, address wrap-around will occur.

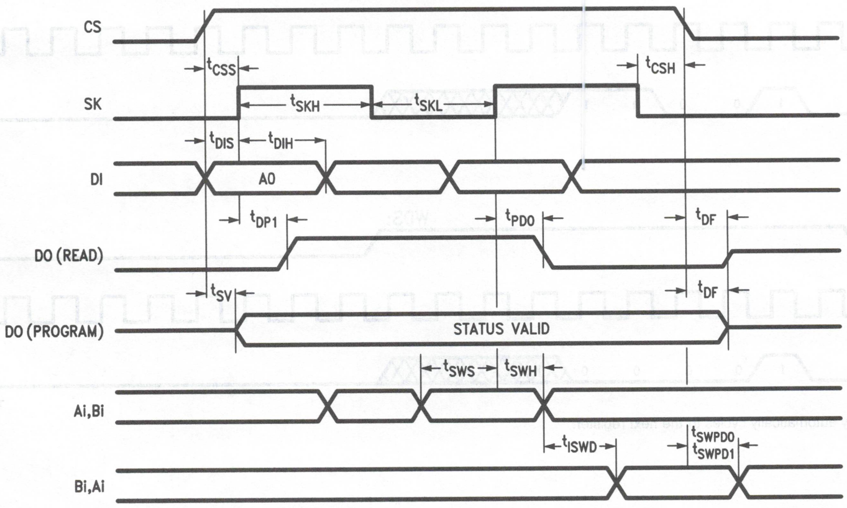
During a sequential register read there will be a dummy bit preceding the first word read, after which, the bit stream will be continuous without any dummy bits separating the data words.

Ready/Busy Indication

Programming an E^2 memory takes several milliseconds. Unlike some devices which require the user to keep track of the elapsed time to ensure completion of the programming cycle, the NMC95C12 contains an on-chip timer. The timer starts when the CS input goes LOW after the last data bit is entered. After entering a programming cycle (CS forced LOW), the timer status may be observed by forcing the CS input back HIGH. The timer status is available on the D0 pin if the CS input is forced HIGH within one ms of starting the programming cycle. LOW on the D0 pin indicates that the programming is still in progress while HIGH indicates the device is READY for the next instruction. It should be noted that if the CS input is made HIGH for status observation, it must be made LOW when READY is indicated before loading the next instruction.

Timing Diagrams

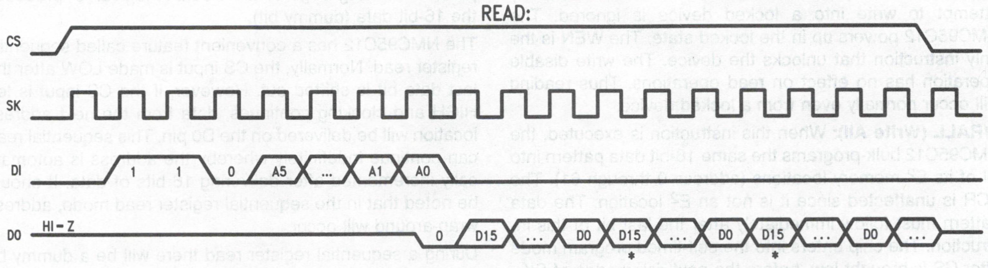
Synchronous Data Timing



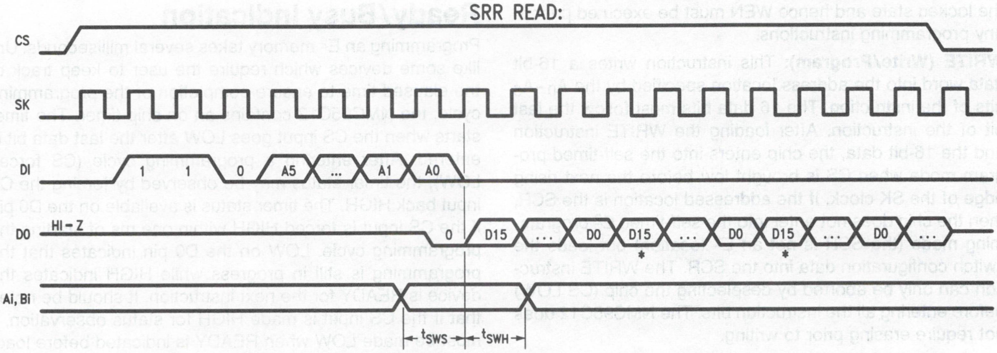
TL/D/9632-7

Timing Diagrams (Continued)

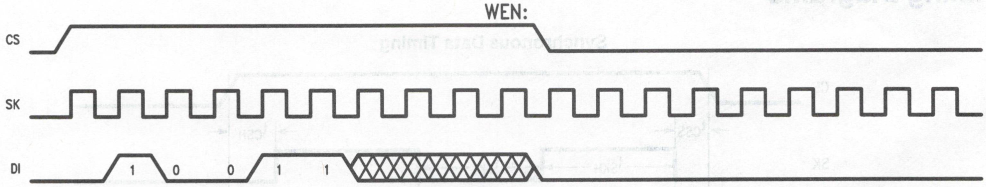
Instruction Sequence


READ:
CS
SK
DI
1
1
0
A5
...
A1
A0
DO
HI-Z
0
D15
...
D0
D15
...
D0
D15
...
D0
...
*
*

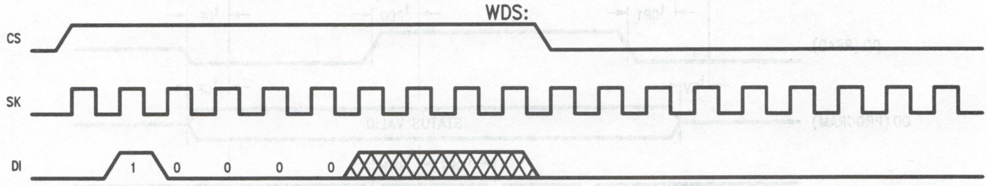
TL/D/9632-8


SRR READ:
CS
SK
DI
1
1
0
A5
...
A1
A0
DO
HI-Z
0
D15
...
D0
D15
...
D0
D15
...
D0
Ai, Bi
t_{SWS}
t_{SWH}
*
*

TL/D/9632-14


WEN:
CS
SK
DI
1
0
0
1
1

TL/D/9632-9

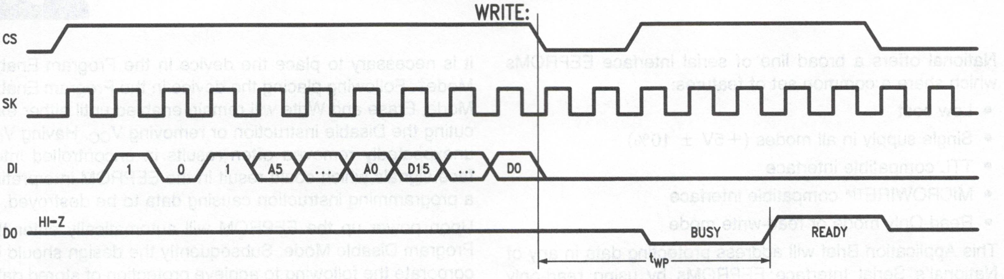

WDS:
CS
SK
DI
1
0
0
0
0

TL/D/9632-10

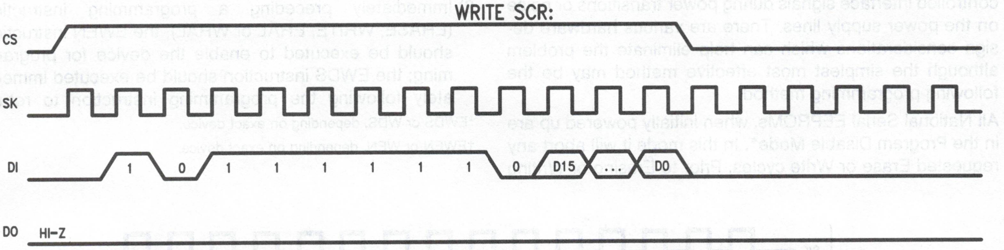
*The memory automatically cycles to the next register.

Timing Diagrams (Continued)

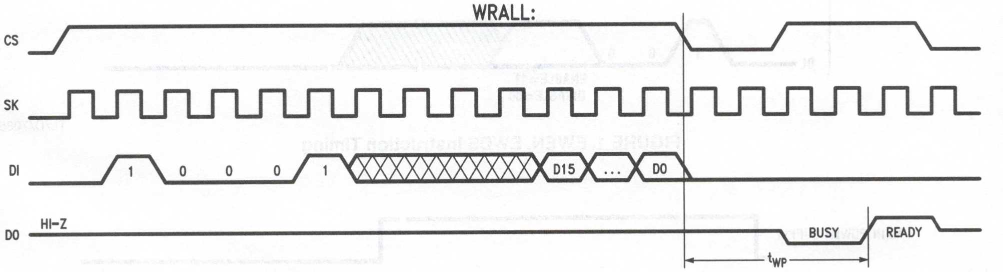
Instruction Sequence (Continued)


WRITE:
CS
SK
DI
1
0
1
A5
...
A0
D15
...
D0
DO
HI-Z
BUSY
READY
t_{WP}

TL/D/9632-11


WRITE SCR:
CS
SK
DI
1
0
1
1
1
1
1
1
0
D15
...
D0
DO
HI-Z

TL/D/9632-12


WRALL:
CS
SK
DI
1
0
0
0
1
D15
...
D0
DO
HI-Z
BUSY
READY
t_{WP}

TL/D/9632-13

Protecting Data in Serial EEPROMs

National Semiconductor
Application Brief 15
Paul Lubeck

National offers a broad line of serial interface EEPROMs which share a common set of features:

- Low cost
- Single supply in all modes (+5V ± 10%)
- TTL compatible interface
- MICROWIRE™ compatible interface
- Read-Only mode or read-write mode

This Application Brief will address protecting data in any of National's Serial Interface EEPROMs by using read-only mode.

Whereas EEPROM is non-volatile and does not require V_{CC} to retain data, the problem exists that stored data can be destroyed during power transitions. This is due to either uncontrolled interface signals during power transitions or noise on the power supply lines. There are various hardware design considerations which can help eliminate the problem although the simplest most effective method may be the following programming method.

All National Serial EEPROMs, when initially powered up are in the Program Disable Mode*. In this mode it will abort any requested Erase or Write cycles. Prior to Erasing or Writing it is necessary to place the device in the Program Enable Mode†. Following placing the device in the Program Enable Mode, Erase and Write will remain enabled until either executing the Disable instruction or removing V_{CC}. Having V_{CC} unexpectedly removed often results in uncontrolled interface signals which could result in the EEPROM interpreting a programming instruction causing data to be destroyed.

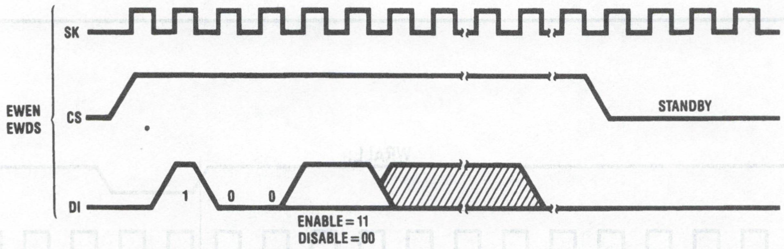
Upon power up the EEPROM will automatically enter the Program Disable Mode. Subsequently the design should incorporate the following to achieve protection of stored data.

1) The device powers up in the read-only mode. However, as a backup, the EWDS instruction should be executed as soon as possible after V_{CC} to the EEPROM is powered up to ensure that it is in the read-only mode.

2) Immediately preceding a programming instruction (ERASE, WRITE, ERAL or WRAL), the EWEN instruction should be executed to enable the device for programming; the EWDS instruction should be executed immediately following the programming instruction to return

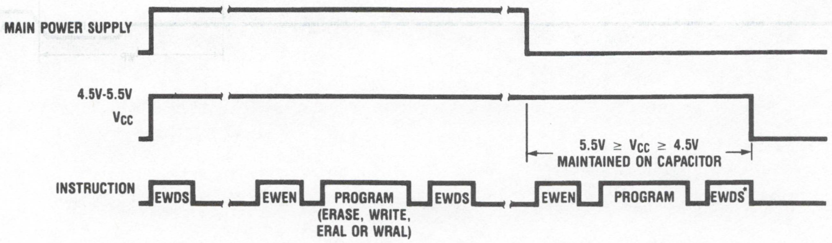
*EWDS or WDS, depending on exact device.

†EWEN or WEN, depending on exact device.



TL/D/7085-1

FIGURE 1. EWEN, EWDS Instruction Timing



TL/D/7085-2

*EWDS must be executed before V_{CC} drops below 4.5V to prevent accidental data loss during subsequent power down and/or power up transients.

FIGURE 2. Typical Instruction Flow for Maximum Data Protection

the device to the read-only mode and protect the stored data from accidental disturb during subsequent power transients or noise.

3) Special care must be taken in designs in which programming instructions are initiated to store data in the EEPROM after the main power supply has gone down. This is usually accomplished by maintaining V_{CC} for the EEPROM and its controller on a capacitor for a sufficient amount of time (approximately 50 ms, depending on the clock rate) to complete these operations. This capacitor must be large enough to maintain V_{CC} between 4.5 and 5.5 volts for the total duration of the store operation, INCLUDING the execution of the EWDS instruction immediately following the last programming instruction. FAILURE TO EXECUTE THE LAST EWDS INSTRUCTION BEFORE V_{CC} DROPS BELOW 4.5 VOLTS MAY CAUSE INADVERTENT DATA DISTURB DURING SUBSEQUENT POWER DOWN AND/OR POWER UP TRANSIENTS.

Electronic Compass Calibration Made Easy With E^2 Memory, NMC9306

National Semiconductor
Application Brief 18
Doug Zrebski

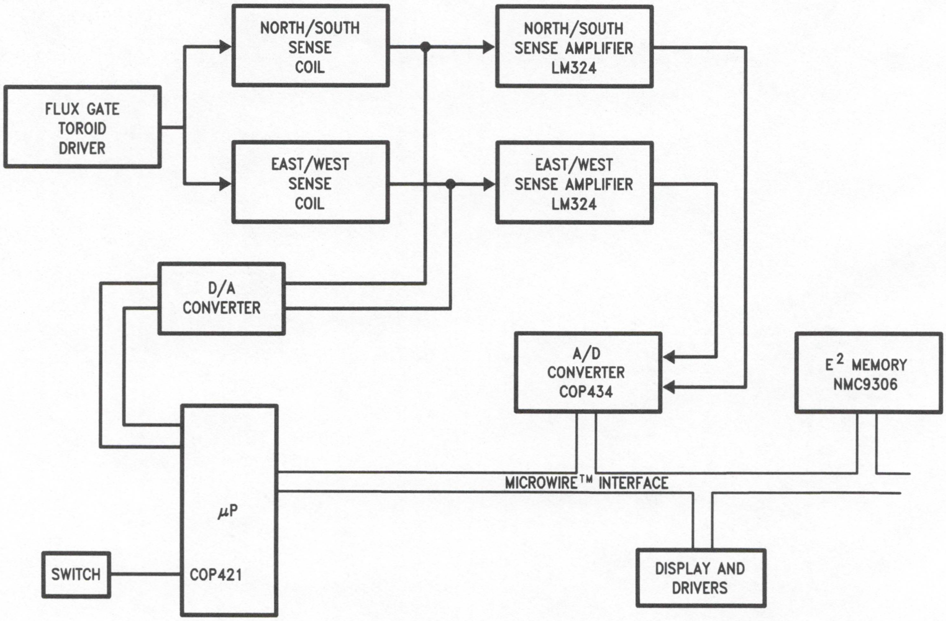
When a compass is first installed in a vehicle, or when new equipment, such as car speakers, are added to a vehicle with a compass, the compass must be compensated for stray magnetic fields. With a magnetic compass, it must be pointed towards magnetic north and then adjusted. This procedure is repeated at all four main points of the compass until the compass is calibrated. This procedure is lengthy and also requires another calibrated compass to point the vehicle in the correct direction.

The block diagram illustrates an electronic compass that, with the aide of an E^2 memory, makes adjusting a compass as easy as pushing a button, and also eliminates the need for another compass. In addition it gives you the ability to adjust for variation between magnetic and true north. This is a major advantage because it is something that even the most expensive magnetic compass cannot do.

The brain of the electronic compass is the COP421 microcontroller. There are two sense coils, one for north/south and one for east/west. The output of each of the sense amplifiers is an analog voltage which is fed into the A to D converter. These voltages are read by the COP421 over the microwire interface. From these voltages, the microcontroller determines the direction and displays the results once again over the microwire interface. To compensate the compass in a new environment the procedure is very simple. Start by pointing the car in any direction and push the switch. The CPU at this time will measure the voltage at the sense amplifiers and store this information in the E^2 memory over the microwire interface. Now the vehicle is turned 180°, and the button is pushed again. The same procedure will be followed internally. The compensation procedures are now complete. During operation the CPU will compensate for stray fields by adding an analog voltage back into the sense amplifiers. This value is stored in E^2 memory and not lost when the power is turned off, but is readjustable if its environment is modified.

Compass variation is the difference between true and magnetic north. This variation differs all over the world and is something that must be taken into consideration when navigating by compass. With the E^2 memory device, a variance can be programmed in for any given location. In California this is approximately 17°, in Michigan approximately 1°. Once again, this cannot be accomplished by a magnetic compass, and would have been impossible to accomplish without an E^2 memory device.

Electronic Compass Block Diagram



TL/D/8613–1

Automatic Low Cost Thermostat

National Semiconductor
Application Brief 22
Kent Brooten

Ths application brief describes the use of the NMC9346 (64 x 16) serial EEPROM. With the advent of the inexpensive COPS™ family from National Semiconductor, heretofore "expensive" applications can now be realized inexpensively. Such an application is a low cost thermostat. Typical features of such a device are:

1) Ability to interface to local and remote temperature sensors,
2) Ability to hold changeable settings,
3) Digital display of present temperature,
4) Inexpensive in high volume.

CIRCUIT DESCRIPTION

The basis of the thermostat is the COP410 microcontroller. This, with the addition of 2 ADC0854 A/D converters, an NMC9346 EEPROM and some logic for LED display, comprise an extremely versatile, yet low cost, system. The ADC0854 allows 4 channels of temperature sensors, 1 local and 3 remote. Temperature sensors used are LM34 (for readings in °F) or LM35 (for readings in °C).

While there are several possible choices for A/D converters that are MICROWIRE™ compatible, the ADC0854 was chosen because of its "settability". By presetting the "cold" temperature (i.e., when the cooling unit should come on—say 80°F) all the microcomputer has to do is to multiplex the inputs and read the data in line. Similarly, the "hot" A/D can be preset to the temperature where the furnace should come on (e.g., 60°F) and scanned in a like manner. Since the microcomputer is also keeping time of day, selecting an A/D with more "smarts" (as in the ADC0854) the software can be kept manageable and an external real time clock chip is not needed.

The EEPROM (NMC9346) holds the presettable temperature ranges (high and low settings) by day of the week. Since data is in EEPROM rather than in mask ROM, it can be changed.

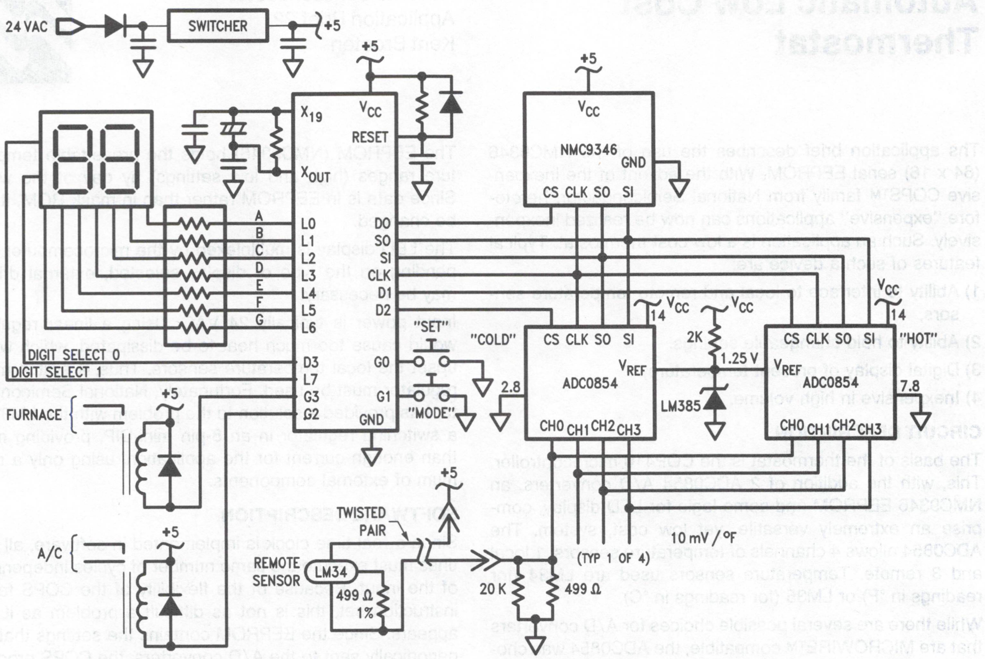
The LED display is multiplexed by the microcomputer. Depending on the type of display selected, external drivers may be necessary.

Input power is typically 24 VAC. Using a linear regulator would cause too much heat to be dissipated, which would upset the local temperature sensors. Thus, a switch mode regulator must be used. Fortunately, National Semiconductor has provided a solution to the problem with the LM3578, a switching regulator in an 8-pin mini-DIP, providing more than enough current for the application, using only a minimum of external components.

SOFTWARE DESCRIPTION

Since a real time clock is implemented in software, all routines must execute the same number of cycles independent of the input. Because of the flexibility of the COPS family instruction set, this is not as difficult a problem as it first appears. Since the EEPROM contains the settings that are periodically sent to the A/D converters, the COPS program merely fetches data from one source and dumps it to another while monitoring the output. Even the SET and MODE keys can be acted upon in a predictable manner IF the software designer carefully plans the program flow BEFORE writing code.

Note: Also see App Brief 15.


24 VAC
SWITCHER
+5
+5
X19
VCC
RESET
XOUT
+5
VCC
NMC9346
GND
CS CLK SO SI
A
B
C
D
E
F
G
L0
L1
L2
L3
L4
L5
L6
D0
SO
SI
CLK
D1
D2
"SET"
"COLD"
DIGIT SELECT 0
DIGIT SELECT 1
D3
L7
G3
G2
G0
G1
"MODE"
GND
2.8
14
VCC
VCC
14
VCC
CS CLK SO SI
2K
1.25 V
VREF
ADC0854
LM385
CH0 CH1 CH2 CH3
CS CLK SO SI
"HOT"
VREF
ADC0854
7.8
CH0 CH1 CH2 CH3
FURNACE
+5
A/C
+5
+5
TWISTED PAIR
REMOTE SENSOR
LM34
499 Ω 1%
10 mV / °F
(TYP 1 OF 4)
20 K
499 Ω

TL/D/8647–1

FIGURE 1

Designing with the NMC9306/COP494 a Versatile Simple to Use E^2 PROM

National Semiconductor
Application Note 338
Masood Alavi

This application note outlines various methods of interfacing an NMC9306/COP494 with the COPS™ family of microcontrollers and other microprocessors. *Figures 1–6* show pin connections involved in such interfaces. *Figure 7* shows how parallel data can be converted into a serial format to be inputted to the NMC9306; as well as how serial data outputted from an NMC9306 can be converted to a parallel-format.

The second part of the application note summarizes the key points covering the critical electrical specifications to be kept in mind when using the NMC9306/COP494.

The third part of the application note shows a list of various applications that can use a NMC9306/COP494.

GENERIC CONSIDERATIONS

A typical application should meet the following generic criteria:

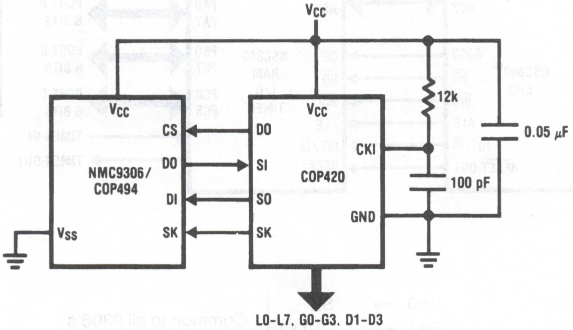
1. Allow for no more than 10,000 E/W cycles for optimum and reliable performance.
2. Allow for any number of read cycles.
3. Allow for an erase or write cycle that operates in the 10–30 ms range, and not in the tens or hundreds of ns range as used in writing RAMs. (Read vs write speeds are distinctly different by orders of magnitude in E^{2}PROM, not so in RAMs.)
4. No battery back-up required for data-retention, which is fully non-volatile for at least 10 years at room-ambient.

SYSTEM CONSIDERATIONS

When the control processor is turned on and off, power supply transitions between ground and operating voltage may cause undesired pulses to occur on data, address and control lines. By using WEEN and WEDS instructions in conjunction with a LO-HI transition on CS, accidental erasing or writing into the memory is prevented.

The duty cycle in conjunction with the maximum frequency translates into having a minimum Hi-time on the SK clock. If the minimum SK clock high time is greater than 1 µs, the duty cycle is not a critical factor as long as the frequency does not exceed the 250 kHz max. On the low side no limit exists on the minimum frequency. This makes it superior to the COP499 CMOS-RAM. The rise and fall times on the SK clock can also be slow enough not to require termination up to reasonable cable-lengths.

Since the device operates off of a simple 5V supply, the signal levels on the inputs are non-critical and may be operated anywhere within the specified input range.



TL/D/5286–1

FIGURE 1. NMC9306/COP494 — COP420 Interface

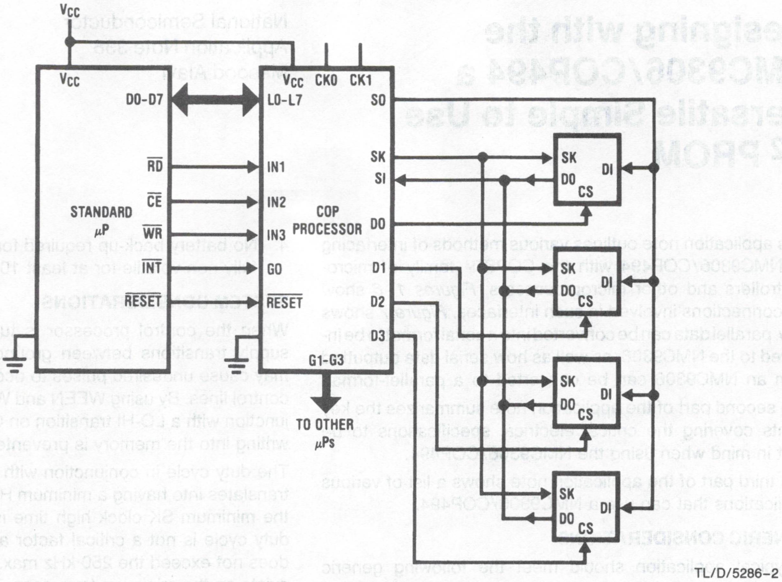
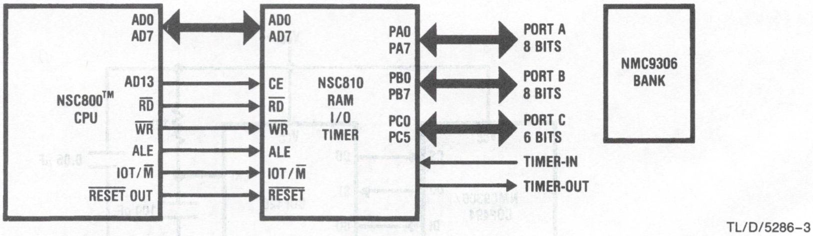

V_{CC}
VCC
VCC
D0–D7
RD
CE
WR
INT
RESET
STANDARD µP
VCC
CK0
CK1
L0–L7
IN1
IN2
IN3
GO
RESET
COP PROCESSOR
SO
SK
SI
DO
D1
D2
D3
G1–G3
TO OTHER µPs
SK
DO
CS
DI
TL/D/5286–2

FIGURE 2. NMC9306—Standard µP Interface Via COP Processor

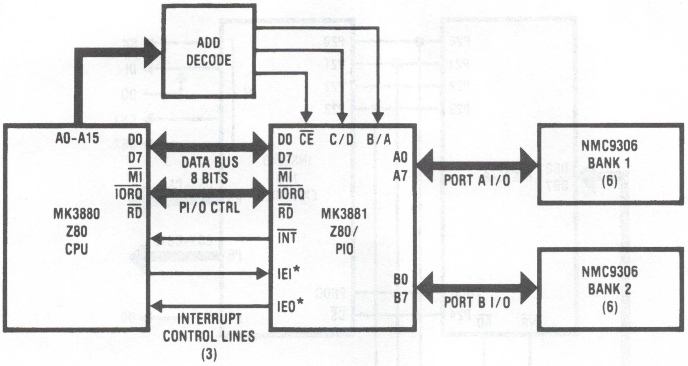

AD0
AD7
AD13
RD
WR
ALE
IOT/M
RESET OUT
NSC800™ CPU
AD0
AD7
CE
RD
WR
ALE
IOT/M
RESET
NSC810 RAM I/O TIMER
PA0
PA7
PB0
PB7
PC0
PC5
PORT A 8 BITS
PORT B 8 BITS
PORT C 6 BITS
TIMER-IN
TIMER-OUT
NMC9306 BANK
TL/D/5286–3

PA0 → SK
PA1 → DI/DO
Common to all 9306's
PA2–7 → 6CS for 6– 9306's

*** SK is generated on port pins by bit-set and bit-clear operations in software. A symmetrical duty cycle is not critical.**

*** CS is set in software. To generate 10–30 ms write/erase the timer/counter is used. During write/erase. SK may be turned off.**

FIGURE 3. NSC800™ to NMC9306 Interface (also Valid for 8085/8085A and 8156)


ADD
DECODE
A0-A15
D0
D7
$\overline{MI}$
$\overline{IORQ}$
$\overline{RD}$
MK3880
Z80
CPU
DATA BUS
8 BITS
PI/O CTRL
INTERRUPT
CONTROL LINES
(3)
D0
$\overline{CE}$
C/D
B/A
D7
$\overline{MI}$
$\overline{IORQ}$
$\overline{RD}$
$\overline{INT}$
IEI*
IEO*
MK3881
Z80/
PIO
A0
A7
B0
B7
PORT A I/O
PORT B I/O
NMC9306
BANK 1
(6)
NMC9306
BANK 2
(6)

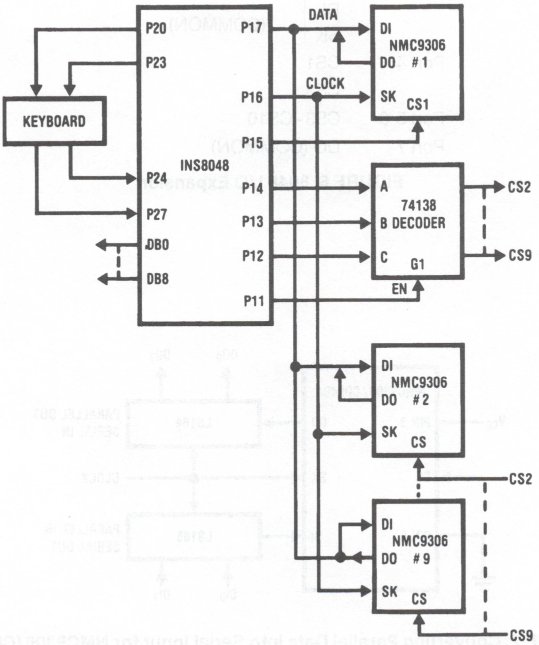
TL/D/5286-4

Z80-P10	9306	
A0	SK	Common to all 9306's (Bank 1)
A1	DI/DO	
A2-A7	CS1-CS6	

*** Only used if priority interrupt daisy chain is desired**

*** Identical connection for Port B**

FIGURE 4. Z80 — NMC9306 Interface Using Z80-PIO Chip

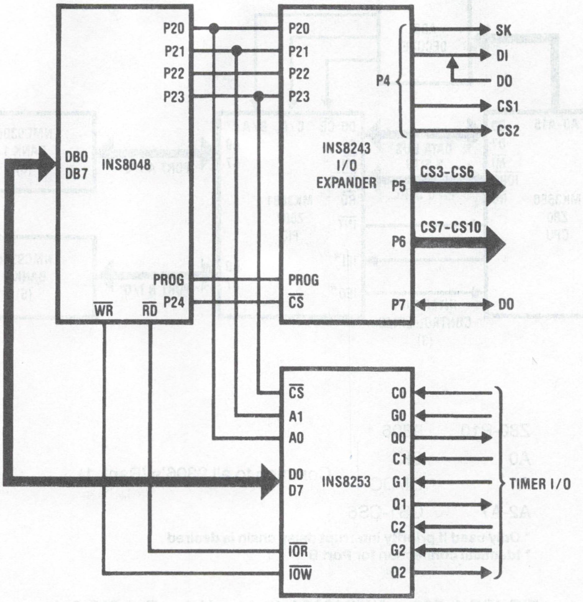

P20
P23
KEYBOARD
P24
P27
DB0
DB8
INS8048
P17
P16
P15
P14
P13
P12
P11
DATA
CLOCK
DI
NMC9306
DO #1
SK
CS1
A
74138
B DECODER
C
G1
EN
CS2
CS9
DI
NMC9306
DO #2
SK
CS
CS2
DI
NMC9306
DO #9
SK
CS
CS9

TL/D/5286-5

*** SK and DI are generated by software. It should be noted that at 2.72 μs/instruction. The minimum SK period achievable will be 10.88 μs or 92 kHz, well within the NMC9306 frequency range.**

*** DO may be brought out on a separate port pin if desired.**

FIGURE 5. 48 Series μP — NMC9306 Interface

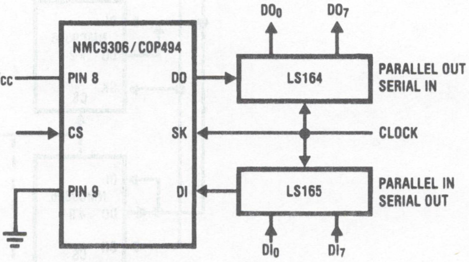

P20
P21
P22
P23
DB0
DB7
INS8048
PROG
P24
WR
RD
P20
P21
P22
P23
P4
INS8243
I/O
EXPANDER
P5
P6
PROG
CS
P7
SK
DI
DO
CS1
CS2
CS3-CS6
CS7-CS10
DO
CS
A1
A0
D0
D7
INS8253
IOR
IOW
C0
G0
Q0
C1
G1
Q1
C2
G2
Q2
TIMER I/O

TL/D/5286-6

Expander outputs

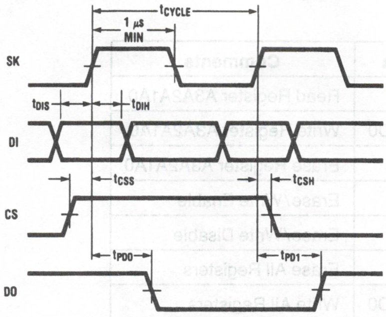
Port 4	DI SK	(COMMON)
	CS1	
	CS2	
Port 5-6	CS3-CS10	
Port 7	DO (COMMON)	

FIGURE 6. 8048 I/O Expansion


NMC9306/COP494
V_{CC}
PIN 8
DO
CS
SK
PIN 9
DI
DO_0
DO_7
LS164
PARALLEL OUT
SERIAL IN
CLOCK
LS165
PARALLEL IN
SERIAL OUT
DI_0
DI_7

TL/D/5286-7

FIGURE 7. Converting Parallel Data into Serial Input for NMC9306/COP494



	Min	Max
t_{CYCLE}	0	250 kHz
t_{DIS}	400	ns
t_{D1H}	400	ns
t_{CSS}	200	ns
t_{CSH}	0	ns
t_{PD0}		2 µs
t_{PD1}		2 µs

TL/D/5286–8

FIGURE 8. NMC9306/COP494 Timing

THE NMC9306/COP494

Extremely simple to interface with any µP or hardware logic. The device has six pins for the following functions:

Pin 1	CS*	HI enabled
Pin 2	SK	Serial Clock input
Pin 3	DI	For instruction or data input
Pin 4	DO**	For data read, TRI-STATE® otherwise
Pin 5	GND	
Pin 8	V_{CC}	For 5V power
Pins 6–7	No Connect	No termination required

*Following an E/W instruction feed, CS is also toggled low for 10 ms (typical) for an E/W operation. This internally turns the VPP generator on (HI-LO on CS) and off (LO-HI on CS).

**DI and DO can be on a common line since DO is TRI-STATED when unselected DO is only on in the read mode.

USING THE NMC9306/COP494

The following points are worth noting:

1. SK clock frequency should be in the 0–250 kHz range. With most µPs this is easily achieved when implemented in software by bit-set and bit-clear instructions, which take 4 instructions to execute a clock or a frequency in the 100 kHz range for standard µP speeds. Symmetrical duty cycle is irrelevant if SK HI time is ≥ 2 µs.
2. CS low period following an E/W instruction must not exceed the 30 ms max. It should best be set at typical or minimum spec of 10 ms. This is easily done by timer or a software connect. The reason is that it minimizes the 'on time' for the high V_{PP} internal voltage, and so maximizes endurance. SK-clock during this period may be turned off if desired.
3. All E/W instructions must be preceded by EWEN and should be followed by an EWDS. This is to secure the stored data and avoid inadvertent erase or write.
4. A continuously 'on' SK clock does not hurt the stored data. Proper sequencing of instructions and data on DI is essential to proper operation.
5. Stored data is fully non-volatile for a minimum of ten years independent of V_{CC}, which may be on or off. Read cycles have no adverse effects on data retention.
6. Up to 10,000 E/W cycles/register are possible. Under typical conditions, this number may actually approach 1 million. For applications requiring a large number of cycles, redundant use of internal registers beyond 10,000 cycles is recommended.
7. Data shows a fairly constant E/W Programming behavior over temperature. In this sense E²PROMs supersede EPROMs which are restricted to room temperature programming.
8. As shown in the timing diagrams, the start bit on DI must be set by a ZERO - ONE transition following a CS enable (ZERO - ONE), when executing any instruction. ONE CS enable transition can only execute ONE instruction.
9. In the read mode, following an instruction and data train, the DI can be a don't care, while the data is being outputted i.e., for next 17 bits or clocks. The same is true for other instructions after the instruction and data has been fed in.
10. The data-out train starts with a dummy bit 0 and is terminated by chip deselect. Any extra SK cycle after 16 bits is not essential. If CS is held on after all 16 of the data bits have been outputted, the DO will output the state of DI till another CS LO-HI transition starts a new instruction cycle.
11. When a common line is used for DI and DO, a probable overlap occurs between the last bit on DI and start bit on DO.
12. After a read cycle, the CS must be brought low for 1 SK clock cycle before another instruction cycle can start.

All commands, data in, and data out are shifted in/out on rising edge of SK clock.

Write/erase is then done by pulsing CS low for 10 ms.

All instructions are initiated by a LO-HI transition on CS followed by a LO-HI transition on DI.

READ — After read command is shifted in DI becomes don't care and data can be read out on data out, starting with dummy bit zero.

WRITE — Write command shifted in followed by data in (16 bits) then CS pulsed low for 10 ms minimum.

INSTRUCTION SET

Instruction	SB	Opcode	Address	Data	Comments
READ	01	10xx	A3A2A1A0		Read Register A3A2A1A0
WRITE	01	01xx	A3A2A1A0	D15–D0	Write Register A3A2A1A0
ERASE	01	11xx	A3A2A1A0		Erase Register A3A2A1A0
EWEN	01	0011	XXXX		Erase/Write Enable
EWDS	01	0000	XXXX		Erase/Write Disable
ERAL	01	0010	XXXX		Erase All Registers
WRAL	01	0001	XXXX	D15–D0	Write All Registers

NMC9306 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

The following is a list of various systems that could use a NMC9306/COP494

A. Airline terminal
Alarm system
Analog switch network
Auto calibration system
Automobile odometer
Auto engine control
Avionics fire control
B. Bathroom scale
Blood analyzer
Bus interface
C. Cable T.V. tuner
CAD graphics
Calibration device
Calculator—user programmable
Camera system
Code identifier
Communications controller
Computer terminal
Control panel
Crystal oscillator
D. Data acquisition system
Data terminal
E. Electronic circuit breaker
Electronic DIP switch
Electronic potentiometer
Emissions analyzer
Encryption system
Energy management system
F. Flow computer
Frequency synthesizer
Fuel computer
G. Gas analyzer
Gasoline pump
H. Home energy management
Hotel lock
I. Industrial control
Instrumentation
J. Joulemeter
K. Keyboard -softkey
L. Laser machine tool
M. Machine control
Machine process control
Medical imaging
Memory bank selection
Message center control
Mobile telephone
Modem
Motion picture projector
N. Navigation receiver
Network system
Number comparison
O. Oilfield equipment
P. PABX
Patient monitoring
Plasma display driver
Postal scale
Process control
Programmable communications
Protocol converter
Q. Quiescent current meter
R. Radio tuner
Radar dectector
Refinery controller
Repeater
Repertory dialer
S. Secure communications system
Self diagnostic test equipment
Sona-Bouy
Spectral scanner
Spectrum analyzer
T. Telecommunications switching system
Teleconferencing system
Telephone dialing system
T.V. tuner
Terminal
Test equipment
Test system
TouchTone dialers
Traffic signal controller
U. Ultrasound diagnostics
Utility telemetering
V. Video games
Video tape system
Voice/data phone switch
W. Winchester disk controller
X. X-ray machine
Xenon lamp system
Y. YAG—laser controller
Z. Zone/perimeter alarm system

The NMC9346—An Amazing Device

National Semiconductor
Application Note 423
Stacy Deming

Question: What has 8 pins, runs on 5V and can store any one of more than 10^{300} unique bit patterns?

Answer: The NMC9346—a 1024-bit serial EEPROM.

Surprised? It is easy to check:

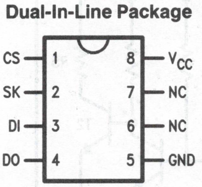
2^{1024} = number of possible combinations

$2^{10} = 10^3$

$2^{1024} \cong (2^{10})^{102} = (10^3)^{102} = 10^{306}$

10^{306} combinations are more than enough for any conceivable security application, serial number, or station I.D. many times over. Although the NMC9346 is a small part both physically and in memory size, its capacity to store unique codes is boundless.

Figure 1 shows the pin assignments and pin names for the NMC9346. Pins 6 and 7 are not connected, leaving only 6 active pins on the device. The DO pin is not active while data is being loaded through the DI pin. DI and DO can be tied together, creating a device that requires a 5-wire interface. This interface may be useful in security applications. The EEPROM could be built into a module that could be used as a "smart key" in electronic security systems. The key would be read whenever it was inserted into a 5-contact keyhole and access would be granted or denied as determined by the stored code. If only 256 bits of the EEPROM were to be used to store the code, this would still provide 10^{77} possible combinations. The remainder of the memory in the key could be used for data collection or to keep a record of where the key had been. It should be noted that ability to write data into the key allows the key to be immediately erased if it is misused.



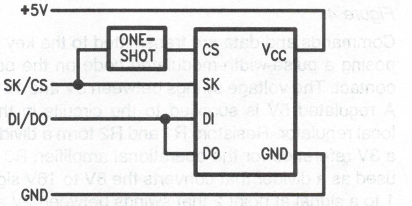
TL/D/8611-1

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Data Input
DO	Data Output
V_{CC}	+5V
GND	Ground
NC	No Connection

FIGURE 1

The 5-contact key is nice, but a 4-contact key is at least 20% better. *Figure 2* shows how the addition of a retriggerable one-shot can achieve this reduction. This circuit puts some timing constraints on the serial clock signal, but these are easily met. The output pulse of the one-shot should remain high for a period that is slightly longer than one serial clock cycle to prevent the NMC9346 from being reset. (The falling edge of CS must occur before the rising edge of the serial clock after the last bit of a write command is transmitted.)

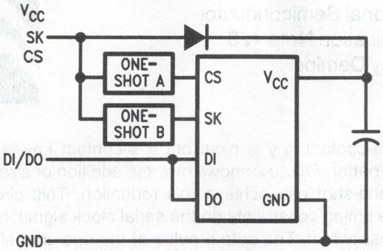


TL/D/8611-2

One-shot is retriggerable MM74HC123

FIGURE 2

A circuit for a 3-contact key is shown in *Figure 3*. A filter capacitor, diode and one-shot have been added. Both one-shots are triggered whenever a pulse to ground occurs on the power supply contact. The capacitor and diode provide power to the NMC9346 and the one-shots during this brief power interruption. An operational amplifier can be used as the power source and can easily generate the required waveform. Both the serial clock and chip select signals are recovered from this waveform.



TL/D/8611-3

One-Shot A—½ MM74HC123

One-Shot B—½ MM74HC123

FIGURE 3

By adding more circuitry to the key, it is possible to achieve a 2-contact interface. A circuit for this interface is shown in *Figure 4*.

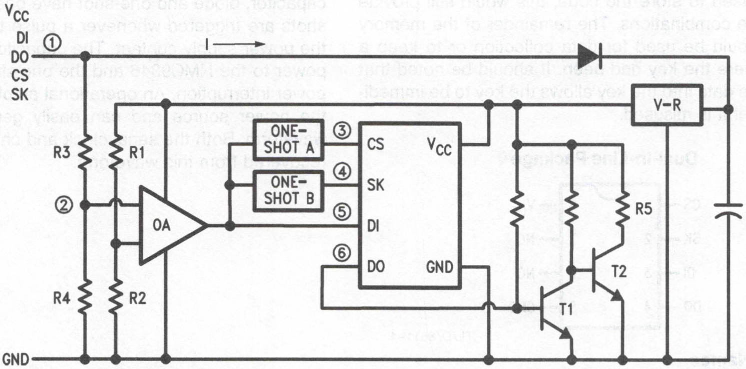
Commands and data are transmitted to the key by superimposing a pulse-width-modulated code on the power supply contact. The voltage swings between 8V and 16V at point 1. A regulated 5V is supplied to the circuits in the key by a local regulator. Resistors R1 and R2 form a divider to create a 3V reference for the operational amplifier. R3 and R4 are used as a divider that converts the 8V to 16V signal at point 1 to a signal at point 2 that swings between 2V and 4V. The output of the operational amplifier now follows the signal at point 1 but swings from 0V to 5V. This signal is used to trigger the one-shots as in the 3-contact circuit, and appears at the DI pin as a pulse-width-modulated signal. Command and data signals may now be entered. Data is read from the key by monitoring the power supply current. When the DO pin is in TRI-STATE® or outputs a one, transistor T2 is turned off. When DO outputs a zero, T2 is turned on and current flows through R5. The value of R5 may be chosen to create whatever current change is needed to detect the state of DO. The current should be tested when the voltage at point 1 is 16V. The resistor in this example will produce a 10 mA change.

Figure 5 shows a typical read sequence for the circuit shown in *Figure 4*.

Conclusion

This application note describes a number of circuits that are useful in security and data collection systems. These circuits should be considered only the beginning. It no longer makes sense to install DIP switches to select access codes in garage door openers, cordless and mobile phones, or any other microcontroller-based system. "Smart keys" can be used to gain access to databases and can be invalidated over normal communication lines if they are abused. It boggles the mind to consider what can be done with so many unique codes.

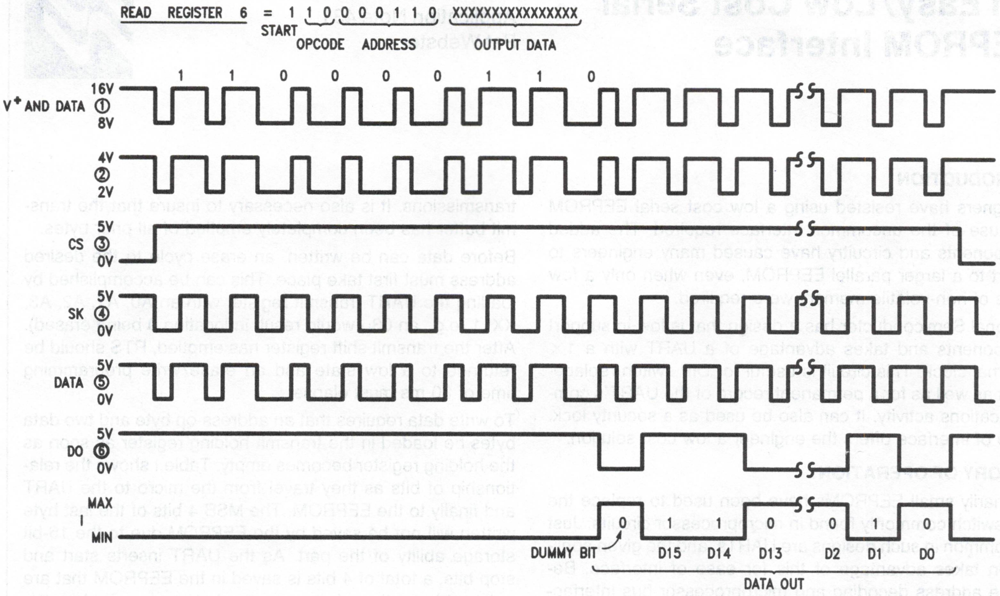
Note: The circuits in this application note feature the NMC9346. The NMC9306 is a pin-compatible part that stores 256 bits. The NMC9346 was used because it has a self-timing write cycle and the NMC9306 does not. Additional circuitry is not required to use the NMC9306, but an additional chip select signal must occur at the CS pin to terminate a write cycle.



TL/D/8611-4

R1 = 20K
R2 = 30K
R3 = 15K
R4 = 5K
One-Shot A = ½ MM74HC123
One-Shot B = ½ MM74HC123
V-R = LM2930Z-5.0
OA = LM358
R5 = 1600Ω

FIGURE 4


READ REGISTER 6 = 1 1 0 0 0 0 1 1 0 XXXXXXXXXXXXXXX
START
OPCODE
ADDRESS
OUTPUT DATA
1 1 0 0 0 0 1 1 0
16V
V+ AND DATA ①
8V
4V
②
2V
5V
CS ③
0V
5V
SK ④
0V
5V
DATA ⑤
0V
5V
DO ⑥
0V
MAX
1
MIN
DUMMY BIT
0
1
1
0
0
1
0
D15
D14
D13
D2
D1
D0
DATA OUT

TL/D/8611-5

FIGURE 5

An Easy/Low Cost Serial EEPROM Interface

National Semiconductor
Application Note 431
Pat Webster

INTRODUCTION

Designers have resisted using a low cost serial EEPROM because of the uncommon interface required. The added components and circuitry have caused many engineers to resort to a larger parallel EEPROM, even when only a few bytes of non-volatile memory were required.

National Semiconductor has a design that is low in support components and takes advantage of a UART with a 1× external clock. This circuit is useful for DIP switch replacement as well as for a permanent record of the UART's communications activity. It can also be used as a security lock. Ease of interface offers the engineer a low cost solution.

THEORY OF OPERATION

Ordinarily small EEPROMs have been used to replace the DIP switch commonly found in microprocessor circuits. Just as common in such designs are UARTs, and the given application takes advantage of this for ease of interface. Because address decoding and microprocessor bus interfacing have already been accomplished, the UART is an ideal support interface for a serial EEPROM. The only true requirements for a serial EEPROM are the serial data path, clock timing, and chip select signal. All of these signals are derived from a UART in this application.

The Data In for the EEPROM is the transmitted data of the UART. Data Out of the EEPROM is directed to the receive data line of the UART. The chip select required by the EEPROM is a modem control line whose level is used to select either the modem device or the EEPROM. Finally, the serial clock required by the EEPROM can be a 1× clock provided by the UART.

THE WRITE CYCLE

When a write cycle is desired, the UART must be set up for an external 1× clock, 8 data bits, 1 stop bit, no parity and RTS must be programmed for a high output prior to data transmissions. It is also necessary to insure that the transmit buffer has been completely emptied of all prior bytes.

Before data can be written, an erase cycle to the desired address must first take place. This can be accomplished by loading the UART transmit register with an A0, A1, A2, A3, XX11 (e.g., an 03_H would result in location 0 being erased). After the transmit shift register has emptied, RTS should be returned to a low state and an erase/write programming time of 30 ms must elapse.

To write data requires that an address-op byte and two data bytes be loaded in the transmit holding register as soon as the holding register becomes empty. Table I shows the relationship of bits as they travel from the micro to the UART and finally to the EEPROM. The MSB 4 bits of the last byte written will not be saved by the EEPROM due to the 16-bit storage ability of the part. As the UART inserts start and stop bits, a total of 4 bits is saved in the EEPROM that are not usable by the microprocessor but are required by the UART.

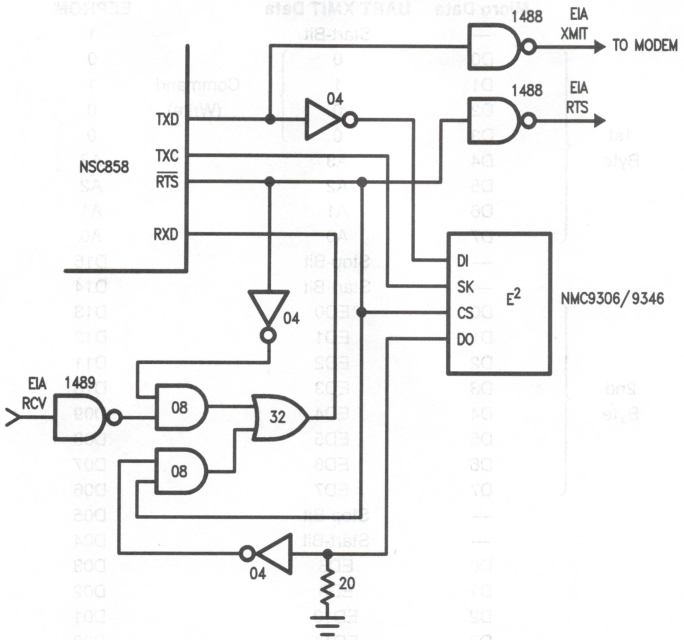
THE READ CYCLE

As was true for the write cycle, the UART must be set up for 8 data bits, 1 stop bit, and an external 1× clock. To start the read cycle, a byte with read op and address must be written to the UART. An example of read location 0 would be 01_H. After the transmit shift register has emptied, the receiver shift register will begin to accumulate the data that was written and two reads will be required before the operation can be considered complete.

CONCLUSION

For a further understanding of this interface, refer to the NMC9306/9346 and the NSC858 data sheets. Parity could be added for data integrity with further sacrifice of usable data bits in the EEPROM and the possibility of the second byte read being in parity error.

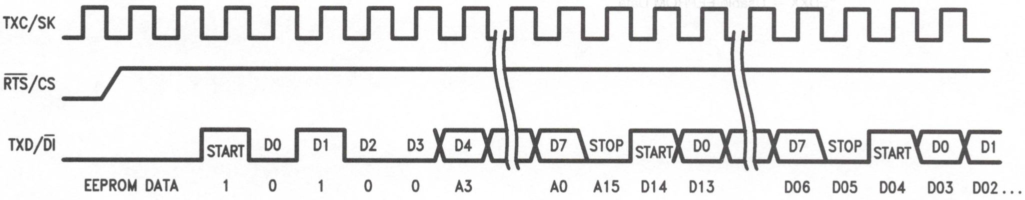
UART/EEPROM Interface


1488
EIA XMIT
TO MODEM
04
1488
EIA RTS
TXD
TXC
NSC858
RTS
RXD
DI
SK
E2
CS
NMC9306/9346
DO
04
EIA RCV
1489
08
32
08
04
20

TL/D/8642-1

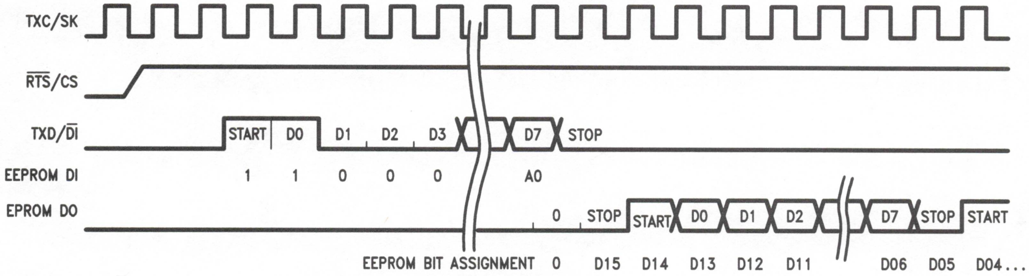
UART/EEPROM Timing

Write Cycle (9306)


TXC/SK
RTS/CS
TXD/DI
START
D0
D1
D2
D3
D4
D7
STOP
START
D0
D7
STOP
START
D0
D1
EEPROM DATA
1
0
1
0
0
A3
A0
A15
D14
D13
D06
D05
D04
D03
D02...

TL/D/8642-2

Read Cycle


TXC/SK
RTS/CS
TXD/DI
START
D0
D1
D2
D3
D7
STOP
EEPROM DI
1
1
0
0
0
A0
EPROM DO
0
STOP
START
D0
D1
D2
D7
STOP
START
EEPROM BIT ASSIGNMENT
0
D15
D14
D13
D12
D11
D06
D05
D04...

TL/D/8642-3

Table I

	Micro Data	UART XMIT Data		EEPROM
	—	Start-Bit		1
1st Byte	D0	0	Command (Write)	0
	D1	1		1
	D2	0		0
	D3	0		0
	D4	A3		A3
	D5	A2		A2
	D6	A1		A1
	D7	A0		A0
	—	Stop-Bit		D15
	—	Start-Bit		D14
2nd Byte	D0	*ED0		D13
	D1	ED1		D12
	D2	ED2		D11
	D3	ED3		D10
	D4	ED4		D09
	D5	ED5		D08
	D6	ED6		D07
	D7	ED7		D06
	—	Stop-Bit		D05
	—	Start-Bit		D04
	D0	ED8		D03
	D1	ED9		D02
	D2	ED10		D01
	D3	ED11		D00
	D4	N/A		N/A
	D5	N/A		N/A
	D6	N/A		N/A
	D7	N/A		N/A
	—	Stop-Bit		N/A

*EDXX = Usable EEPROM Data

Using the NMC9306 for Configuration and Production Information in a TMP Based Terminal System

National Semiconductor
Application Note 433
Richard Zarr

ABSTRACT

This application note gives a detailed description of the use of the NMC9306 E^{2}PROM in a TMP based environment. The function of the E^{2}PROM is to contain all the configuration data for the terminal (i.e., baud rate, auto dial numbers, function selects, etc.) and also production information (i.e., serial number, date of manufacture, etc.)

INTRODUCTION

In a computer terminal environment, there are many user selectable options that need to be strapped into the terminal before it can be used. Some terminals have modems built into them that can automatically dial numbers for you. Some terminals can even emulate several different industry standard terminals, all in one. This configuration information is usually programmed into the terminal by using DIP switches accessed through some access cover or by removing a certain panel. A major drawback to this type of configuring is that the terminal must be opened by the user if they are to change the strapping. Another disadvantage is the terminal usually cannot be changed dynamically. Enter NON-VOLATILE RAM or battery-backed-up RAM. This creates another problem in that the system cost is increased, reliability suffers, and board space may not be available. Enter NMC9306 serial E^{2}PROM in an 8-pin Mini-DIP. This device is not only non-volatile, but is small, inexpensive, and simple to use.

HARDWARE MAIN DESCRIPTION

Since the NS455 Terminal Management Processor (TMP) does not have a MICROWIRE™ interface, another method of interfacing must be devised. The TMP has provisions for an external output port attached to the ROM bus which can be used to simulate the MICROWIRE interface. This is done by using three free data bits of a 74LS273 as shown in *Figure 1.* These three bits will be the CHIP SELECT, CLOCK, and the DATA IN inputs to the NMC9306. The TMP also has an input port enable pin that can be used to read a set of buffers such as a 74LS244. A single pin can be used for the DATA OUT signal from the NMC9306 as shown in *Figure 2.* If no input port is required, the DATA OUT signal can be driven directly onto the ROM expansion bus through a 4.7k resistor as shown in *Figure 1.* This is all the hardware that is required to interface the part.

SOFTWARE MAIN DESCRIPTION

This is where things get a bit tricky. Routines must be written to communicate with the NMC9306. These routines must read, write, erase, and enable erase/write in the NMC9306 by simulating the MICROWIRE interface. This is done by turning the output ports pins on and off with the correct timing to simulate the interface without interfering with the other pins. Also, the input data must be converted to usable form as well as converting the outgoing data to serial form. Simple.

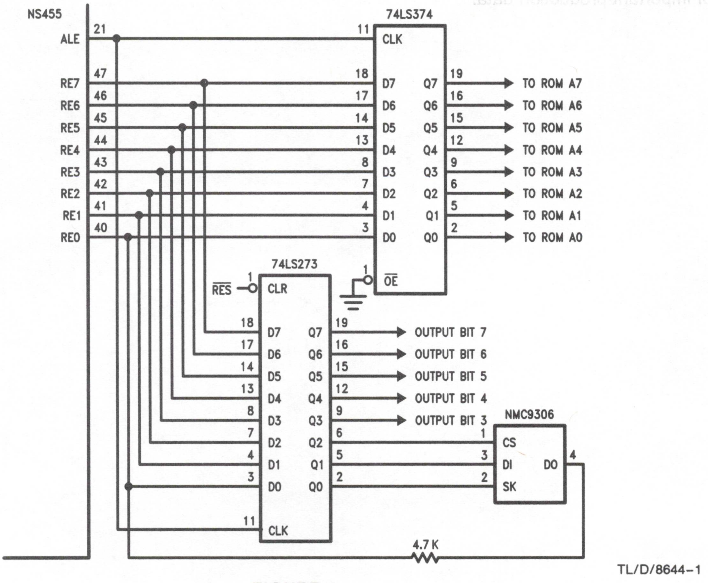


FIGURE 1

To start, there are a few things to be mentioned. The TMP has a modified 8048 processor for its controller. This controller has a 16-bit accumulator, addressed as two 8-bit registers, which are ACC and HACC. The high accumulator (HACC) is accessed through the low accumulator (ACC). This is important since the NMC9306 is arranged in 16 words of 16 bits each. Also, to allow the port to be modified without changing any unwanted bits, a PORT MASK must be defined in the memory of the TMP. Any change to the port should be done by updating the mask, and then sending the mask data to the port. This will also make testing the data on the port possible. The codes for communicating with the NMC9306 can be obtained from the *National Semiconductor 1984 MOS Memory Databook* in Section 7. Also, all critical timing parameters are described therein.

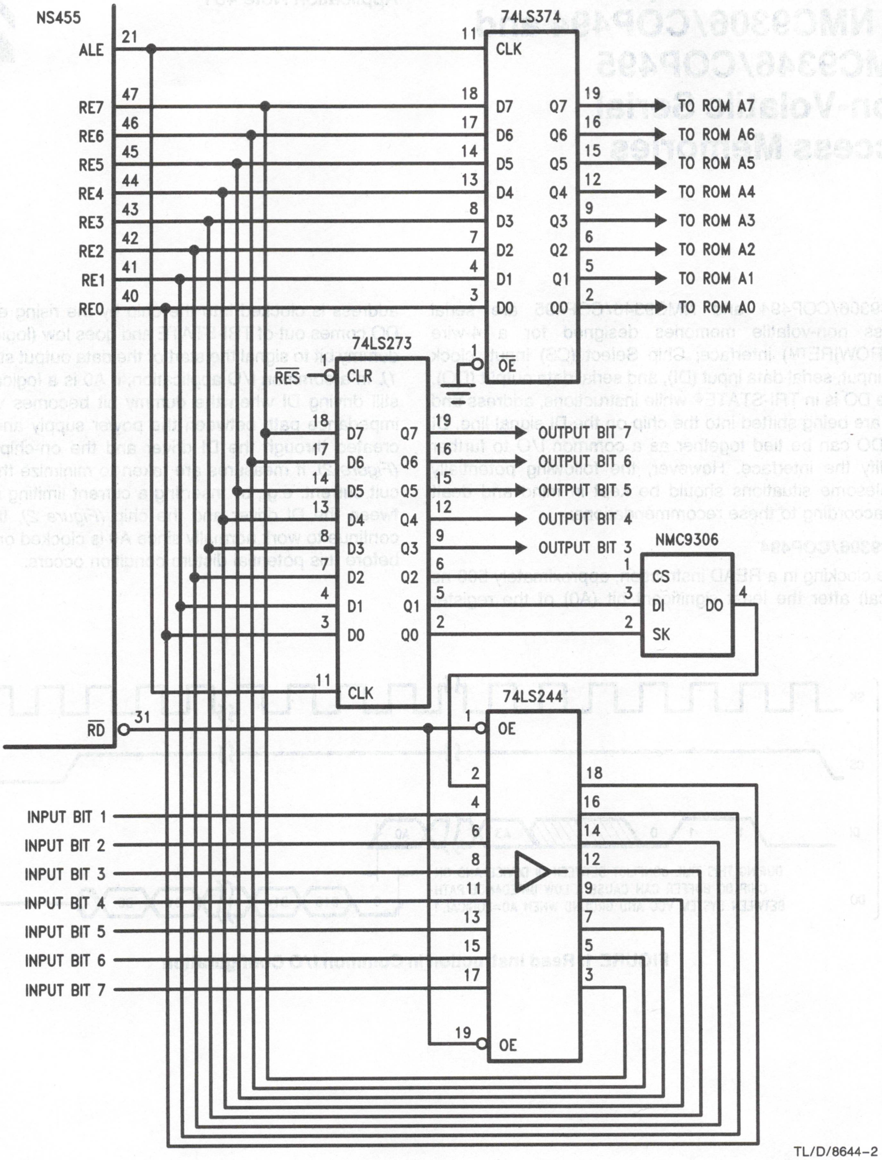
In a typical TMP system, there are large amounts of configuration data that must be set up before the terminal can communicate properly. If the system is really complex, it may need more yet. A typical configuration map is shown below. Along with the configuration data, production information should be included. This may be entered by some code at power-up that is not documented in the end user guide. This set-up screen may ask for the date of assembly, the assembly location code, the serial number, the customer code, the options enabled (tricky sales pitch— "for only $50 more . . . ."), the number of times the unit was returned to the factory for service, and any other data that must be tracked for production. If the NMC9306 does not have enough room, the NMC9346 is 4 times larger, and has the same hardware requirements. Only slight software changes are required.

CONCLUSION

It can be seen that the NMC9306 is simple, yet functional in replacing strapping switches and enhancing the product. The NMC9306/NMC9346 components in this application, replace more costly and larger parts, and are easily integrated into a TMP or other terminal design. The end product will be more versatile through enhanced user interface and tracking of important production data.

Typical Configuration Map

Location (Hex)		Description
0	Bit 0	Cursor Blink Enable
	Bit 1	Cursor Underline/Block
	Bit 2	Cursor Inverts Video On
	Bit 3	Screen Norm/Inverse Vid
	Bit 4	Local Mode On/Off
	Bit 5	Status Line Enable
	Bits 6–F	(Spare)
1	Bits 0–3	Baud Rate
	Bit 4	1 or 2 Stop Bits
	Bit 5	7 or 8 Data Bits
	Bit 6	Parity On/Off
	Bit 7	Odd or Even Parity
	Bits 8–F	(Spare)
2	Bits 0–F	(Spare)
3	Bits 0–F	Month and Year of Assem.
4	Bits 0–7	Day of Assembly
	Bits 8–F	Assembly Location
5	Bits 0–7	Inspector Code
	Bits 8–F	No. of Returns
6	Bits 0–F	Serial Number (MSW)
7	Bits 0–F	Serial Number
8	Bits 0–F	Serial Number (LSW)
9	Bits 0–7	Failure Code 1
	Bits 8–F	Failure Code 2
A	Bits 0–F	Check Sum
B–F		(Spare)


NS455
ALE 21
RE7 47
RE6 46
RE5 45
RE4 44
RE3 43
RE2 42
RE1 41
RE0 40
RD 31
74LS374
11 CLK
18 D7 Q7 19
17 D6 Q6 16
14 D5 Q5 15
13 D4 Q4 12
8 D3 Q3 9
7 D2 Q2 6
4 D1 Q1 5
3 D0 Q0 2
1 OE
TO ROM A7
TO ROM A6
TO ROM A5
TO ROM A4
TO ROM A3
TO ROM A2
TO ROM A1
TO ROM A0
74LS273
RES 1 CLR
18 D7 Q7 19
17 D6 Q6 16
14 D5 Q5 15
13 D4 Q4 12
8 D3 Q3 9
7 D2 Q2 6
4 D1 Q1 5
3 D0 Q0 2
11 CLK
OUTPUT BIT 7
OUTPUT BIT 6
OUTPUT BIT 5
OUTPUT BIT 4
OUTPUT BIT 3
NMC9306
1 CS
3 DI
DO 4
2 SK
74LS244
1 OE
2 18
4 16
6 14
8 12
11 9
13 7
15 5
17 3
19 OE
INPUT BIT 1
INPUT BIT 2
INPUT BIT 3
INPUT BIT 4
INPUT BIT 5
INPUT BIT 6
INPUT BIT 7

TL/D/8644-2

FIGURE 2

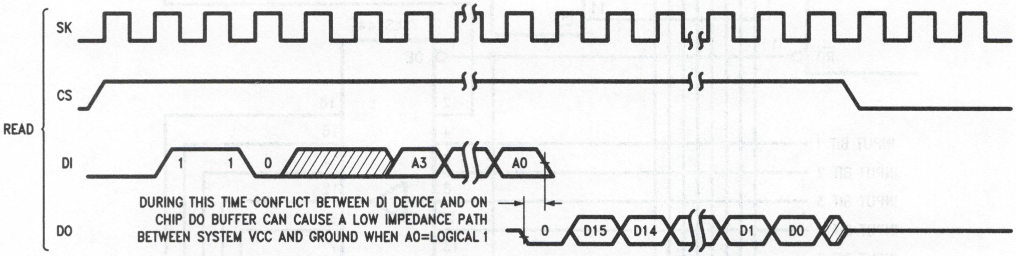
Common I/O Applications of NMC9306/COP494 and NMC9346/COP495 Non-Volatile Serial Access Memories

National Semiconductor
Application Note 481

NMC9306/COP494 and NMC9346/COP495 are serial access non-volatile memories designed for a 4-wire (MICROWIRE™) interface; Chip Select (CS) input, clock (SK) input, serial data input (DI), and serial data output (DO). Since DO is in TRI-STATE® while instructions, address and data are being shifted into the chip on the DI signal line, DI and DO can be tied together as a common I/O to further simplify the interface. However, the following potentially troublesome situations should be kept in mind and dealt with according to these recommendations:

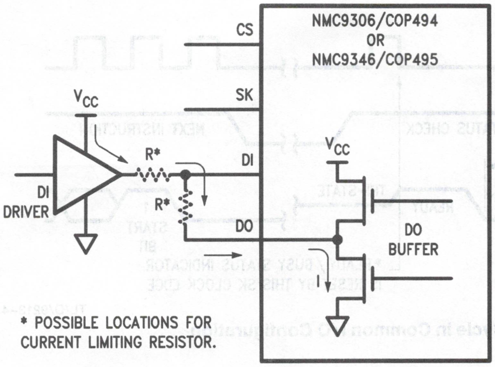
NMC9306/COP494

While clocking in a READ instruction, approximately 500 ns (typical) after the least significant bit (A0) of the register address is clocked into the chip by the rising edge of SK, DO comes out of TRI-STATE and goes low (logical '0') as a dummy bit to signal the start of the data output string *(Figure 1).* In a common I/O application, if A0 is a logical '1' and is still driving DI when the dummy bit becomes valid, a low impedance path between the power supply and ground is created through the DI driver and the on-chip DO buffer *(Figure 2).* If measures are taken to minimize the short circuit current, e.g., by inserting a current limiting resistor between the DI driver and the chip *(Figure 2),* the part will continue to work normally since A0 is clocked onto the chip before this potential disturb condition occurs.


SK
CS
READ
DI
1
1
0
A3
A0
DURING THIS TIME CONFLICT BETWEEN DI DEVICE AND ON CHIP DO BUFFER CAN CAUSE A LOW IMPEDANCE PATH BETWEEN SYSTEM VCC AND GROUND WHEN A0=LOGICAL 1
DO
0
D15
D14
D1
D0

TL/D/9213–1

FIGURE 1. Read Instruction in Common I/O Configuration



TL/D/9213–2

FIGURE 2. Current Path during DI Driver and DO Buffer Conflict during Read Instruction

NMC9346/COP495

The NMC9346/COP495 has a self-timed programming cycle which uses DO to indicate the ready/busy status of the chip. Therefore, in addition to the potential problem in the READ mode similar to NMC9306/COP494 described above, another pitfall may be encountered at the end of a programming cycle in common I/O applications.

The self-timed programming cycle is initiated by the falling edge of CS after a programming instruction (ERASE, WRITE, ERAL, WRAL) is shifted in. If CS is brought high subsequently, after a minimum of 1 µs (tcs), DO indicates the ready/busy status of the chip. DO = logical '0' indicates that programming is still in progress. DO = logical '1' signals the end of the programming cycle. This 'status check' function of DO is cancelled (i.e., DO returns to TRI-STATE) when a logical '1' on DI is clocked into the chip by SK with CS high. With separate input and output this is automatically accomplished by the start bit of the next instruction *(Figure 3)*.

In a common I/O application, the following clocking sequence is recommended to avoid premature cancellation of the 'ready' status and/or interference of the 'ready' status with the serial input sequence for the next instruction *(Figure 4)*:

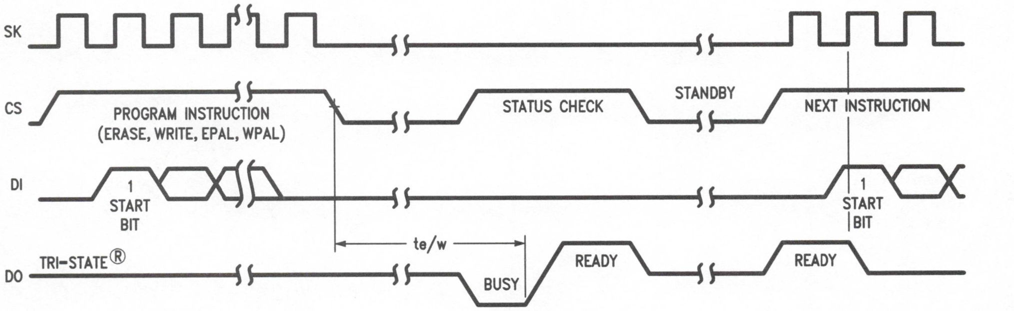
1) Inhibit the SK clock after clocking in the programming instruction.
2) After acknowledging the 'ready' status, clock SK once while the common I/O is still high to cancel the ready/busy status function of DO.
3) Bring CS low for a minimum of 1 µs (tcs) to clear the instruction register before initiating the next instruction.

DO is now reset back to TRI-STATE, and the chip is ready to accept the next instruction.

The chip may enter the 'ready' status mode under certain conditions of V_{CC} power-up. This occurs due to the V_{CC} power-up conditions setting the status mode logic on the chip, and is not an indication of a spurious programming cycle on V_{CC} power-up. The following clocking sequence is recommended to ensure cancellation of this status signal after V_{CC} power-up *(Figure 5)*:

1) Bring CS high.
2) Clock SK once to ensure cancellation of the 'ready' status.
3) Bring CS low for a minimum of 1 µs (tcs) to clear the instruction register before initiating the first instruction.

NMC9346 Timing Diagrams

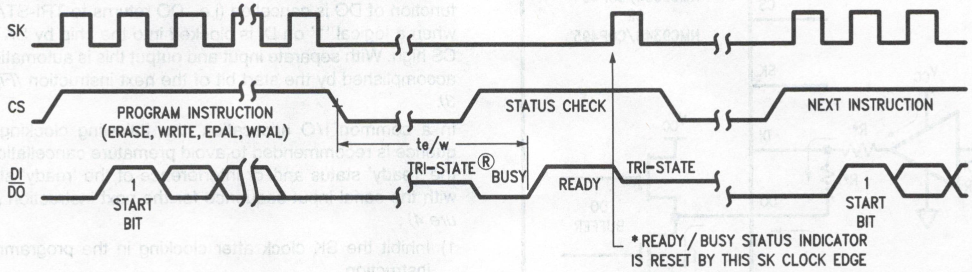


TL/D/9213–3

*The Ready/Busy Status Indicator for a program Instruction (ERASE, WRITE, ERAL, WRAL) is reset when the Start bit for the following Instruction is clocked in.

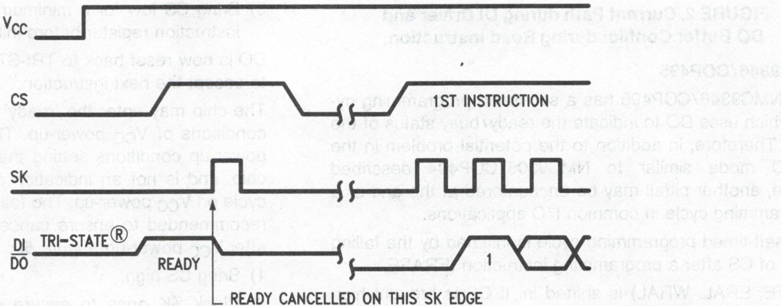
FIGURE 3. Programming Cycle with 4-Wire Interface

NMC9346 Timing Diagrams (Continued)


SK
CS
PROGRAM INSTRUCTION
(ERASE, WRITE, EPAL, WPAL)
DI/DO
1
START
BIT
te/w
TRI-STATE®
BUSY
READY
STATUS CHECK
TRI-STATE
* READY / BUSY STATUS INDICATOR
IS RESET BY THIS SK CLOCK EDGE
NEXT INSTRUCTION
1
START
BIT

TL/D/9213-4

FIGURE 4. Recommended Programming Cycle in Common I/O Configuration


VCC
CS
1ST INSTRUCTION
SK
DI/DO
TRI-STATE®
READY
1
READY CANCELLED ON THIS SK EDGE

TL/D/9213-5

FIGURE 5. Recommended Clocking Sequence on V_{CC} Power-Up in Common I/O Configuration

Error Detection and Correction Techniques for National Semiconductor's EEPROM Products

National Semiconductor
Application Note 482

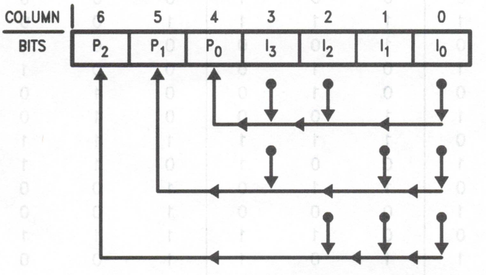
This application note provides the non-volatile memory system designer who cannot tolerate the very low failure rate associated with National Semiconductor's E²PROMs, with a method to assure data integrity and extend the life span of the product.

With a minimum additional parts cost, the following error detection and correction techniques allow the designer to extend the usable life of an EEPROM device. The technique is applicable for applications requiring 100,000 or more erase/write cycles per register.

All EEPROMs fail with extended erase/write cycling. National Semiconductor EEPROMs fail in a statistically predictable and well behaved fashion as the number of erase/write cycles increase. The failure of one bit cell does not influence the operation of adjacent bit cells. Since bit failure is a gradual wearout phenomenon which only affects discrete cell locations one at a time, it is possible to apply simple encoding techniques which can determine the locations of cell failures so that faltering memory addresses can be avoided in the future.

Single parity checking is the simplest way to check for errors in a binary code. In a parity checking system an extra-parity-bit is chosen so that the number of 1s in the block of data, including the parity bit, is even. In practice this is accomplished using modulo 2 addition (i.e., 0 + 0 = 0; 0 + 1 = 1; 1 + 0 = 1; 1 + 1 = 0; 0 + 0 + 1 = 1; etc.). Modulo 2 addition is quickly accomplished through an exclusive OR gate. When the data is read back, the number of ones are counted and the sum is checked to see if it is odd or even. An odd sum is an indication that an error occurred in the data. This method of single parity checking can detect the occurrence of an error in a block but it cannot be used to determine the exact location of the error to correct the bad data.

A natural extension of single parity checking is the Hamming code. A Hamming code uses several parity checks, instead of just one. This allows errors to be corrected as well as detected. Using bits in blocks of 7, where 4 of the bits are information and 3 are parity allows for error detection and correction of any single bit within the block, including the parity bits themselves.



TL/D/9214–1

FIGURE 1. Computation Scheme for Parity Bits Using Hamming Code

The initial parity is calculated as shown in *Figure 1.* The parity bits are in columns 4, 5 and 6, while the actual information bits are in columns 0, 1, 2, and 3. The contents of each parity bit comes from summing the contents of a unique combination of three of the four information bits. The parity bit is chosen so that this sum will be an even number when added to the parity bit itself. Notice that each one of the parity bits calculates its contents by using different combinations of the data bits. Every data bit in the block has its information read at least twice. Using this overlapping scheme is what allows the code to correct errors.

Since there are only 4 bits of information there can be only $2^4 = 16$ possible combinations of 1s and 0s. These 16 possible correct combinations are listed on the code word table in Table I. When the encoded block is read back from memory, the same parity coding scheme is used again on the information bits and compared to the original parity bits. This forms what is called a syndrome. If any errors have occurred in the 7-bit block their locations can be determined and the errors corrected. Table II shows the decoding matrix which is used on the syndromes to determine the location of an error. If no errors occurred the syndrome will be 000. Table III shows all the combinations of the 7-bit block. Note that there are only 128 possible variations of 1s and 0s in the block: (7 mistake combinations per block + 1 correct combination per block) × (16 possible block combinations). All these combinations can be stored in a table and called up quickly to check for possible data errors without the need to even create a syndrome upon reading a word. For example, suppose we want to store the data 1000. From Table I we see that the 7-bit block would be 1111000 after the Hamming code had been applied. If information bit 3 for example goes bad, then the new block would read 1110000. This is case number 112 in Table III, and we see that the correct information is 1000. With Table III available in the computer memory, the received codeword can be corrected automatically. An array of 128 bytes can provide both the corrected information and the syndrome information.

The 7-bit codeword works nicely with National Semiconductor's serial EEPROMs because they are organized as arrays of 16-bit registers. Each 16 bit register is modified or accessed with a simple-serial protocol. The 16-bit unit can be partitioned two eight-bit bytes. Each byte can contain a seven-bit codeword and one-bit flag that indicates whether an error has been previously detected in the byte. This scheme provides one byte of error corrected information per 16-bit register. Slightly more elaborate systems can be used which will detect and correct more errors if additional parity bits are added to the data.

TABLE I. Encoding Table for Hamming Code

	Sixteen Code Words						
	Parity Bits			Information Bits			
	P 2	P 1	P 0	I 3	I 2	I 1	I 0
0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	1
2	1	0	1	0	0	1	0
3	0	1	1	0	0	1	1
4	0	1	1	0	1	0	0
5	1	0	1	0	1	0	1
6	1	1	0	0	1	1	0
7	0	0	0	0	1	1	1
8	1	1	1	1	0	0	0
9	0	0	1	1	0	0	1
10	0	1	0	1	0	1	0
11	1	0	0	1	0	1	1
12	1	0	0	1	1	0	0
13	0	1	0	1	1	0	1
14	0	0	1	1	1	1	0
15	1	1	1	1	1	1	1

TABLE II. Syndrome Decoding Table for Hamming Code

Syndrome			Meaning
0	0	0	No error detected
0	0	1	Check bit 0 in error
0	1	0	Check bit 1 in error
0	1	1	Information bit 2 corrected
1	0	0	Check bit 2 in error
1	0	1	Information bit 1 corrected
1	1	0	Information bit 0 corrected
1	1	1	Information bit 3 corrected

With this added data protection the reliability of EEPROMs can be extended because the probability of two or more cells failing on the same codeword is low. To illustrate the Hamming code, an experiment on 16 devices with 1k bits each was conducted. The experiment results are shown in Table IV. While the first bit failure was detected somewhere between 12,589 and 15,849 cycles, the Hamming code just described would have protected against the loss of data until somewhere between 79,433 and 100,000 erase/write cycles. Notice that 55 bit failures were indicated when the first Hamming code failure was detected. This is to be expected because a Hamming failure will not occur until two or more bits within a particular group of seven bits have failed.

TABLE III. Information Retrieval Table for All Possible Combinations of Single-Bit-Correct Hamming Code

	Received Codeword							Syndrome Bits			Corrected Information			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1	1	0	0	0	0	0
2	0	0	0	0	0	1	0	1	0	1	0	0	0	0
3	0	0	0	0	0	1	1	0	1	1	0	1	1	1
4	0	0	0	0	1	0	0	0	1	1	0	0	0	0
5	0	0	0	0	1	0	1	1	0	1	0	1	1	1
6	0	0	0	0	1	1	0	1	1	0	0	1	1	1
7	0	0	0	0	1	1	1	0	0	0	0	1	1	1
8	0	0	0	1	0	0	0	1	1	1	0	0	0	0
9	0	0	0	1	0	0	1	0	0	1	1	0	0	1
10	0	0	0	1	0	1	0	0	1	0	1	0	1	0
11	0	0	0	1	0	1	1	1	0	0	1	0	1	1
12	0	0	0	1	1	0	0	1	0	0	1	1	0	0
13	0	0	0	1	1	0	1	0	1	0	1	1	0	1
14	0	0	0	1	1	1	0	0	0	1	1	1	1	0
15	0	0	0	1	1	1	1	1	1	1	0	1	1	1
16	0	0	1	0	0	0	0	0	0	1	0	0	0	0
17	0	0	1	0	0	0	1	1	1	1	1	0	0	1
18	0	0	1	0	0	1	0	1	0	0	0	0	1	0
19	0	0	1	0	0	1	1	0	1	0	0	0	1	1
20	0	0	1	0	1	0	0	0	1	0	0	1	0	0
21	0	0	1	0	1	0	1	1	0	0	0	1	0	1
22	0	0	1	0	1	1	0	1	1	1	1	1	1	0
23	0	0	1	0	1	1	1	0	0	1	0	1	1	1
24	0	0	1	1	0	0	0	1	1	0	1	0	0	1
25	0	0	1	1	0	0	1	0	0	0	1	0	0	1
26	0	0	1	1	0	1	0	0	1	1	1	1	1	0
27	0	0	1	1	0	1	1	1	0	1	1	0	0	1
28	0	0	1	1	1	0	0	1	0	1	1	1	1	0
29	0	0	1	1	1	0	1	0	1	1	1	0	0	1
30	0	0	1	1	1	1	0	0	0	0	1	1	1	0
31	0	0	1	1	1	1	1	1	1	0	1	1	1	0

TABLE III. Information Retrieval Table for All Possible Combinations of Single-Bit-Correct Hamming Code (Continued)

	Received Codeword							Syndrome Bits			Corrected Information			
32	0	1	0	0	0	0	0	0	1	0	0	0	0	0
33	0	1	0	0	0	0	1	1	0	0	0	0	0	1
34	0	1	0	0	0	1	0	1	1	1	1	0	1	0
35	0	1	0	0	0	1	1	0	0	1	0	0	1	1
36	0	1	0	0	1	0	0	0	0	1	0	1	0	0
37	0	1	0	0	1	0	1	1	1	1	1	1	0	1
38	0	1	0	0	1	1	0	1	0	0	0	1	1	0
39	0	1	0	0	1	1	1	0	1	0	0	1	1	1
40	0	1	0	1	0	0	0	1	0	1	1	0	1	0
41	0	1	0	1	0	0	1	0	1	1	1	1	0	1
42	0	1	0	1	0	1	0	0	0	0	1	0	1	0
43	0	1	0	1	0	1	1	1	1	0	1	0	1	0
44	0	1	0	1	1	0	0	1	1	0	1	1	0	1
45	0	1	0	1	1	0	1	0	0	0	1	1	0	1
46	0	1	0	1	1	1	0	0	1	1	1	0	1	0
47	0	1	0	1	1	1	1	1	0	1	1	1	0	1
48	0	1	1	0	0	0	0	0	1	1	0	1	0	0
49	0	1	1	0	0	0	1	1	0	1	0	0	1	1
50	0	1	1	0	0	1	0	1	1	0	0	0	1	1
51	0	1	1	0	0	1	1	0	0	0	0	0	1	1
52	0	1	1	0	1	0	0	0	0	0	0	1	0	0
53	0	1	1	0	1	0	1	1	1	0	0	1	0	1
54	0	1	1	0	1	1	0	1	0	1	0	1	0	0
55	0	1	1	0	1	1	1	0	1	1	0	0	1	1
56	0	1	1	1	0	0	0	1	0	0	1	0	0	0
57	0	1	1	1	0	0	1	0	1	0	1	0	0	0
58	0	1	1	1	0	1	0	0	0	1	1	0	1	0
59	0	1	1	1	0	1	1	1	1	1	0	0	1	1
60	0	1	1	1	1	0	0	1	1	1	0	1	0	0
61	0	1	1	1	1	0	1	0	0	1	1	1	0	1
62	0	1	1	1	1	1	0	0	1	0	1	1	1	0
63	0	1	1	1	1	1	1	1	0	0	1	1	1	1
64	1	0	0	0	0	0	0	1	0	0	0	0	0	0
65	1	0	0	0	0	0	1	0	1	0	0	0	0	1
66	1	0	0	0	0	1	0	0	0	1	0	0	1	0
67	1	0	0	0	0	1	1	1	1	1	1	0	1	1
68	1	0	0	0	1	0	0	1	1	1	1	1	0	0
69	1	0	0	0	1	0	1	0	0	1	0	1	0	1
70	1	0	0	0	1	1	0	0	1	0	0	1	1	0
71	1	0	0	0	1	1	1	1	0	0	0	1	1	1
72	1	0	0	1	0	0	0	0	1	1	1	1	0	0
73	1	0	0	1	0	0	1	1	0	1	1	0	1	1
74	1	0	0	1	0	1	0	1	1	0	1	0	1	1
75	1	0	0	1	0	1	1	0	0	0	1	0	1	1
76	1	0	0	1	1	0	0	0	0	0	1	1	0	0
77	1	0	0	1	1	0	1	1	1	0	1	1	0	0
78	1	0	0	1	1	1	0	1	0	1	1	1	0	0
79	1	0	0	1	1	1	1	0	1	1	1	0	1	1

TABLE III. Information Retrieval Table for All Possible Combinations of Single-Bit-Correct Hamming Code (Continued)

	Received Codeword							Syndrome Bits			Corrected Information			
80	1	0	1	0	0	0	0	1	0	1	0	0	1	0
81	1	0	1	0	0	0	1	0	1	1	0	1	0	1
82	1	0	1	0	0	1	0	0	0	0	0	0	1	0
83	1	0	1	0	0	1	1	1	1	0	0	0	1	0
84	1	0	1	0	1	0	0	1	1	0	0	1	0	1
85	1	0	1	0	1	0	1	0	0	0	0	1	0	1
86	1	0	1	0	1	1	0	0	1	1	0	0	1	0
87	1	0	1	0	1	1	1	1	0	1	0	1	0	1
88	1	0	1	1	0	0	0	0	1	0	1	0	0	0
89	1	0	1	1	0	0	1	1	0	0	1	0	0	1
90	1	0	1	1	0	1	0	1	1	1	0	0	1	0
91	1	0	1	1	0	1	1	0	0	1	1	0	1	1
92	1	0	1	1	1	0	0	0	0	1	1	1	0	0
93	1	0	1	1	1	0	1	1	1	1	0	1	0	1
94	1	0	1	1	1	1	0	1	0	0	1	1	1	0
95	1	0	1	1	1	1	1	0	1	0	1	1	1	1
96	1	1	0	0	0	0	0	1	1	0	0	0	0	1
97	1	1	0	0	0	0	1	0	0	0	0	0	0	1
98	1	1	0	0	0	1	0	0	1	1	0	1	1	0
99	1	1	0	0	0	1	1	1	0	1	0	0	0	1
100	1	1	0	0	1	0	0	1	0	1	0	1	1	0
101	1	1	0	0	1	0	1	0	1	1	0	0	0	1
102	1	1	0	0	1	1	0	0	0	0	0	1	1	0
103	1	1	0	0	1	1	1	1	1	0	0	1	1	0
104	1	1	0	1	0	0	0	0	0	1	1	0	0	0
105	1	1	0	1	0	0	1	1	1	1	0	0	0	1
106	1	1	0	1	0	1	0	1	0	0	1	0	1	0
107	1	1	0	1	0	1	1	0	1	0	1	0	1	1
108	1	1	0	1	1	0	0	0	1	0	1	1	0	0
109	1	1	0	1	1	0	1	1	0	0	1	1	0	1
110	1	1	0	1	1	1	0	1	1	1	0	1	1	0
111	1	1	0	1	1	1	1	0	0	1	1	1	1	1
112	1	1	1	0	0	0	0	1	1	1	1	0	0	0
113	1	1	1	0	0	0	1	0	0	1	0	0	0	1
114	1	1	1	0	0	1	0	0	1	0	0	0	1	0
115	1	1	1	0	0	1	1	1	0	0	0	0	1	1
116	1	1	1	0	1	0	0	1	0	0	0	1	0	0
117	1	1	1	0	1	0	1	0	1	0	0	1	0	1
118	1	1	1	0	1	1	0	0	0	1	0	1	1	0
119	1	1	1	0	1	1	1	1	1	1	1	1	1	1
120	1	1	1	1	0	0	0	0	0	0	1	0	0	0
121	1	1	1	1	0	0	1	1	1	0	1	0	0	0
122	1	1	1	1	0	1	0	1	0	1	1	0	0	0
123	1	1	1	1	0	1	1	0	1	1	1	1	1	1
124	1	1	1	1	1	0	0	0	1	1	1	0	0	0
125	1	1	1	1	1	0	1	1	0	1	1	1	1	1
126	1	1	1	1	1	1	0	1	1	0	1	1	1	1
127	1	1	1	1	1	1	1	0	0	0	1	1	1	1

TABLE IV. Hamming Code Experimental Demonstration on 16 Devices of 1k Bits Each

Erase/Write Cycles	Total Bit Failures	Total Codeword Failures	Percent Bit Failures	Percent Codeword Failures
1000	0	0	0.00%	0.00%
1259	0	0	0.00%	0.00%
1585	0	0	0.00%	0.00%
1995	0	0	0.00%	0.00%
2512	0	0	0.00%	0.00%
3162	0	0	0.00%	0.00%
3981	0	0	0.00%	0.00%
5012	0	0	0.00%	0.00%
6310	0	0	0.00%	0.00%
7943	0	0	0.00%	0.00%
10000	0	0	0.00%	0.00%
12589	1	0	0.01%	0.00%
15849	1	0	0.01%	0.00%
19953	1	0	0.01%	0.00%
25119	1	0	0.01%	0.00%
31623	3	0	0.02%	0.00%
39811	4	0	0.02%	0.00%
50119	10	0	0.06%	0.00%
63096	16	0	0.10%	0.00%
79433	55	1	0.34%	0.05%
100000	103	3	0.63%	0.15%

Using the NMC93CSxx Family

National Semiconductor
Application Note 507

INTRODUCTION

This application note is intended for system designers interested in using the NMC93CSxx family of CMOS serial EEPROM devices. These devices are well-suited for applications that call for non-volatile, writeable memory. The NMC93CSxx devices offer the additional benefit of selective write-protection by use of an on-chip protect register. This allows the device to perform both read-only memory (ROM) and EEPROM functions on the same chip.

EEPROMs are useful in a wide variety of applications because of their non-volatile, writeable characteristics. The devices can be used for applications that store configuration values, such as feature telephones, station presets on radios, and PC boards with configuration DIP switches and jumpers. Adaptive, closed-loop systems, such as environment controllers and motor controllers, can use EEPROMs to store loop control variables. Data logging is another of the many application areas of EEPROMS.

The NMC93CSxx family can support a new set of applications because of their additional capability to perform selective ROM functions. ROM is a requirement when the integrity of data stored in a device must be guaranteed. Applications can make use of this feature while at the same time allocating other locations in the device to operate as EEPROM.

The NMC93CSxx family devices exhibit extremely low power consumption due to the low drive requirements of their serial interface and the use of CMOS technology. The serial interface also provides the designer with a flexible interface mechanism allowing the devices to be easily designed into microcontroller and microprocessor systems. In microcontroller systems, or those with a serial bus, the devices can be connected with little or no support logic. The serial interface allows the device to fit in a smaller package, resulting in minimal board space requirements.

TABLE I. NMC93CSxx Family

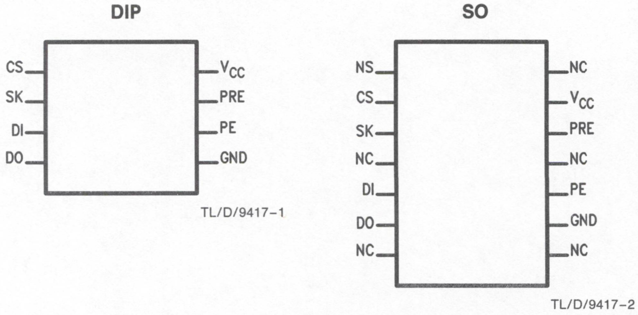
Device	Memory Size
NMC93CS06	16 x 16
NMC93CS26	32 x 16
NMC93CS46	64 x 16
NMC93CS56	128 x 16
NMC93CS66	256 x 16

NMC93CSxx FAMILY DESCRIPTION

The NMC93CSxx family is a set of 5 CMOS serial EEPROM devices with on-chip write-protection logic. The members of the family are differentiated by their memory array size, which ranges from 256 to 4096 bits organized 16 bits wide (see Table I). Because the devices use a serial interface, the pinout for each family member is identical. The devices conform to the MICROWIRE interface and are backwards compatible with previous National serial EEPROM devices (see *Figure 1*).

A set of 10 instructions are provided to control device operation. The general format of the instructions is a start bit (logic 1) followed by opcode, register address and data fields. The register address for the NMC93CS06/26/46 is 6 bits, while the register address for the NMC93CS56/66 is 8 bits. Data is shifted into the device on the D1 pin, and out on the DO pin following a low to high transition of SK. CS must be high to access the device (see Table 2).

A read operation is performed by issuing the start bit, the appropriate opcode (10), and the desired register address. The device responds by shifting out a dummy bit (logic 0) followed by the data in the selected register. The device will continue to shift data from subsequent registers as long as SK is active (non-volatile shift register mode). Write operations are performed by issuing the start bit, opcode (01), register address, and 16 bits of data. CS must be brought low to initiate the self-timed programming cycle, which includes an automatic erase cycle. CS can then be brought high to monitor DO (low to high transition) for completion of the cycle.



TL/D/9417-1

TL/D/9417-2

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Serial In
DO	Serial Out
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

FIGURE 1. NMC93CSxx Device Pinout

TABLE II. NMC93CSxx Instruction Set

Instruction	SB	Op Code	Address	Data	PRE	PR	Comments
READ	1	10	A_X–A_0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A_X–A_0	D15–D0	0	1	Write register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Write all register. Valid only when "protect register" is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in "protect register".
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A_X–A_0		1	1	Programs address into "protect register". Thereafter, memory address < the address in "protect register" are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the "protect register" cannot be altered.

The protect register is used to write protect a segment of registers. The value contained in the protect register designates the first address of the protected segment. All subsequent register locations are write-protected.

USING THE PROTECT REGISTER

The incorporation of the protect register in NMC93CSxx devices sets the family apart from other CMOS serial EEPROMs. Including a protect register allows the devices to function as EEPROM and ROM simultaneously. The distribution of EEPROM and ROM in a device is determined by the value in the protect register. The distribution of EEPROM and ROM can be changed in the system by changing the protect register value.

ROM applications typically require that data storage be non-volatile so that no changes will occur when power is turned off and read-only so that changes won't occur under any other circumstances. EEPROMs are non-volatile, but aren't read-only. An EEPROM will function as a ROM if write operations are never attempted or if any attempted write fails.

The protect register is valuable when an application requires a mix of EEPROM and ROM. A NMC93CSxx device can be made less susceptible to write problems without using the protect register. The entire device may be made read-only by grounding PE. System software can be implemented to avoid writing to read-only locations and limit when write instructions may be performed by making use of the write enable (WEN) and disable (WDS) instructions. The device would only be susceptible to a write problem if a system failure caused an illegal write or some external source with access to the device abused its write privileges. Use of the protect register under system control would be somewhat safer, but the device would still be subject to the above-mentioned problems. Write access to the protect register must be inhibited for the protected locations to be truly read-only.

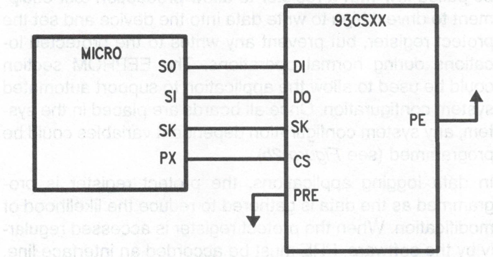


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FIGURE 2a. Protect Register Disabled

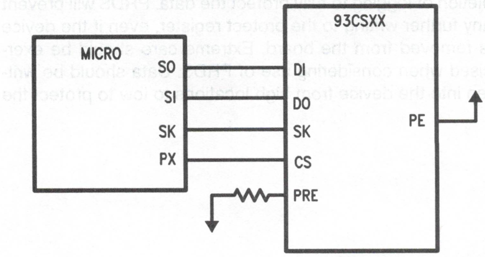

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FIGURE 2b. Protect Register Enabled with Pulldown

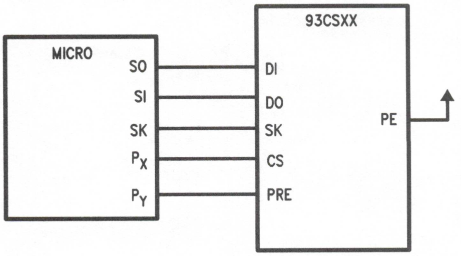

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FIGURE 2c. Protect Register Enabled

ROM devices are most often programmed with data before insertion into a PC board. This approach is applicable to NMC93CSxx devices. In a microcontroller system, program code or data could be off-loaded from the internal ROM of the microcontroller into a ROM section in an NMC93CSxx device. An EEPROM section could be allocated for any writeable data, such as configuration data values. ROM is desirable in this application because any spurious writes that could corrupt the program will be prevented, a smaller internal microcontroller ROM is possible and if ROM code or data needed alteration, it would be much easier and cheaper to reprogram a NMC93CSxx device than the internal ROM of the microcontroller. In manufacturing, the ROM data and the protect register value would be programmed into the device, and the protect register enabled before PC board insertion. The PRE pin would be tied low on the board to prevent write access to the protect register (see *Figure 2a*).

Another application for these devices is in systems that support automated production. Production information, such as date codes and status, would be programmed into the NSC93CSxx on a board as it progressed through each step of the production process. Board identification (serial number) and fixed configuration information could also be programmed into the device as a last step. The PRE pin would be pulled low with a resistor to allow production test equipment to drive it high to write data into the device and set the protect register, but prevent any writes to the protected locations during normal operations. The EEPROM section could be used to allow the application to support automated system configuration. Once all boards are placed in the system, any system configuration dependent variables could be programmed (see *Figure 2b*).

In data logging applications, the protect register is programmed as the data is gathered to reduce the likelihood of modification. When the protect register is accessed regularly by the software, PRE must be accorded an interface line, usually a port pin that is controlled by software. The protect register disable (PRDS) instruction must be used upon completion of logging to fully protect the data. PRDS will prevent any further writing to the protect register, even if the device is removed from the board. Extreme care should be exercised when considering use of PRDS. Data should be written into the device from high locations to low to protect the data as it is read in. In addition, the protect register then serves the dual purpose of being a pointer to the last location written, simplifying software and saving a variable location (see *Figure 2c*).

INTERFACING TO THE NMC93CSxx FAMILY

COP800 Interface

The COP800 family is a set of 8-bit CMOS microcontrollers. The family members differ by program and data memory, on-chip peripherals, and package size. Some members have on-chip EEPROM for program or data memory. The devices with EEPROM for program memory are only intended for development purposes. All members of the family have an on-chip MICROWIRE™ interface.

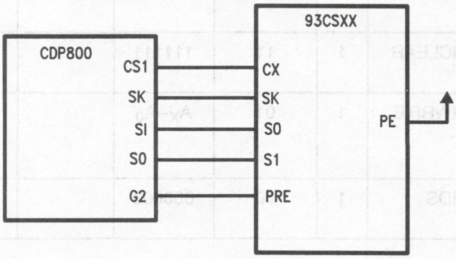

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FIGURE 3. MICROWIRE Interface

The COP800 family provides three options when interfacing to a NMC93CSxx device. The interface could be designed by using the COP800 device parallel port pins under software control, on-chip UART if available, or the MICROWIRE interface port. The most attractive option for the interface is the MICROWIRE because NMC93CSxx devices connect directly to it.

The MICROWIRE port provides a serial clock (SK), serial input (SI), and serial output (SO). These lines are directly connected to SK, DO and DI of the EEPROM. COP800 parallel port pins can be used for providing CS, PE and PRE. If PE or PRE are static in the application, they can be tied low or high. No other hardware is required for the interface (see *Figure 3*). In a system with multiple devices on the MICROWIRE, additional logic may be required to perform chip selection. If available, parallel port pins could be used for additional chip selects. Otherwise, a PAL device could be designed so that chip selects are set serially preceding any serial device operations.

```
;WREEPROM-WRITE DATA TO EEPROM
;
;THIS ROUTINE WILL WRITE A SPECIFIED NUMBER OF BYTES
;TO THE EEPROM USING THE MICROWIRE INTERFACE. THIS CODE
;ASSUMES THE SHIFT CLOCK RATE IS 1/2 THE XTAL FREQUENCY.
;THE ARGUMENT STRING CONSISTS OF A BYTE COUNT, OPCODE,
;REGISTER ADDRESS, FOLLOWED BY A DATA STREAM.
;
WREEPROM: LD    A,[B+]   ;COPY BYTE COUNT
          X     A,x'F0   ;
          SBIT  1,x'D4   ;CHIP SELECT
          SBIT  7,x'E9   ;SEND START BIT
          SBIT  2,x'EF   ;
          RBIT  2,x'EF   ;
SLOOP:    LD    A,[B+]   ;SEND DATA BYTES
          X     A,x'E9   ;
          SBIT  2,x'EF   ;
BIT_TST:  IFBIT 2,x'EF   ;STILL BUSY?
          JMP   BIT_TST  ;
          DRSZ  x'F0     ;DONE SENDING?
          JMP   SLOOP    ;
          RBIT  1,x'D4   ;DROP CS
          RET
```

FIGURE 4. COP800 MICROWIRE Write Routine

```
;RDEEPROM-READ DATA FROM EEPROM
;
;THIS ROUTINE WILL READ A SPECIFIED NUMBER OF BYTES FROM
;THE EEPROM USING THE MICROWIRE. THE CODE ASSUMES THAT THE
;SHIFT CLOCK IS PROGRAMMED AT 1/2 THE INSTRUCTION CLOCK RATE.
;THE ARGUMENTS PASSED TO THIS ROUTINE ARE A BYTE COUNT, OPCODE,
;AND REGISTER ADDRESS, POINTED TO BY B.
;THE BYTE COUNT AND DATA READ ARE POINTED AT BY B ON RETURN.
;
RDEEPROM:  LD    A,x'FE     ;SAVE POINTER
           X     A,x'F1     ;
           LD    A,[B+]     ;COPY BYTE COUNT
           X     A,x'F0     ;
           SBIT  1,x'D4     ;CHIP SELECT
           SBIT  7,x'E9     ;SEND START BIT
           SBIT  2,x'EF     ;
           RBIT  2,x'EF     ;
           LD    A,[B]      ;SEND INSTRUCTION
           X     A,x'E9     ;
           SBIT  2,x'EF     ;
TST1:      IFBIT 2,x'EF     ;BUSY?
           JMP   TST1       ;
           SBIT  2,x'EF     ;GET DUMMY BIT?
           RBIT  2,x'EF     ;
RLOOP:     CLRA             ;GET DATA BYTES
           SBIT  2,x'EF     ;
TST2:      IFBIT 2,x'EF     ;BUSY?
           JMP   TST2       ;
           X     A,x'E9     ;
           X     A,[B+]     ;
           DRSZ  x'F0       ;DONE GETTING?
           JMP   RLOOP      ;
           LD    A,x'F1     ;RESTORE POINTER
           X     A,x'FE     ;
           RBIT  1,x'D4     ;DROP CHIP SELECT
           RET
```

FIGURE 5. COP800 MICROWIRE Read Routine

Inside a COP800 device the MICROWIRE hardware consists of an 8-bit shift register (SIO), a control bit (BUSY) in the program status word (PSW), and a control register (CNTRL), BUSY is set by the control program to initiate a shift operation and is automatically reset when eight bits have been shifted. BUSY can be reset by the program for shift operations of less than eight bits. CNTRL is used to set the MICROWIRE mode and rate of SK. SK can be set to a divide by 2, 4, or 8 of the instruction clock rate. The MSEL bit of CNTRL sets the MICROWIRE to Master mode or Slave mode. In Master mode, a device will generate SK and in Slave mode it will receive SK. Master mode is used to interface to an NMC93CSxx device.

In addition to initializing the interface, software rountines are required to control data transfers to and from the EEPROM through the MICROWIRE port. The same routines used to read and write to the EEPROM can be used to execute the NMC93CSxx instructions, including accessing the protect register. The only extra step required to access the protect register is that PRE must be set high.

A routine must access SIO to perform an NMC93CSxx instruction. Since the MICROWIRE shift register is only eight bits wide, multiple accesses are required to complete an instruction. In addition, instructions aren't byte-aligned; routines must align the operation. Instructions can be byte-aligned by sending a single start bit followed by a byte of opcode and address. A start bit can be sent by using the set bit (SBIT) instruction to set BUSY, followed by the rest bit (RBIT) instruction when SK is being divided by two, or by sending a byte with seven leading zeros as dummy bits and a single one for the start bit. The NMC83CS56/66 devices require two more bits to be sent for alignment because of their larger address space. In this case it is easier to send the byte with leading zeros.

The write routine, WREEPROM, sets CS to select the device, then writes a single start bit, followed by a byte of opcode and address, and two bytes of data. The bytes sent are stored as a string preceeded by a byte-count. The byte count must, obviously, be three for a write. This routine can be used to perform the other write-only NMC93CSxx instructions by setting the byte-count and data string appropriately. CS is brought low to initiate the automatic erase/write cycle. The routine doesn't bring CS back high to check for completion of the cycle. This allows the routine to be used to perform the other NMC93CSxx instructions and the control program to perform other tasks during the cycle. If the program is unsure of cycle completion, DO should be checked before initiating another instruction (see *Figure 4*).

The read routine, RDEEPROM, sets CS and sends the start bit, opcode and address in the same manner as the write routine. The routine then reads a dummy bit (logic 0) from the EEPROM and the number of bytes of data specified by the byte-count. The dummy bit is read in exactly the same way as a start bit is sent (see *Figure 5*).

HPC Interface

The HPC family is a set of high performance 16-bit microcontrollers. Like the COPS microcontrollers, the HPC devices are MICROWIRE compatible, providing an excellent means of interfacing to NMC93CSxx devices. Though, a software controlled interface using parallel port pins could be used, as well as an on-chip UART.

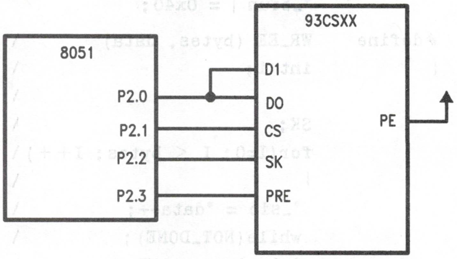

FIGURE 7. 8051 Interface

```
#define   SET_CS   *_iporta|=0x40   /* set chip select*/
#define   DROP_CS  *_iporta & = 0xFB /* lower chip select*/
#define   SIO      0xD6             /* SIO register location*/
#define   PORTA    0xC8             /* PORT A location*/
#define   IRPD     0xD2             /* IRPD register location*/
#define   NOT_DONE I(*_Irpd & 0x04) /* DONE flag set if true*/
#define   BFUN     0xF4             /* BFUN register*/
#define   SK                        \
          *_bfun & = 0xBF           \
          *_bfun | = 0x40;

#define   WR_EE (bytes, data)       \
{         int i;                    \
                                    \
          SK;                       \
          for(I=0; I < bytes; I++)  \
          {                         \
           *_sio = *data++;         \
           while(NOT_DONE);         \
           *_irpd & = 0xFB;         \
          }                         \
}
/* Global Definitions*/
char      *_sio = SIO;
char      *_iporta = PORTA;
char      *_irpd = IRPD;
char      *_bufn = BFUN;

wr_eeprom(bytes,data)
int       bytes;   /* byte count*/
char      *data;   /* data buffer*/
{

          SET_CS;
          WR_EE;
          DROP_CS;
}

rd_eeprom(bytes, data)
int       bytes;   /* byte count*/
char      *data;   /* buffer pointer*/
{

          SET_CS;
          WR_EE (1, data);
          SK;                       /* get dummy bit*/
          for (i = 0; i < bytes; I ++){
            *data ++ = *_sio;
            while(NOT_DONE);
            *_irpd & = 0xFB;
          }
          DROP_CS;
}
```

FIGURE 6. HPC C Language Interface Routine

```
;
;SNDBYT - SHIFTS 8 BITS OF DATA TO EEPROM
;
;THIS ROUTINE SHIFTS A BYTE POINTED AT BY RO
;ASSUMES CHIP SELECT ALREADY ACTIVE (HIGH)
;
SNDBYT     MOV   B,#8     ;LOAD SHIFT COUNT
           MOV   A,@RO    ;GET BYTE
S_LOOP:    RLC   A        ;SHIFT
           MOV   P2.0,C   ;SEND BIT
           CLR   P2.2     ;SK
           SETB  P2.2     ;
           DJNZ  B,S_LOOP ;DONE?
           RET
;
;WREEPROM - WRITE DATA TO EEPROM
;
;THIS ROUTINE WRITES A SPECIFIED NUMBER OF BYTES TO THE
;EEPROM USING SNDBYT UTILITY ROUTINE. THE DATA IS POINTED AT
;BY THE RO REGISTER AND CONSISTS OF BYTE COUNT, OPCODE/REG ADDR
;AND DATA BYTES. DO IS SET HIGH TO AVOID CONTENTION.
;
WREEPROM: MOV    R2,@RO      ;COPY BYTE COUNT
          INC    RO          ;
          SETB   P2.1        ;CHIP SELECT
          CLR    P2.2        ;START BIT
          SETB   P2.2        ;
WR_LOOP:  LCALL  SNDBYT      ;WRITE DATA BYTES
          INC    RO          ;
          DJNZ   R2,WR_LOOP;
          SETB   P2.0        ;DEFAULT DO HIGH
          CLR    P.21        ;DESELECT/PROGRAM
          RET
```

FIGURE 8. 8051 Parallel Port Pin Interface—Write Routines

The MICROWIRE interface provides signals for SK, SI and SO. CS, PE and PRE signals can be provided by using parallel port pins. Port A on the HPC is allocated for general use and is ideal for this function. When used in Master mode, the clock rate for the MICROWIRE is set by programming the appropriate value into the DIVBY register. The 8-bit SIO register is used as a buffer for serial operations.

Unlike the COP800 microcontrollers, the HPC does not use a BUSY bit to control shifting. The DONE flag in the IRPD register is polled to determine completion of a shift operation. A single bit can be transferred by changing the mode of the SK pin back to a general purpose port pin (B.6). This is accomplished by clearing bit six of the port B function register (BFUN). If port B bit six is high, the pin will go high immediately clocking the EEPROM.

```
;RCVBYT - READ A BYTE OF SERIAL DATA
;
;THIS ROUTINE WILL SERIALLY READ 8 BITS OF DATA FROM THE PORT PIN
;AND STORE THE DATA IN THE LOCATION POINTED AT BY RO
;
RCVBYT:     MOV   B,#8        ;LOAD SHIFT COUNT
R_LOOP:     CLR   P2.2        ;SK
            SETB  P2.2        ;
            MOV   C,P2.0      ;GET BIT
            RLC   A           ;SHIFT
            DJNZ  B,R_LOOP    ;DONE?
            MOV   @RO,A       ;STORE DATA
            RET
;RDEEPROM - READ DATA FROM EEPROM
;
;THIS ROUTINE WILL READ A SPECIFIED NUMBER OF BYTES FROM
;THE EEPROM USING THE RCVBYT ROUTINE. INPUT ARGUMENT STRING IS
;A BYTE COUNT, AND OPCODE/REGISTER ADDRESS. ON RETURN, RO POINTS
;TO A STRING CONTAINING THE BYTE COUNT FOLLOWED BY DATA BYTES
;
RDEEPROM:   MOV   R2,@RO      ;COPY BYTE COUNT
            PUSH  RO          ;SAVE POINTER
            INC   RO          ;
            SETB  P2.1        ;CHIP SELECT
            CLR   P2.2        ;START BIT
            SETB  P2.2        ;
            LCALL SNDBYT      ;SEND INSTRUCTION
            SETB  P2.0        ;DEFAULT DO HIGH
            CLR   P2.2        ;DUMMY BIT
            SETB  P2.2        ;
RD_LOOP     LCALL RCVBYT      ;GET DATA BYTES
            INC   RO          ;
            DJNZ  R2,RD_LOOP;DONE?
            POP   RO          ;RESTORE POINTER
            CLR   P2.1        ;DESELECT
            RET
```

FIGURE 9. 8051 Parallel Port Pin Interface Read Routines

The HPC supports program development in the C language. The software routines to support an HPC interface are similar to those for the COP800, except that they are written in C (see *Figure 6*). The main difference is how the start bit and dummy read bit are handled. Since the HPC supports the C language, core routines are written utilizing macros, eliminating the overhead of an extra level of subroutine calls.

8051 Interface

The 8051 offers two interface alternatives for the NMC93CSxx family; the first uses parallel port pins under software control and the second is based on using the on-chip serial port. Both interfaces require a minimum number of device pins and no support logic. The main differences are that the serial port is faster and requires less software.

The first choice for discussion is the use of the port pins. The 8051 has four 8-bit bidirectional I/O ports. The ports are accessed through a special function register. The port registers are bit addressable which facilitates their use in this application. The minimum interface requires the use of only three port pins. A pin for CS, SK, and one connected to both DI and DO (see *Figure 7*). A two wire interface is possible by tying CS active, but this leaves the device in the active (high power) state and prevents the device programming cycle from being executed.

It is not necessary to have separate lines for DI and DO because DO is placed in a high-Z condition during write operations. During a read operation the DI pin is driven to send the instruction to the EEPROM and DO outputs the dummy bit (0) and data. To prevent contention DI has to stop driving a high before DO can output the dummy bit. The 8051 doesn't drive a high, it uses internal pull-ups to obtain a high, so there is no contention problem. This may be a concern in other designs. The DO pin is driven when CS is brought high following a write operation to time completion of programming Contention will occur on the operation following a write if programming completion isn't checked. A dummy check can be used.

When using the port pins, one must consider that some of the port pins have alternate functions. For example, Port 3 pins 0 and 1 are also allocated for the serial port. Similarly, if the program being executed on the 8051 resides in external memory, then Ports 0 and 2 will serve as the system bus during external memory access.

The software support routines are primarily concerned with controlling the flow of data to/from the EEPROM. Because the 8051 is an 8-bit machine, two utility routines, SNDBYT and RCVBYT, are used to shift a byte of data to and from the NMC93CSxx.

The write routine, WREEPROM, raises CS to access the device, shifts out a start bit, then calls SNDBYT to shift out the opcode/register address byte, and other data bytes, as specified by the byte-count (see *Figure 8*).

The read routine, RDEEPROM, starts out by raising CS, sending a start bit, and using SNDBYT for the opcode/register address byte. The dummy bit is then shifted from the device and RCVBYT is called to shift in the number of bytes of data specified by the byte-count (see *Figure 9*).

```
;RDEEPROM - READS DATA FROM NMC93CSXX DEVICE
;
;THE ROUTINE READS A SPECIFIED NUMBER OF BYTES FROM
;THE EEPROM USING THE SERIAL PORT. RO POINTS TO AN ARGUMENT STRING
;CONTAINING THE BYTE COUNT AND THE OPCODE/REGISTER BYTE
;A STRING IS RETURNED CONTAINING THE BYTE COUNT FOLLOWED BY DATA.
RDEEPROM:
           PUSH    RO         ;SAVE POINTER
           MOV     R2,@RO     ;COPY BYTE COUNT
           INC     RO         ;
           SETB    P2.1       ;CHIP SELECT
           CLR     P3.1       ;SEND START BIT
           SETB    P3.1       ;
           MOV     SBUF       ;SEND INSTRUCTION
           JBC     TI$        ;DONE?
           CLR     TI         ;
           CLR     P3.1       ;GET DUMMY BIT
           SETB    P3.1       ;
           SETB    REN        ;GET DATA BYTES
RLOOP;     JBC     RI,$       ;DONE?
           CLR     RI         ;
           MOV     @RO,SBUF   ;
           INC     RO         ;
           DJNZ    R2,RLOOP   ;
           CLR     REN        ;
           CLR     P2.1       ;DESELECT
           POP     RO         ;RESTORE POINTER
           RET

;WREEPROM - WRITE DATA TO EEPROM
;
;THE ROUTINE WRITES A SPECIFIED NUMBER OF BYTES TO EEPROM
;POINTED AT BY RO. ARGUMENTS INCLUDE BYTE COUNT AND OPCODE/ADDRESS
;
WREEPROM:  MOV     R2,@RO     ;COPY BYTE COUNT
           INC     RO         ;
           SETB    P2.1       ;CHIP SELECT
           SETB    P3.0       ;START BIT
           CLR     P3.1       ;
           SETB    P3.1       ;
SLOOP:     MOV     SBUF,@RO   ;SEND DATA BYTES
           INC     RO         ;
           JBC     TI,$       ;DONE?
           DJNZ    R2,SLOOP   ;
           CLR     P2.1       ;DESELECT
           RET
```

FIGURE 10. 8051 Serial Port Read and Write Routines

8051 INTERFACE—SERIAL PORT

The 8051 serial port operates in one of four modes: 8-bit shift register, 8-bit UART and two different 9 bit UART modes. The 8-bit shift register mode (Mode 0) is preferred because it operates with no protocol, as opposed to the UART modes which send and receive packeted data. When in Mode 0, the 8051 RxD pin is used as a serial in/out pin and the shift clock is provided on the TxD pin. The TxD pin would be connected to SK and RxD would be connected to DI and DO on the NMC93CSxx device. CS, PE and PRE would be connected the same way as in the port pin interface.

When using the serial port in Mode 0, the serial port control register (SCON) must be programmed by setting the SM0 and SM1 bits (bits 7 and 6) to 0. The serial clock runs at a fixed rate of $1/12$ of the oscillator frequency. The maximum frequency for the serial clock on NMC93CSxx devices is 1 MHz. This means the 8051 can run with an oscillator frequency up to 12 MHz. After every eighth bit is received or transmitted the 8051 hardware will set either the receive interrupt (RI) or transmit interrupt (TI) bit in SCON. These bits may be polled, or used to generate interrupts.

The software routines for the serial port interface are virtually the same as those for the previous example. The only differences are that the 8051 serial port performs the same functions as the SNDBYT and RCVBYT routines. Instead of calling these routines, the REN bit is enabled to initiate reception and the data is read from the serial buffer (SBUF). For writing, the data is written into SBUF to perform the transfer. The routines poll the RI or TI bits. Because data transactions are synchronous, interrupts are not applicable (see *Figure 10*).

8096 INTERFACE

The 8096 is a 16-bit microcontroller. Like other microcontrollers, it interfaces easily to the NMC93CSxx devices. The use of parallel port pins or the on-chip serial port provide two interface options.

When implementing the parallel port pin interface, the choice of the port pins used is more critical because more of these pins have alternate functions. If the 8096 must perform external memory accesses, the use of Ports 3 and 4 becomes a problem because these two 8-bit ports make up the address/data bus. Port 0 pins are used for the analog input channels. Port 2 pins have alternate functions such as the serial port. Port 1 pins do not have alternate functions and may be preferred for use.

The 8096 provides an on-chip serial port which may be used for interfacing the NMC93CSxx devices. The serial port has 4 modes of operation. The mode of interest for this application is the shift register mode (Mode 0). The 8096 shift register mode serial clock rate is not a fixed rate. It is therefore the responsibility of the support software to program the baud rate appropriately.

INTERFACING NMC93CSxx WITH HIGH PERFORMANCE MICROPROCESSORS

High performance microprocessors like the NS32000, iAPX386 and the MC680x0 are usually implemented as central processor in computers and aren't directly involved with peripheral devices. Rather, these machines communicate over a backplane bus. These processors are designed for high speed, parallel data transfers. The NMC93CSxx devices could be used with these processors if a serial bus is implemented as part of the backplane bus. Typically, a serial bus would be used for system configuration or diagnostic purposes. Both the VME bus and Multibus II supply serial communication signals that may be used to interface NMC93CSxx devices to a high performance processor.

SUMMARY

The NMC93CSxx family can be used in a wide variety of applications. The devices provide a non-volatile, writeable memory that requires the least amount of board space, support logic and power. The protect register allows for a flexible mix of RAM and ROM. The previous examples illustrate that the NMC93CSxx family easily interfaces to microcontrollers and systems with a serial bus.

```
;RCYBYT - READ UTILITY ROUTINE
;
;THIS ROUTINE WILL READ 8 BITS OF DATA FROM THE SERIAL PORT
;THE DATA IS STORED IN THE LOCATION POINTED AT BY THE DX REGISTER.

RCVBYT:     LDB   AH,#8        ;LOAD SHIFT COUNT
BOP_SK:     ANDB  P2,#FBH      ;STROBE SK
            ORB   P2,#04H      ;
            JBS   P2,3,BIT_1   ;READ BIT
            ANDB  AL,#FEH      ;
            SJMP  R_SHIFT      ;
BIT_1:      ORB   AL,#01H      ;
R_SHIFT:    SHLB  AL,1         ;
            DECB  AH           ;DONE?
            JNE   BOP_SK       ;
            LDB   (DX),AL      ;SAVE DATA
            RET


;RDEEPROM - READ DATA FROM EEPROM
;
;SI, SK, CS, SO = P2[3 . . . 0]
;THIS ROUTINE WILL READ A SPECIFIED NUMBER OF BYTES FROM THE
;EEPROM AND STORE THE DATA. ARGUMENTS SUPPLIED TO THIS ROUTINE
;ARE A BYTE COUNT, OPCODE/REGISTER ADDRESS, AND ADDRESS FOR
;STORING THE DATA.
;
RDEEPROM:   PUSH  DX           ;SAVE POINTER
            LDB   BL,(DX)+     ;COPY BYTE COUNT
            ANDB  P2,#F0H      ;CHIP SELECT,START BIT
            ORB   P2,#03       ;
            ORB   P2,#04       ;
            LCALL SNDBYT       ;SEND INSTRUCTION
            ANDB  P2,#FBH      ;GET DUMMY BIT
            ORB   P2, #04H     ;
RD_LOOP:    LCALL RCVBYT       ;GET DATA BYTES
            INC   DX           ;
            DECB  BL           ;DONE?
            JNE   RD_LOOP      ;
            ANDB  P2,#FDH      ;DESELECT
            POP   DX           ;RESTORE POINTER
            RET
```

FIGURE 11. 8096 Port Pin Interface Read Routines

```
;SNDBYT - WRITE 8 BITS OF DATA TO PORT PIN
;
;THIS ROUTINE WILL WRITE 8 BITS OF DATA TO THE PORT PIN. THE
;DATA BYTE IS POINTED AT BY THE DX REGISTER.
;
SNDBYT:     LDB   AH,#8          ;LOAD SHIFT COUNT
            LDB   AL,(DX)        ;GET DATA BYTE
SLOOP:      JBS   AL,7,BIT_1     ;SEND BIT
            ANDB  P2,#FEH        ;
            SJMP  TOG_SK
BIT1:       ORB   P2,#01H        ;
TOG_SK:     ANDB  P2,#FBH        ;
            ORB   P2,#04H        ;
            SHLB  AL
            DECB  AH             ;DONE?
            JNE   SLOOP
            RET

;WREEPROM - WRITE DATA TO EEPROM
;
;SI, SK, CS, SO = P2[3..0]
;THIS ROUTINE WILL WRITE A SPECIFIED AMOUNT OF BYTES TO THE
;EEPROM. THE DATA TO BE WRITTEN IS POINTED AT BY THE DX REGISTER.
;THE ARGUMENTS INCLUDE THE BYTE COUNT, OPCODE/REGISTER ADDRESS,
;AND 1 OR MORE DATA BYTES.
;
WREEPROM:   LDB   BL,(DX)+       ;COPY BYTE COUNT
            ANDB  P2,#F0H        ;CHIP SELECT, START BIT
            ORB   P2,#03H        ;
            ORB   P2,#04H        ;
WR_LOOP:    LCALL SNDBYT         ;SEND DATA BYTES
            INC   DX
            DECB  BL             ;DONE?
            JNE   WR_LOOP
WR_EXIT:    ANDB  P2#FDH         ;DESELECT/PROGRAM
            RET
```

FIGURE 12. 8096 Parallel Port Pin Interface Write Routines

The Reliability of National Semiconductor's EEPROM Products

This applications note provides the non-volatile memory system designer with the necessary information to design reliable non-volatile memory subsystems. The first section is an introduction to EEPROM technology. Next, is a description of the intrinsic failure mechanisms common to all EEPROM devices. The third section is a description of the reliability aspects of National Semiconductor's manufacturing process.

INTRODUCTION TO EEPROM TECHNOLOGY

EEPROM Background

The Electrically Erasable Programmable Read Only Memory (EEPROM) is a non-volatile, fully static data storage device which is also electrically erasable. It can be erased and written rapidly without removing the chip from the end application system or using a PROM programmer. The technology allows for both byte- and chip-clear operations. These advantages are in contrast to UVPROMs which require removal from the system and total erasure of all the bits on the chip.

Technology Description

National Semiconductor's NMOS EEPROM devices utilize a 2.5 micron process. This technology was developed from the basic NMOS double poly process, which National Semiconductor's Memory Division has been using for about 10 years.

The new family of CMOS devices is based on National's 2 micron M^{2}CMOS process, which is the process National Semiconductor uses most widely for such diverse products as: Gate Arrays, Telecom, Microprocessing and many others. It is presently fabricated in one of the most modern, state-of-the-art, 6 inch wafer fab facilities in the world.

Device Description

National Semiconductor EEPROM devices utilize a double poly silicon gate process. *Figure 1* depicts the basic memory element in cross section. It is comprised of an N-channel transistor with an additional floating polysilicon gate sandwiched between the control gate and the transistor channel region. The gate structures are separated from each other and from the transistor channel and drain regions by silicon dioxide (SiO_2). A tunnel oxide which is less than 120 Angstroms thick is used in the region between the floating polysilicon gate and the N$^+$ drain region. National's E^2 Cell allows individual bit erasing and writing.

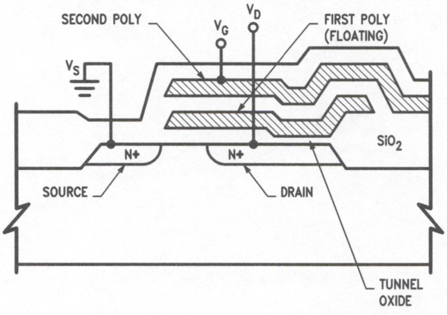

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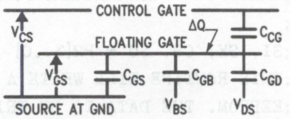
FIGURE 1. Cross Section of MOS Floating Gate EEPROM

EEPROM technology relies upon stored charge on the floating gate to retain information. Floating and control gate voltages are referenced to the source which is grounded. A mode of the equivalent capacitances and voltages for an EEPROM is shown in *Figure 2.* V_{GS} is the voltage on the floating gate, and delta Q is the charge stored on the floating gate. The charge remains on the floating gate even when power is not applied because the surrounding silicon dioxide serves as an excellent insulating material. Electrons are transferred to and from the floating gate and the underlying MOS device through a process known as Fowler-Nordheim tunneling.



TL/X/0006–2

$$V_{GS} = \frac{V_{CS}\,C_{CG} + V_{DS}\,C_{GD} + V_{BS}\,C_{GB} + \Delta Q}{C_{GS} + C_{GB} + C_{GD} + C_{CG}}$$

FIGURE 2. Equivalent Capacitances and Voltages

Tunneling Physics

The non-volatile memory storage in EEPROMs takes advantage of a quantum mechanical phenomenon known as Fowler-Nordheim tunneling. This tunneling process is a function of the energy levels of the materials involved. A schematic of the energy configuration for an EEPROM is illustrated in *Figure 3.* The energy difference between the valence and conduction bands in silicon dioxide (SiO_2) is about 9.05 eV. The energy difference between the same two bands for silicon (Si) is approximately 1.1 eV. When the SiO_2 and the Si are joined together the conduction band of the SiO_2 is 3.25 eV above the conduction band of the Si, while the valence band of the SiO_2 lies about 4.7 eV below the valence band of the Si. Since the thermal energy of an electron at room temperature (23°C) is only 0.025 eV the likelihood of an electron jumping from the valence band of the SiO_2 to the conduction band of the SiO_2 is very slight.

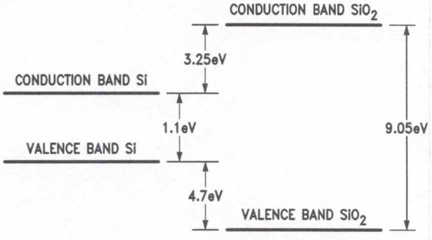


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FIGURE 3. Energy Band Diagram of the Si and SiO_2 System in its Neutral State

Fowler-Nordheim tunneling predicts that these energy bands can be distorted in the presence of an electric field. This process is depicted in *Figure 4*. In EEPROMs, tunneling of electrons occurs between the drain and floating gate through the SiO_2 tunneling region. The direction of Fowler-Nordheim tunneling of electrons through the tunneling region depends on the polarity of the voltages between the control gate and the drain. Tunneling physics predicts that when the electric fields across a thin insulator, such as SiO_2, are high enough, electrons from the negative electrode can acquire enough energy to pass or tunnel through the forbidden gap and enter the conduction band. The resulting current flux (J) is approximately proportional to an exponential function of the applied voltage (V) as illustrated in *Figure 5*. In order to obtain fields strengths large enough to initiate tunneling ($V > 7 \times 10^6$ eV/cm), at reasonable voltages (20V), the SiO_2 layer must be limited to a thickness less than 120 Angstroms.

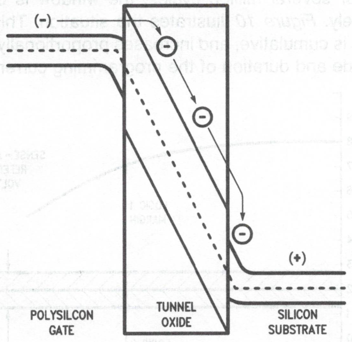
(-)
(+)
POLYSILICON GATE
TUNNEL OXIDE
SILICON SUBSTRATE

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FIGURE 4. Distortion of Energy Bands in the Presence of a Strong Electric Field

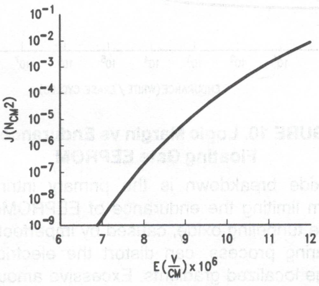

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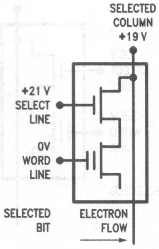
FIGURE 5. Fowler-Nordheim Tunneling I-V Characteristic

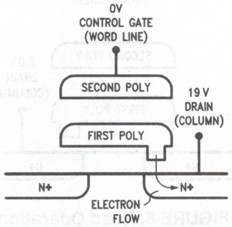
Device Operation

To write the cell to logic "0" the control gate is set to ground potential, and a high voltage (19V) is applied to the drain, while the source is left floating. The write operation is shown in *Figure 6*. This causes electrons on the floating gate to tunnel through the SiO_2 into the drain. In this configuration the transistor will allow current to flow. The electric field strength is highest in the region between the floating gate and the drain. Hence tunneling occurs in this thin SiO_2 region. The electric field intensity across the tunneling SiO_2 region is determined by the capacitive coupling ratio of the cell.


SELECTED COLUMN +19 V
+21 V SELECT LINE
0V WORD LINE
SELECTED BIT
ELECTRON FLOW

TL/X/0006-6

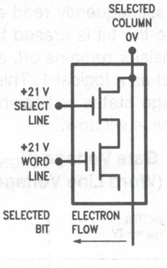
E^2PROM Transistor Write


0V CONTROL GATE (WORD LINE)
SECOND POLY
19 V DRAIN (COLUMN)
FIRST POLY
N+
N+
ELECTRON FLOW

TL/X/0006-7

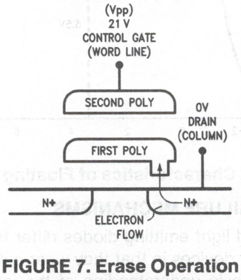
FIGURE 6. Write Operation

During the erase operation the drain is set to ground potential while the control gate is pulled up to 21V, as shown in *Figure 7*. This charging of the control gate causes the floating gate to become capacitively coupled with a positive bias and electrons then tunnel from the drain into the floating gate. The transfer of electrons shifts the cell threshold positive forcing the transistor to pinch-off current flow, which is then interpreted as a logic "1" state at its output.


SELECTED COLUMN 0V
+21 V SELECT LINE
+21 V WORD LINE
SELECTED BIT
ELECTRON FLOW

TL/X/0006-8

E^2PROM Transistor


(Vpp) 21 V CONTROL GATE (WORD LINE)
SECOND POLY
0V DRAIN (COLUMN)
FIRST POLY
N+
N+
ELECTRON FLOW

TL/X/0006-9

FIGURE 7. Erase Operation

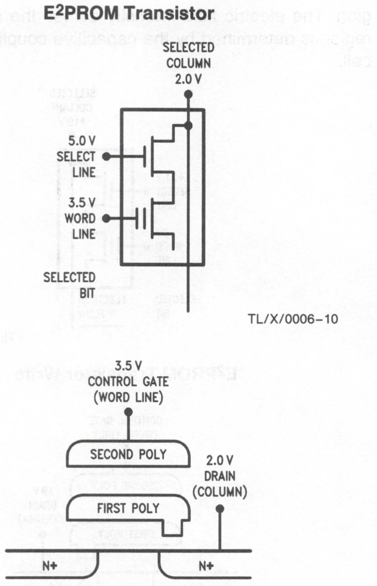


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FIGURE 8. Read Operation

The read operation is illustrated in *Figure 8*. To read the bit, 3.5V is applied to the gate of the transistor (word line). The charge stored on the floating gate influences the transistor characteristics. When the floating gate has a net negative charge, the transistor will not conduct current, and while positively charged it will pass current. Distinguishing between current flow and non-current flow allows logical states to be represented by the transistor. *Figure 9* illustrates the situation. When written to, the threshold voltage of the transistor (V_{th}) is equal to $-2V$ and the transistor is turned on. This is subsequently read as a logical 0 on the memory pins. While the bit is erased the threshold voltage will be 6V, the transistor remains off, and the logic is interpreted at the output as a logical 1. This difference between high and low voltage states is known as the cell margin, logic margin, or device window.

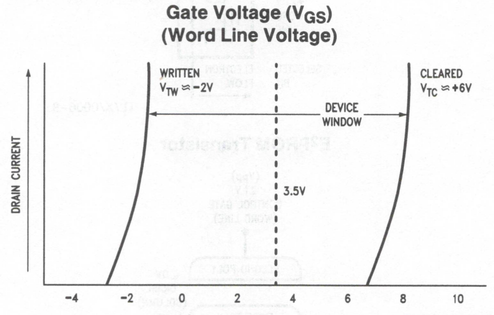

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FIGURE 9. I-V Characteristics of Floating Gate EEPROM

INTRINSIC FAILURE MECHANISMS

EEPROMs and light emitting diodes differ from many other semiconductor devices in that they wear out with use. However, with a basic understanding of the intrinsic wear out and failure mechanisms associated with EEPROMs, the designer can construct systems which successfully account for these limitations. The three primary failure mechanisms which affect all EEPROMs are charge trapping and tunnel oxide breakdown which are endurance related, and charge leakage which is data retention related.

Endurance

An EEPROM's endurance—that is, the number of write and erase operations through which each bit can be cycled reliably—is based largely on the degradation of cell margin. The amount of charge that can be stored and removed from an EEPROM cell decreases as the cumulative number of programming cycles rises.

Charge trapping is an intrinsic failure mechanism associated with EEPROMs which tends to narrow the difference between negatively and positively charged threshold voltages (device window) as a function of erase/write cycles. Eventually, after several million cycles, the window is collapsed completely. *Figure 10* illustrates the situation. This charge trapping is cumulative, and increases proportionally with the magnitude and duration of the programming current.

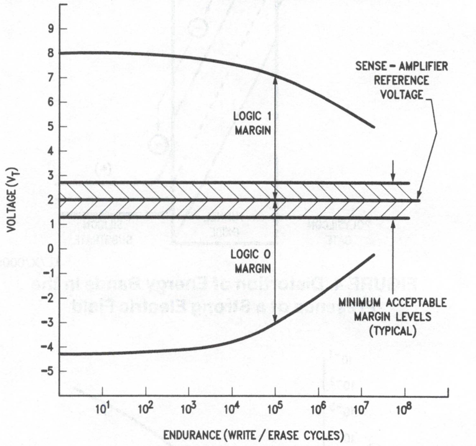

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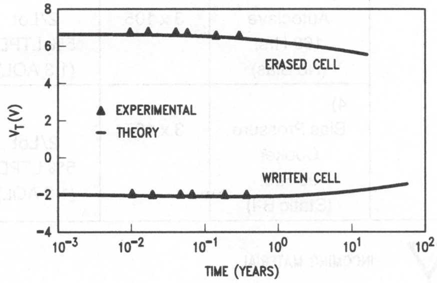
FIGURE 10. Logic Margin vs Endurance for Floating Gate EEPROM

Tunnel oxide breakdown is the primary intrinsic failure mechanism limiting the endurance of EEPROMs. Tiny defects in the tunneling oxide, caused by imperfections in the manufacturing process, can distort the electric field and cause large localized gradients. Excessive amounts of current flow through the regions where the electric field is tightly concentrated leading to high localized mechanical stresses. As write cycles continue, the probability that some imperfection in the oxide will break down increases. Given enough time, the cell will fail to operate correctly because the silicon dioxide which insulates the floating memory cell from the underlying voltage drain will become shorted. The rate of failures due to tunnel oxide breakdown can be reduced by minimizing particulate contaminants, decreasing the cross sectional area as much as is photo-lithographically possible, and controlling the ramp rate of the programming voltage so as to decrease the peak electric field which is created across the tunneling oxide.

Data Retention

Data retention in an EEPROM specification refers to the device's ability to retain a charge on its floating gate with or without an applied bias to the control gate, over extended periods of time. A floating gate on an EEPROM cell requires between one to five million electrons as stored charge. In order to store this amount of charge a current of approximately 10^{-10}A is required for a period of 10 ms. To insure that a wide enough logic margin exists on the cell, the designed floating gate leakage is limited to 10% of the initial charge (1.0^{-10}A) over a period of 10 years. This means that for continuous reading or storage operations over this period, the leakage must be kept below 10^{-21}A per cycle. *Figure 11* shows a typical plot of logic margin vs. time for EEPROMs.



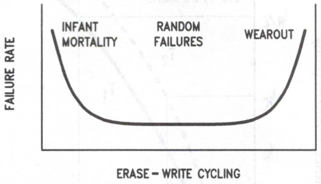
TL/X/0006–14

FIGURE 11. Logic Margin vs Data Retention of MOS Floating Gate EEPROM

Fowler-Nordheim tunneling, the process responsible for charging the floating cell, is also the means by which charge is leaked from the storage cell. This failure mechanism falls into a very broad class of failures which are proportional to $\exp(-E_a/kT)$ where E_a is the activation energy of the process, k is Boltzmann's constant, and T is the absolute temperature. This is very useful because if the activation energy is known for a given process, then tests can be conducted at elevated temperatures, reducing testing time, and the data can be extrapolated to lower operating temperatures using the relationship above.

Combined Effects

The total failure rate of an EEPROM is the sum of the combined rates from all the failure mechanisms involved. *Figure 12* shows the observed failure rate vs. erase/write cycling for EEPROMs. The distribution is a bathtub-shaped curve. The infant mortality region is characterized by an initially high, but rapidly decreasing failure rate. This period is dominated by failures which arise from manufacturing defects. Burn in reliability measures taken during National Semiconductor's manufacturing process are designed to eliminate these devices before they can be shipped to customers. The middle region is dominated by random failures and the rate is approximately level until the wearout region is reached. The wearout region is characterized by an increasing failure rate as the device reaches the end of its useful life.



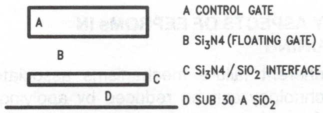
TL/X/0006–15

FIGURE 12. Typical Failure Curve for MOS Floating Gate EEPROM

Comparison to Other Technologies

CMOS static RAM devices with battery backup are often used for non-volatile memory storage. While the CMOS device does not exhibit the wearout mechanisms associated with EEPROM technology, the batteries associated with them do. Nickel Cadmium batteries have a wearout mechanism. Typically, they are good for only a couple of years before they must be replaced. Lithium batteries wear out with use and they display another liability in the fact that when shorted they can become very hot. Cost is another consideration when comparing battery backed up memory vs. EEPROM technology for small sized memory applications. Batteries and their associated mounting hardware can be quite expensive.

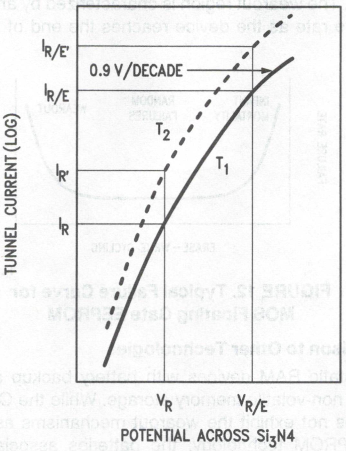
MNOS


A
B
C
D
A CONTROL GATE
B Si_3N4 (FLOATING GATE)
C Si_3N4 / SiO_2 INTERFACE STATES
D SUB 30 Å SiO_2

TL/X/0006–16

FIGURE 13. Cross Section of Nitride EEPROM

Some semiconductor manufacturers use nitrides in the production of their EEPROMs, resulting in two similar classes of memories known as SNOS and MNOS devices. A cross section of one of these nitride EEPROMs is illustrated in *Figure 13*. Its operation is similar to an MOS EEPROM. The nitride layer is analogous to the floating gate on the MOS devices. One of the problems encountered with the nitride technology is its temperature dependence on the current/voltage curve. This effect is shown in *Figure 14*. As the temperature increases the curve shifts up and to the left. The higher temperature causes a large increase in current for the same read voltage. This leads to poor data retention because Fowler-Nordheim tunneling is enhanced at these higher current levels and thus large amounts of charge can leak with each read cycle. Transistor voltages on nitride structures are also adversely affected by even small voltage stresses. The final problem associated with this technology is that the oxide-nitride interface is degraded by silicon-gate processing.



TL/X/0006-17

FIGURE 14. Current Increase from Increased Temperature Leading to Loss of Data Retention for Nitride EEPROM

On the other hand, MOS EEPROMs which use a polysilicon floating gate structure, tend to have better endurance characteristics and superior data retention under voltage and/or temperature stress. Polysilicon floating gate devices also have a longer history in processing, which accounts for their reproducibility and slow wear out as compared to nitride systems.

RELIABILITY ASPECTS OF EEPROMs IN MANUFACTURING

All of the inherent failure mechanisms associated with EEPROM technology can be reduced by applying quality control techniques during the manufacturing process. Quality control measures the component's conformance to specification. Careful monitoring of both the process and the individual devices assures the customer of the highest possible reliability.

Quality Control

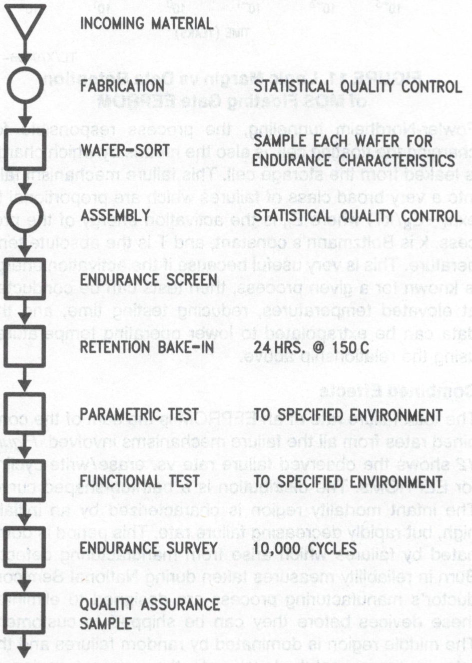
The introduction of any new part into the National Semiconductor product line requires first that the product must pass strict design and manufacturing requirements. A table of the reliability qualification procedure which National Semiconductor follows for the introduction of a new EEPROM product appears in Table I.

TABLE I. Reliability Qualification Procedure for All National Semiconductor EEPROM Products

	Test	Sample	Allowed Fail.
J Pkg.	Operating Life 125°C 1000 Hrs.	3 x 105	2/Lot 5% LTPD (0.78 AQL)
	Dynamic B-I at 5.5. All inputs exercised. (Read, Disable, Read, Disable . . .)		

TABLE I. Reliability Qualification Procedure for All National Semiconductor EEPROM Products (Continued)

	Test	Sample	Allowed Fail.
N Pkg.	1) Operating Life 125°C 1008 Hrs.	3 x 105	2/Lot 5% LTPD (1.3 AQL)
	2) 85/85 1008 Hrs.	3 x 105	2/Lot 5% LTPD (1. 3 AQL)
	3) Autoclave 168 Hrs. (No Bias)	3 x 105	2/Lot 5% LTPD (1.3 AQL)
	4) Bias Pressure Cooker 96 Hrs. (Static B-I)	3 x 105	2/Lot 5% LTPD (1.3 AQL)


INCOMING MATERIAL
FABRICATION
STATISTICAL QUALITY CONTROL
WAFER-SORT
SAMPLE EACH WAFER FOR ENDURANCE CHARACTERISTICS
ASSEMBLY
STATISTICAL QUALITY CONTROL
ENDURANCE SCREEN
RETENTION BAKE-IN
24 HRS. @ 150 C
PARAMETRIC TEST
TO SPECIFIED ENVIRONMENT
FUNCTIONAL TEST
TO SPECIFIED ENVIRONMENT
ENDURANCE SURVEY
10,000 CYCLES
QUALITY ASSURANCE SAMPLE

TL/X/0006-18

FIGURE 15. Quality Control Steps for National Semiconductor EEPROMs

For EEPROMs which are in the manufacturing phase, statistical quality control and testing are used to evaluate product compliance to specification. *Figure 15* shows a flow chart of the various quality control steps which National Semiconductor puts their EEPROM chips through.

Burn In

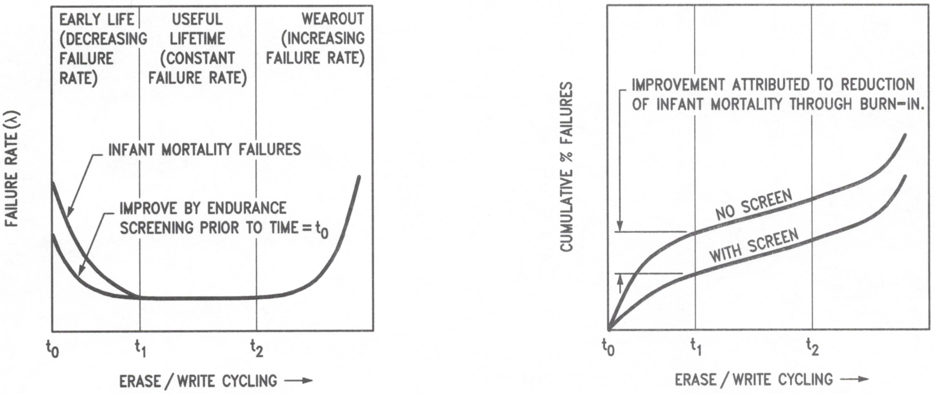
In addition to strict qualifying requirements of products prior to manufacture and tight quality control procedures, National Semiconductor also implements burn-in tests, which weed out the weaker chips, and ensure an even higher level of reliability for the surviving EEPROMs. *Figure 16* is an illustration of typical improvements in product reliability resulting from burning in chips, and removing the ones which would normally fail in the infant mortality region.

RELIABILITY ASPECTS OF EEPROMs IN APPLICATIONS

Reliability Testing and Results

Endurance failure in EEPROM testing is often defined in very different ways. One of the more lenient methods of describing failures on an EEPROM is to simply say that every non-operative cell in a memory device constitutes one failure. National Semiconductor, however, chooses to use a fundamentally more rigorous definition, in which a failure is indicated the first time any single memory bit on the entire chip fails. Depending on memory size and specific devices, one can typically expect a failure rate over 10,000 erase/write cycles of about 3% or less. Of this small percentage of chips which fail after ten-thousand cycles, seldom will any have more than a single-bit error.

It is important to note that the two modes of EEPROM failure, endurance and data retention, are fundamentally orthogonal in applications. That is, a cell that is to be written 10,000 times does not require data retention of 10 years between writes, unless of course you require that the product operate for 100,000 years. Further, even adjacent cells in an EEPROM memory device operate independently from each other, so that any given memory location that is updated only upon rare occasions can be expected to retain its information for long periods, even though adjacent cells are being worn out through extended cycling.



TL/X/0006-19

TL/X/0006-20

FIGURE 16. Improvements Attributed to National Semiconductor's Endurance Screen

Section 3
PROMs

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Bipolar PROM Selection Guide

Non-Registered PROMs

Size (Bits)	Organization	Pins (DIP)	Part Number	t_{AA} (Max) in ns	t_{EA} (Max) in ns	I_{CC} (Max) in mA	Temperature Celsius
256	32 x 8 OC	16	DM54S188	45	30	110	−55°C to +125°C
	32 x 8 OC	16	DM74S188	35	20	110	0°C to +70°C
	32 x 8 TS	16	DM54S288	45	30	110	−55°C to +125°C
	32 x 8 TS	16	DM74S288	35	20	110	0°C to +70°C
	32 x 8 OC	16	DM54S188A	35	30	110	−55°C to +125°C
	32 x 8 OC	16	DM74S188A	25	20	110	0°C to +70°C
	32 x 8 TS	16	DM54S288A	35	30	110	−55°C to +125°C
	32 x 8 TS	16	DM74S288A	25	20	110	0°C to +70°C
	32 x 8 TS	16	PL87X288B	15	12	140	0°C to +70°C
1024	256 x 4 OC	16	DM54S387	60	30	130	−55°C to +125°C
	256 x 4 OC	16	DM74S387	50	25	130	0°C to +70°C
	256 x 4 TS	16	DM54S287	60	30	130	−55°C to +125°C
	256 x 4 TS	16	DM74S287	50	25	130	0°C to +70°C
	256 x 4 OC	16	DM54S387A	40	30	130	−55°C to +125°C
	256 x 4 OC	16	DM74S387A	30	20	130	0°C to +70°C
	256 x 4 TS	16	DM54S287A	40	30	130	−55°C to +125°C
	256 x 4 TS	16	DM74S287A	30	20	130	0°C to +70°C
2048	512 x 4 OC	16	DM54S570	65	35	130	−55°C to +125°C
	512 x 4 OC	16	DM74S570	55	30	130	0°C to +70°C
	512 x 4 TS	16	DM54S571	65	35	130	−55°C to +125°C
	512 x 4 TS	16	DM74S571	55	30	130	0°C to +70°C
	512 x 4 OC	16	DM54S570A	60	35	130	−55°C to +125°C
	512 x 4 OC	16	DM74S570A	45	25	130	0°C to +70°C
	512 x 4 TS	16	DM54S571A	60	35	130	−55°C to +125°C
	512 x 4 TS	16	DM74S571A	45	25	130	0°C to +70°C
	512 x 4 TS	16	DM54S571B	50	35	130	−55°C to +125°C
	512 x 4 TS	16	DM74S571B	35	25	130	0°C to +70°C
	256 x 8 TS	20	DM54LS471	70	35	100	−55°C to +125°C
	256 x 8 TS	20	DM74LS471	60	30	100	0°C to +70°C
4096	512 x 8 OC	20	DM54S473	75	35	155	−55°C to +125°C
	512 x 8 OC	20	DM74S473	60	30	155	0°C to +70°C
	512 x 8 TS	20	DM54S472	75	35	155	−55°C to +125°C
	512 x 8 TS	20	DM74S472	60	30	155	0°C to +70°C
	512 x 8 OC	20	DM54S473A	60	35	155	−55°C to +125°C
	512 x 8 OC	20	DM74S473A	45	30	155	0°C to +70°C
	512 x 8 TS	20	DM54S472A	60	35	155	−55°C to +125°C
	512 x 8 TS	20	DM74S472A	45	30	155	0°C to +70°C
	512 x 8 TS	20	DM54S472B	50	35	155	−55°C to +125°C
	512 x 8 TS	20	DM74S472B	35	25	155	0°C to +70°C
	512 x 8 OC	24	DM54S475	75	40	170	−55°C to +125°C
	512 x 8 OC	24	DM74S475	65	35	170	0°C to +70°C
	512 x 8 TS	24	DM54S474	75	40	170	−55°C to +125°C
	512 x 8 TS	24	DM74S474	65	35	170	0°C to +70°C
	512 x 8 OC	24	DM54S475A	60	35	170	−55°C to +125°C
	512 x 8 OC	24	DM74S475A	45	25	170	0°C to +70°C
	512 x 8 TS	24	DM54S474A	60	35	170	−55°C to +125°C
	512 x 8 TS	24	DM74S474A	45	25	170	0°C to +70°C
	512 x 8 TS	24	DM54S474B	50	35	170	−55°C to +125°C
	512 x 8 TS	24	DM74S474B	35	25	170	0°C to +70°C
	1024 x 4 OC	18	DM54S572	75	45	140	−55°C to +125°C
	1024 x 4 OC	18	DM74S572	60	35	140	0°C to +70°C
	1024 x 4 TS	18	DM54S573	75	45	140	−55°C to +125°C
	1024 x 4 TS	18	DM74S573	60	35	140	0°C to +70°C
	1024 x 4 OC	18	DM54S572A	60	35	140	−55°C to +125°C
	1024 x 4 OC	18	DM74S572A	45	25	140	0°C to +70°C
	1024 x 4 TS	18	DM54S573A	60	35	140	−55°C to +125°C
	1024 x 4 TS	18	DM74S573A	45	25	140	0°C to +70°C
	1024 x 4 TS	18	DM54S573B	50	35	140	−55°C to +125°C
	1024 x 4 TS	18	DM74S573B	35	25	140	0°C to +70°C

Non-Registered PROMs (Continued)

Size (Bits)	Organization	Pins (DIP)	Part Number	t_{AA} (Max) in ns	t_{EA} (Max) in ns	I_{CC} (Max) in mA	Temperature Celsius
8192	1024 x 8 OC	24	DM77S180	75	35	170	−55°C to +125°C
	1024 x 8 OC	24*	DM77S280	75	35	170	−55°C to +125°C
	1024 x 8 OC	24	DM87S180	55	30	170	0°C to +70°C
	1024 x 8 OC	24*	DM87S280	55	30	170	0°C to +70°C
	1024 x 8 TS	24	DM77S181	75	35	170	−55°C to +125°C
	1024 x 8 TS	24*	DM77S281	75	35	170	−55°C to +70°C
	1024 x 8 TS	24	DM87S181	55	30	170	0°C to +70°C
	1024 x 8 TS	24*	DM87S281	55	30	170	0°C to +70°C
	1024 x 8 TS	24	DM77S181A	65	35	170	−55°C to +125°C
	1024 x 8 TS	24	DM87S181A	45	30	170	0°C to +70°C
	2048 x 4 OC	18	DM77S184	70	30	140	−55°C to +125°C
	2048 x 4 OC	18	DM87S184	55	25	140	0°C to +70°C
	2048 x 4 TS	18	DM77S185	70	30	140	−55°C to +125°C
	2048 x 4 TS	18	DM87S185	55	25	140	0°C to +70°C
	2048 x 4 TS	18	DM77S185A	60	30	140	−55°C to +125°C
	2048 x 4 TS	18	DM87S185A	45	25	140	0°C to +70°C
	2048 x 4 TS	18	DM77S185B	50	30	140	−55°C to +125°C
	2048 x 4 TS	18	DM87S185B	35	25	140	0°C to +70°C

*24-Pin Narrow Dual-In-Line Package

Registered PROMs

Size (Bits)	Organization	Pins (DIP)	Part Number	t_{SA} (Min) in ns	t_{PLH} (CLK) t_{PHL} (CLK) (Max) in ns	I_{CC} (Max) in mA	Temperature Celsius
4096	512 x 8 REG	24*	DM77SR474	55	30	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR474B	40	25	185	−55°C to +125°C
	512 x 8 REG	24*	DM87SR474	50	27	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR474B	35	20	185	0°C to +70°C
	512 x 8 REG	24*	DM77SR476	55	30	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR476B	40	25	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR27	55	30	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR27B	40	25	185	−55°C to +125°C
	512 x 8 REG	24*	DM87SR476	50	27	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR476B	35	20	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR27	50	27	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR27B	35	20	185	0°C to +70°C
8192	1024 x 8 REG	24*	DM77SR181	50	30	175	−55°C to +125°C
	1024 x 8 REG	24*	DM87SR181	40	20	175	0°C to +70°C

*24-Pin Narrow Dual-In-Line Package

National Semiconductor

PL87X288B
(32 x 8) 256-Bit TTL Logic PROMs

General Description

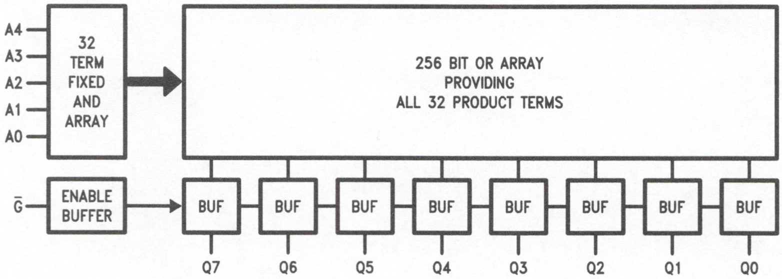
These Schottky programmable logic devices are organized in the popular 32 words by 8-bit configuration. An enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the OFF or high impedance state. The memories are available in the TRI-STATE® version only.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—15 ns max
  - Enable access—12 ns max
  - Enable recovery—12 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- >2000V input protection for electrostatic discharge
- TRI-STATE outputs

Block Diagram


A4
A3
A2
A1
A0
32 TERM FIXED AND ARRAY
256 BIT OR ARRAY PROVIDING ALL 32 PRODUCT TERMS
$\overline{G}$
ENABLE BUFFER
BUF
BUF
BUF
BUF
BUF
BUF
BUF
BUF
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

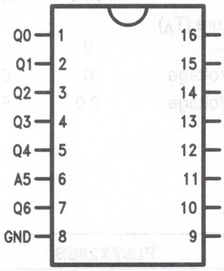
TL/D/6747–1

Pin Names

A0–A4	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

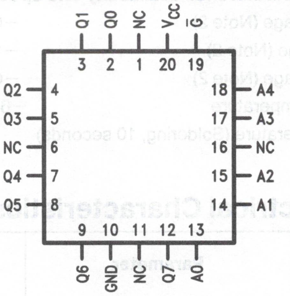

Q0 1
Q1 2
Q2 3
Q3 4
Q4 5
A5 6
Q6 7
GND 8
16 V_{CC}
15 $\overline{G}$
14 A4
13 A3
12 A2
11 A1
10 A0
9 Q7

TL/D/6747-2

Top View

Order Number PL87X288BJ or PL87X288BN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)


Q1
Q0
NC
V_{CC}
$\overline{G}$
3 2 1 20 19
Q2 4
Q3 5
NC 6
Q4 7
Q5 8
18 A4
17 A3
16 NC
15 A2
14 A1
9 10 11 12 13
Q6
GND
NC
Q7
A0

TL/D/6747-9

Top View

Order Number PL87X288BV
See NS Package Number V20A

Ordering Information

Commercial Temperature Range
0°C to +70°C

Parameter/Order Number	Max Access Time (ns)
PL87X288BN	15
PL87X288BJ	15
PL87X288BV	15

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2 to +5.5V
Output Voltage (Note 2)	−0.5 to +5.5V
Storage Temperature	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	>2000V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
PL87X288B	4.75	5.25	V
Ambient Temperature (T_A)			
PL87X288B	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	PL87X288B			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.4V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 24 mA		0.35	0.50	V
V_{IL}	Low Level Input Voltage	(Note 7)			0.80	V
V_{IH}	High Level Input Voltage	(Note 7)	2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.5	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		110	140	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	−30		−130	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.4V to 2.4V Chip Disabled			100 −100	μA
V_{OH}	Output Voltage High	I_{OH} = −3.2 mA	2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: C_L = 50 pF.

Note 6: C_L = 5 pF.

Note 7: These are absolute voltages with respect to the ground pin on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC Electrical Characteristics with standard load and operating conditions

Symbol	Parameter	JEDEC Symbol	PL87X288B			Units
			Min	Typ	Max	
t_{AA}	Address Access Time (Note 5)	TAVQV		10	15	ns
t_{EA}	Enable Access Time (Note 5)	TEVQV		8	12	ns
t_{ER}	Enable Recovery Time (Note 6)	TEXQX		8	12	ns
t_{ZX}	Output Enable Time (Note 5)	TEVQX		8	12	ns
t_{XZ}	Output Disable Time (Note 6)	TEXQZ		8	12	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metalization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S188
(32 x 8) 256-Bit TTL PROM

General Description

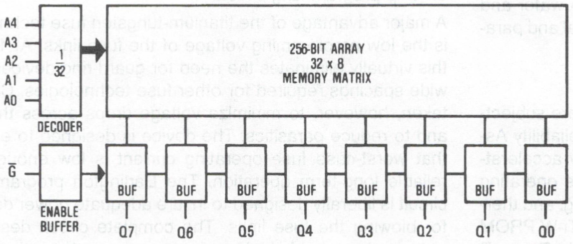
This Schottky memory is organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access down to—25 ns max
  Enable access—20 ns max
  Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



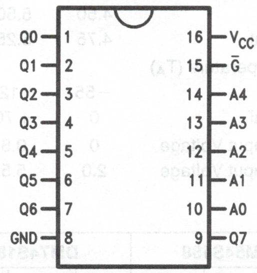
TL/D/9187-1

Pin Names

A0–A4	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package


Q0 1
Q1 2
Q2 3
Q3 4
Q4 5
Q5 6
Q6 7
GND 8
16 V_{CC}
15 $\overline{G}$
14 A4
13 A3
12 A2
11 A1
10 A0
9 Q7

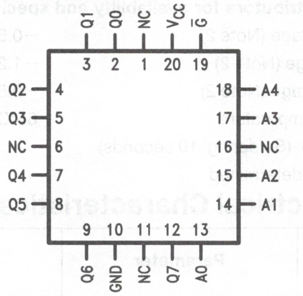
TL/D/9187-2

Top View

Order Number DM54/74S188J, 188AJ, DM74S188N or 188AN

See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)


Q1
Q0
NC
V_{CC}
$\overline{G}$
3 2 1 20 19
Q2 4
Q3 5
NC 6
Q4 7
Q5 8
18 A4
17 A3
16 NC
15 A2
14 A1
9 10 11 12 13
Q6
GND
NC
Q7
A0

TL/D/9187-3

Top View

Order Number DM74S188V or 188AV

See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S188N	35
DM74S188J	35
DM74S188V	35
DM74S188AN	25
DM74S188AJ	25
DM74S188AV	25

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S188J	45
DM54S188AJ	35

Absolute Maximun Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD to be determined

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM54S188			DM74S188			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80			0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		70	110		70	110	mA

Note 1: Absolute Maximum Ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S188			DM74S188A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		22	35		17	25	ns
TEA	TEVQV	Enable Access Time		15	20		15	20	ns
TER	TEXQX	Enable Recovery Time		15	25		15	20	ns
TZX	TEVQX	Output Enable Time		15	20		15	20	ns
TXZ	TEXQZ	Output Disable Time		15	25		15	20	ns

AC Electrical Characteristics with Standard Load and Operating Conditions (Continued)

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S188			DM54S188A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		22	45		17	35	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	35		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S288 (32 x 8) 256-Bit TTL PROM

General Description

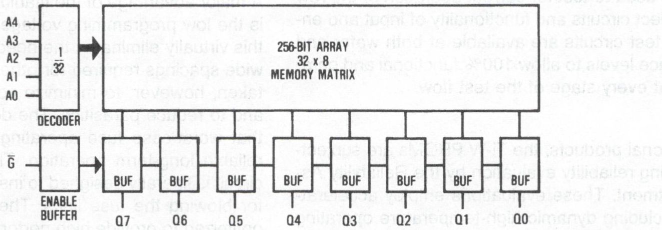
This Schottky memory is organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—25 ns max
  - Enable access—20 ns max
  - Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® Outputs

Block Diagram



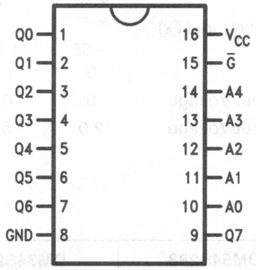
TL/D/8360–1

Pin Names

A0–A4	Addresses
$\overline{G}$	Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

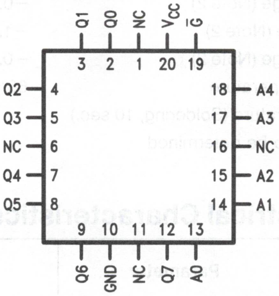

Q0 1
Q1 2
Q2 3
Q3 4
Q4 5
Q5 6
Q6 7
GND 8
16 V_{CC}
15 $\overline{G}$
14 A4
13 A3
12 A2
11 A1
10 A0
9 Q7

TL/D/8360-2

Top View

Order Number DM54/74S288J, 288AJ or DM74S288N, 288AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)


Q1 3
Q0 2
NC 1
V_{CC} 20
$\overline{G}$ 19
Q2 4
Q3 5
NC 6
Q4 7
Q5 8
18 A4
17 A3
16 NC
15 A2
14 A1
Q6 9
GND 10
NC 11
Q7 12
A0 13

TL/D/8360-7

Top View

Order Number DM74S288V or 288AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S288N	35
DM74S288J	35
DM74S288V	35
DM74S288AN	25
DM74S288AJ	25
DM74S288AV	25

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S288J	45
DM54S288AJ	35

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD rating to be determined	

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM54S288			DM74S288			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	µA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	µA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80			0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		70	110		70	110	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 5)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	µA
					−50			−50	µA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 5: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMPERATURE RANGE (0°C to +70°C)

Symbol	Parameter	JEDEC Symbol	DM74S288			DM74S288A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		22	35		17	25	ns
TEA	Enable Access Time	TEVQV		15	20		15	20	ns
TER	Enable Recovery Time	TEXQX		15	25		15	20	ns
TZX	Output Enable Time	TEVQX		15	25		15	20	ns
TXZ	Output Disable Time	TEXQZ		15	25		15	20	ns

MILITARY TEMPERATURE RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S288			DM54S288A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		22	45		17	35	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	35		15	30	ns
TZX	TEVQZ	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metalization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S287 (256 x 4) 1024-Bit TTL PROM

General Description

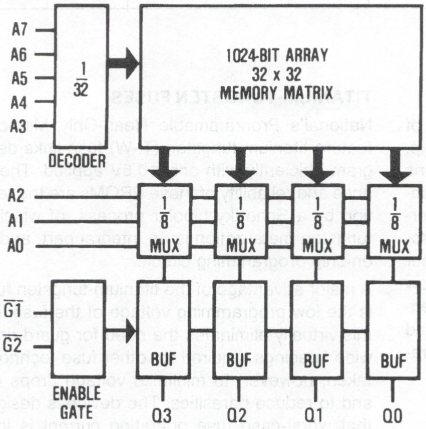
This Schottky memory is organized in the popular 256 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 30 ns max
  - Enable access—20 ns max
  - Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- >2000V input protection for electrostatic discharge
- TRI-STATE® outputs

Block Diagram


A7
A6
A5
A4
A3
1/32
DECODER
1024-BIT ARRAY
32 x 32
MEMORY MATRIX
A2
A1
A0
1/8 MUX
1/8 MUX
1/8 MUX
1/8 MUX
$\overline{G1}$
$\overline{G2}$
ENABLE GATE
BUF
BUF
BUF
BUF
Q3
Q2
Q1
Q0

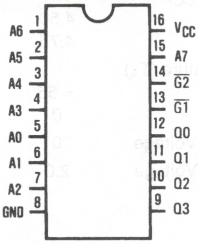
TL/D/8359-1

Pin Names

A0–A7	Addresses
$\overline{G1}$, $\overline{G2}$	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line-Package

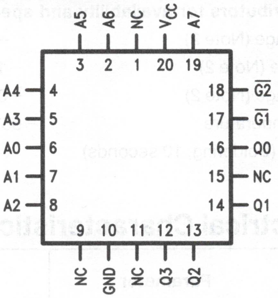

A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 G2
13 G1
12 Q0
11 Q1
10 Q2
9 Q3

TL/D/8359–2

Top View

Order Number DM54/74S287J, 287AJ, DM74S287N or 287AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)


A5 3
A6 2
NC 1
VCC 20
A7 19
A4 4
A3 5
A0 6
A1 7
A2 8
18 G2
17 G1
16 Q0
15 NC
14 Q1
NC 9
GND 10
NC 11
Q3 12
Q2 13

TL/D/8359–7

Top View

Order Number DM74S287V or 287AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S287AJ	30
DM74S287J	50
DM74S287AN	30
DM74S287N	50
DM74S287AV	30
DM74S287V	50

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S287AJ	40
DM54S287J	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD	>2000V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM54S287			DM74S287			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80			0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		80	130		80	130	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 5)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = +25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 5: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S287			DM74S287A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		35	50		20	30	ns
TEA	TEVQV	Enable Access Time		15	25		15	20	ns
TER	TEXQX	Enable Recovery Time		15	25		15	20	ns
TZX	TEVQX	Output Enable Time		15	25		15	20	ns
TXZ	TEXQZ	Output Disable Time		15	25		15	20	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S287			DM54S287A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		35	60		20	40	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S387
(256 x 4) 1024-Bit TTL PROM

General Description

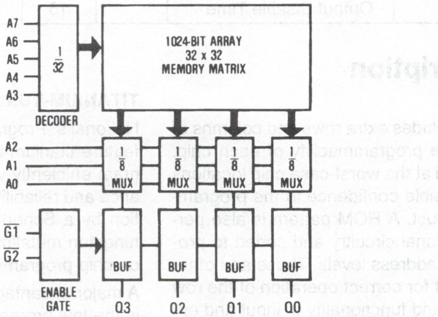
This Schottky memory is organized in the popular 256 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 30 ns max
  - Enable access—20 ns max
  - Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram


A7
A6
A5
A4
A3
1/32
DECODER
1024-BIT ARRAY
32 x 32
MEMORY MATRIX
A2
A1
A0
1/8 MUX
1/8 MUX
1/8 MUX
1/8 MUX
G1
G2
ENABLE GATE
BUF
BUF
BUF
BUF
Q3
Q2
Q1
Q0

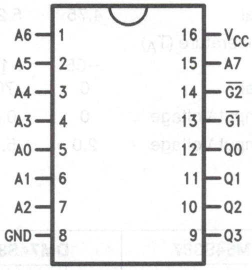
TL/D/9188–1

Pin Names

A0–A7	Addresses
$\overline{G1}$–$\overline{G2}$	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 V$_{CC}$
15 A7
14 $\overline{G2}$
13 $\overline{G1}$
12 Q0
11 Q1
10 Q2
9 Q3

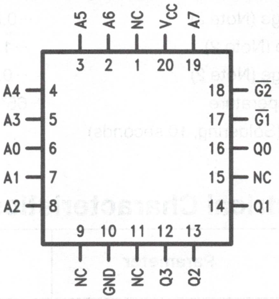
TL/D/9188-2

Top View

Order Number DM54/74S387J, 387AJ, DM74S387N, 387AN

See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)


A5
A6
NC
V$_{CC}$
A7
3 2 1 20 19
A4 4
A3 5
A0 6
A1 7
A2 8
18 $\overline{G2}$
17 $\overline{G1}$
16 Q0
15 NC
14 Q1
9 10 11 12 13
NC
GND
NC
Q3
Q2

TL/D/9188-3

Top View

Order Number DM74S387V, 387AV

See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S387AJ	30
DM74S387J	50
DM74S387AN	30
DM74S387N	50
DM74S387AV	30
DM74S387V	50

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S387AJ	40
DM54S387J	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to + 7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD	>2000V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM54S387			DM74S387			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80			0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		80	130		80	130	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = +25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	Parameter	JEDEC Symbol	DM74S387			DM74S387A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		35	50		20	30	ns
TEA	Enable Access Time	TEVQV		15	25		15	20	ns
TER	Enable Recovery Time	TEXQX		15	25		15	20	ns
TZX	Output Enable Time	TEVQX		15	25		15	20	ns
TXZ	Output Disable Time	TEXQZ		15	25		15	20	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	Parameter	JEDEC Symbol	DM54S387			DM54S387A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		35	60		20	40	ns
TEA	Enable Access Time	TEVQV		15	30		15	30	ns
TER	Enable Recovery Time	TEXQX		15	30		15	30	ns
TZX	Output Enable Time	TEVQX		15	30		15	30	ns
TXZ	Output Disable Time	TEXQZ		15	30		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74LS471
(256 x 8) 2048-Bit TTL PROM

General Description

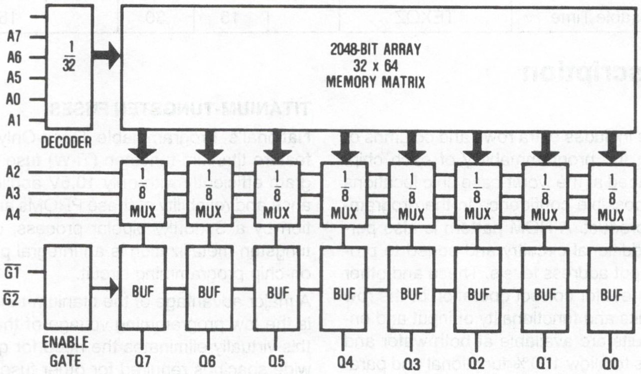
These Schottky memories are organized in the popular 256 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—60 ns max
  - Enable access—30 ns max
  - Enable recovery—30 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram


A7
A6
A5
A0
A1
1/32
DECODER
2048-BIT ARRAY
32 x 64
MEMORY MATRIX
A2
A3
A4
1/8 MUX
BUF
G1
G2
ENABLE GATE
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

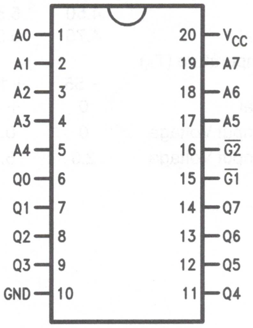
TL/D/9190-1

Pin Names

A0–A7	Addresses
G1–G2	Output Enables
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

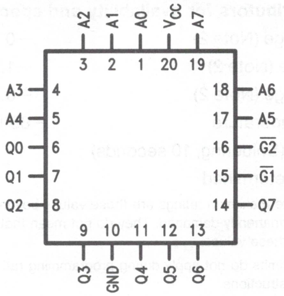

A0 1
A1 2
A2 3
A3 4
A4 5
Q0 6
Q1 7
Q2 8
Q3 9
GND 10
20 V_{CC}
19 A7
18 A6
17 A5
16 $\overline{G2}$
15 $\overline{G1}$
14 Q7
13 Q6
12 Q5
11 Q4

TL/D/9190-2

Top View

Order Number DM54/74LS471J or DM74LS471N
See NS Package Number J20A or N20A

Plastic Leaded Chip Carrier (PLCC)


A2 3
A1 2
A0 1
V_{CC} 20
A7 19
A3 4
A4 5
Q0 6
Q1 7
Q2 8
18 A6
17 A5
16 $\overline{G2}$
15 $\overline{G1}$
14 Q7
9 Q3
10 GND
11 Q4
12 Q5
13 Q6

TL/D/9190-3

Top View

Order Number DM74LS471V
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74LS471N	60
DM74LS471J	60
DM74LS471V	60

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54LS471J	70

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54LS471			DM74LS471			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		75	100		75	100	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0v and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

Symbol	JEDEC Symbol	Parameter	DM54LS471			DM74LS471			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		45	70		40	60	ns
TEA	TEVQV	Enable Access Time		15	35		15	30	ns
TER	TEXQX	Enable Recovery Time		15	35		15	30	ns
TZX	TEVQX	Output Enable Time		15	35		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S472
(512 x 8) 4096-Bit TTL PROM

General Description

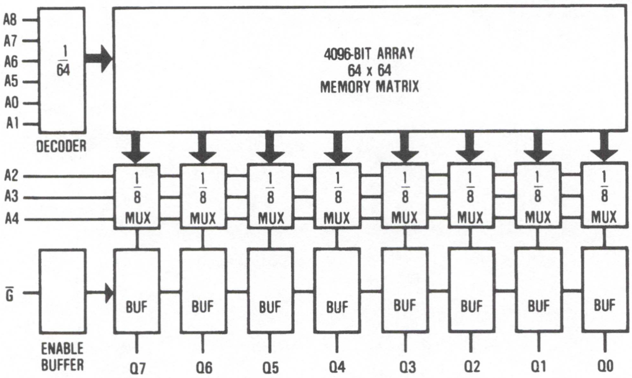
This Schottky memory is organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram


A8
A7
A6
A5
A0
A1
1/64
DECODER
4096-BIT ARRAY
64 x 64
MEMORY MATRIX
A2
A3
A4
1/8 MUX
G̅
ENABLE BUFFER
BUF
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

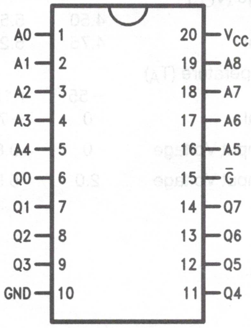
TL/D/9191–1

Pin Names

A0–A8	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

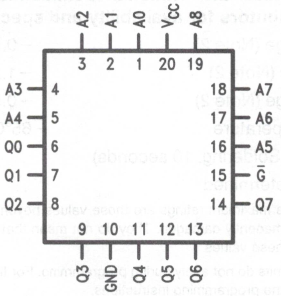

A0 1
A1 2
A2 3
A3 4
A4 5
Q0 6
Q1 7
Q2 8
Q3 9
GND 10
20 V_{CC}
19 A8
18 A7
17 A6
16 A5
15 $\overline{G}$
14 Q7
13 Q6
12 Q5
11 Q4

TL/D/9191-2

Top View

Order Number DM54/74S472J, 472AJ, 472BJ
DM74S472N, 472AN, 472BN
See NS Package Number J20A or N20A

Plastic Leaded Chip Carrier (PLCC)


A2
A1
A0
V_{CC}
A8
3 2 1 20 19
A3 4
A4 5
Q0 6
Q1 7
Q2 8
18 A7
17 A6
16 A5
15 $\overline{G}$
14 Q7
9 10 11 12 13
Q3
GND
Q4
Q5
Q6

TL/D/9191-3

Top View

Order Number DM74S472V, 472AV, 472BV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S472AN	45
DM74S472BN	35
DM74S472N	60
DM74S472AJ	45
DM74S472BJ	35
DM74S472J	60
DM74S472AV	45
DM74S472BV	35
DM74S472V	60

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S472AJ	60
DM54S472BJ	50
DM54S472J	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S472			DM74S472			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	µA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	µA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		110	155		110	155	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	µA
					−50			−50	µA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S472			DM74S472A			DM74S472B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	60		25	45		25	35	ns
TEA	TEVQV	Enable Access Time		15	30		15	30		15	25	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30		15	25	ns
TZX	TEVQX	Output Enable Time		15	30		15	30		15	25	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S472			DM54S472A			DM54S472B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		25	60		25	50	ns
TEA	TEVQV	Enable Access Time		15	35		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		15	35		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		15	35		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54S473/DM74S473 (512 x 8) 4096-Bit TTL PROM

General Description

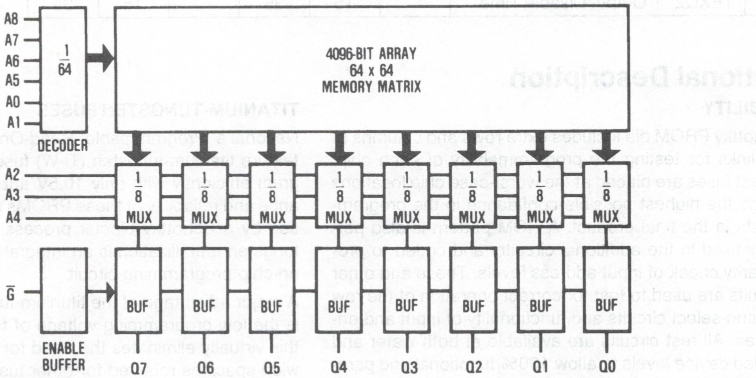
This Schottky memory is organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—45 ns max
  - Enable access—30 ns max
  - Enable recovery—30 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram


A8
A7
A6
A5
A0
A1
1/64
DECODER
4096-BIT ARRAY
64 x 64
MEMORY MATRIX
A2
A3
A4
1/8 MUX
G̅
BUF
ENABLE BUFFER
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

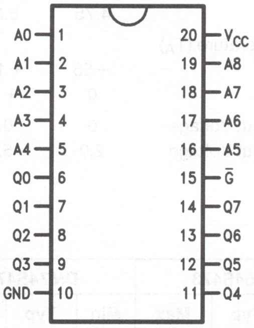
TL/D/9715-1

Pin Names

A0–A8	Addresses
G̅	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

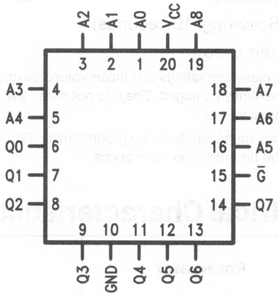

A0 1
A1 2
A2 3
A3 4
A4 5
Q0 6
Q1 7
Q2 8
Q3 9
GND 10
11 Q4
12 Q5
13 Q6
14 Q7
15 $\overline{G}$
16 A5
17 A6
18 A7
19 A8
20 V_{CC}

TL/D/9715–2

Top View

Order Number DM54/74S473J, 473AJ, DM74S473N or 473AN
See NS Package Number J20A or N20A

Plastic Leaded Chip Carrier (PLCC)


A2 3
A1 2
A0 1
V_{CC} 20
A8 19
A3 4
A4 5
Q0 6
Q1 7
Q2 8
18 A7
17 A6
16 A5
15 $\overline{G}$
14 Q7
9 Q3
10 GND
11 Q4
12 Q5
13 Q6

TL/D/9715–3

Top View

Order Number DM74S473V or 473AV
See NS Package Number V20A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S473AN	45
DM74S473N	60
DM74S473AJ	45
DM74S473J	60
DM74S473AV	45
DM74S473V	60

Military Temp. Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S473AJ	60
DM54S473J	75

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S473			DM74S473			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	µA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	µA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	µA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	µA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		110	155		110	155	mA

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP. RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S473			DM74S473A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	60		25	45	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30	ns

MILITARY TEMP. RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S473			DM54S473A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		25	60	ns
TEA	TEVQV	Enable Access Time		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanuim-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S474
(512 x 8) 4096-Bit TTL PROM

General Description

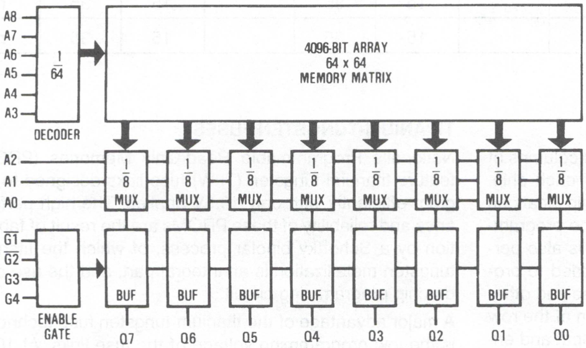
This Schottky memory is organized in the popular 512 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram


A8
A7
A6
A5
A4
A3
1
64
DECODER
4096-BIT ARRAY
64 x 64
MEMORY MATRIX
A2
A1
A0
1
8
MUX
G1
G2
G3
G4
ENABLE
GATE
BUF
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

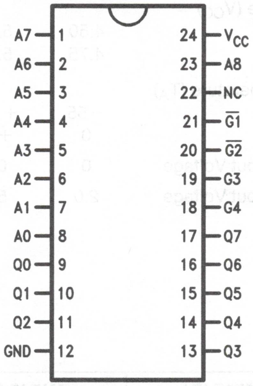
TL/D/9714-1

Pin Names

A0–A8	Addresses
$\overline{G1}$, $\overline{G2}$, G3, G4	Output Enables
GND	Ground
NC	No Connection
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

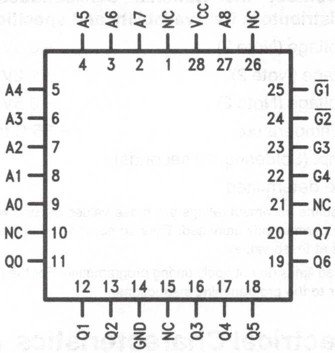

A7
A6
A5
A4
A3
A2
A1
A0
Q0
Q1
Q2
GND
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
V_{CC}
A8
NC
$\overline{G1}$
$\overline{G2}$
G3
G4
Q7
Q6
Q5
Q4
Q3

TL/D/9714-2

Top View

Order Number DM54/74S474J, 474AJ, 474BJ, DM74S474N, 474AN, 474BN
See NS Package Number J24A or N24A

Plastic Leaded Chip Carrier (PLCC)


A5
A6
A7
NC
V_{CC}
A8
NC
4
3
2
1
28
27
26
A4
A3
A2
A1
A0
NC
Q0
5
6
7
8
9
10
11
25
24
23
22
21
20
19
$\overline{G1}$
$\overline{G2}$
G3
G4
NC
Q7
Q6
12
13
14
15
16
17
18
Q1
Q2
GND
NC
Q3
Q4
Q5

TL/D/9714-3

Top View

Order Number DM74S474V, 474AV, 474BV
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S474AJ	45
DM74S474BJ	35
DM74S474J	65
DM74S474AN	45
DM74S474BN	35
DM74S474N	65
DM74S474AV	45
DM74S474BV	35
DM74S474V	65

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S474AJ	60
DM54S474BJ	50
DM54S474J	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S474			DM74S474			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		115	170		115	170	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S474			DM74S474A			DM74S474B			Units
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
TAA	TAVQV	Address Access Time		40	65		25	45		25	35	ns
TEA	TEVQV	Enable Access Time		20	35		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		20	35		15	25		15	25	ns
TZX	TEVQX	Output Enable Time		20	35		15	25		15	25	ns
TXZ	TEXQZ	Output Disable Time		20	35		15	25		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S474			DM54S474A			DM54S474B			Units
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
TAA	TAVQV	Address Access Time		40	70		25	60		25	50	ns
TEA	TEVQV	Enable Access Time		20	40		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		20	40		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		20	40		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		20	40		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S475 (512 x 8) 4096-Bit TTL PROM

General Description

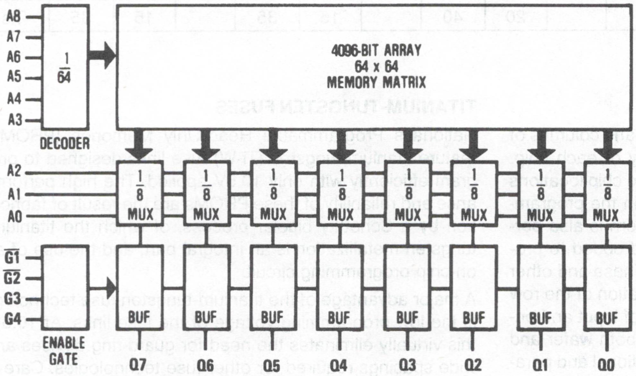
This Schottky memory is organized in the popular 512 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 45 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram


A8
A7
A6
A5
A4
A3
1/64
DECODER
4096-BIT ARRAY
64 x 64
MEMORY MATRIX
A2
A1
A0
1/8
MUX
G1
G2
G3
G4
ENABLE
GATE
BUF
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

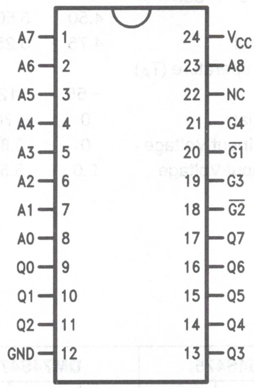
TL/D/9192–1

Pin Names

A0–A8	Addresses
$\overline{G1}$, $\overline{G2}$, G3, G4	Output Enables
GND	Ground
NC	No Connection
Q_0–Q_7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line-Package

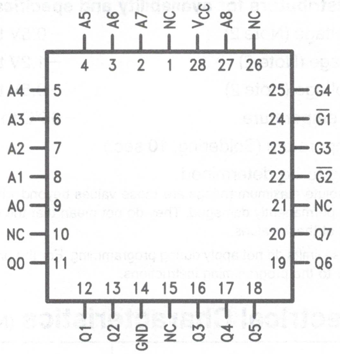

A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
24 V_{CC}
23 A8
22 NC
21 G4
20 $\overline{G1}$
19 G3
18 $\overline{G2}$
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

TL/D/9192–2

Top View

Order Number DM54/74S475J, 475AJ,
DM74S475N or 475AN
See NS Package Number J24A or N24A

Plastic Leaded Chip Carrier (PLCC)


A5 4
A6 3
A7 2
NC 1
V_{CC} 28
A8 27
NC 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
Q0 11
25 G4
24 $\overline{G1}$
23 G3
22 $\overline{G2}$
21 NC
20 Q7
19 Q6
12 Q1
13 Q2
14 GND
15 NC
16 Q3
17 Q4
18 Q5

TL/D/9192–3

Top View

Order Number DM74S475V or 475AV
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S475AJ	45
DM74S475J	65
DM74S475AN	45
DM74S475N	65
DM74S475AV	45
DM74S475V	65

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S475AJ	60
DM54S475J	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logic "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S475			DM74S475			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		115	170		115	170	mA

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics (With Standard Load and Operating Conditions)

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S475			DM74S475A			Units
			Min	Typ	Max	Min	Typ	Max	
T_{AA}	TAVQV	Address Access Time		40	65		25	45	ns
T_{EA}	TEVQV	Enable Access Time		20	35		15	25	ns
T_{ER}	TEXQX	Enable Recovery Time		20	35		15	25	ns
T_{ZX}	TEVQX	Output Enable Time		20	35		15	25	ns
T_{XZ}	TEXQZ	Output Disable Time		20	35		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S475			DM54S475A			Units
			Min	Typ	Max	Min	Typ	Max	
T_{AA}	TAVQV	Address Access Time		40	75		25	60	ns
T_{EA}	TEVQV	Enable Access Time		20	40		15	35	ns
T_{ER}	TEXQX	Enable Recovery Time		20	40		15	35	ns
T_{ZX}	TEVQX	Output Enable Time		20	40		15	35	ns
T_{XZ}	TEXQZ	Output Disable Time		20	40		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti:W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti:W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti:W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S570

(512 x 4) 2048-Bit TTL PROM

General Description

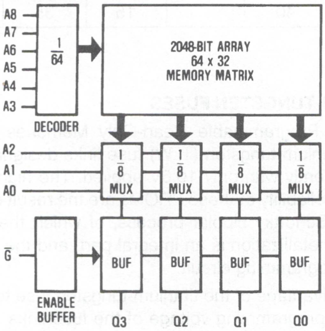
This Schottky memory is organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—45 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram


A8
A7
A6
A5
A4
A3
1/64
DECODER
2048-BIT ARRAY
64 x 32
MEMORY MATRIX
A2
A1
A0
1/8 MUX
1/8 MUX
1/8 MUX
1/8 MUX
G̅
ENABLE BUFFER
BUF
BUF
BUF
BUF
Q3
Q2
Q1
Q0

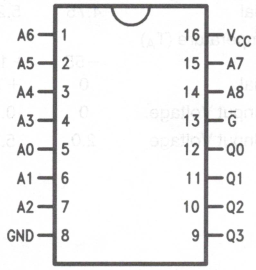
TL/D/9189-1

Pin Names

A0–A8	Addresses
G̅	Enable
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

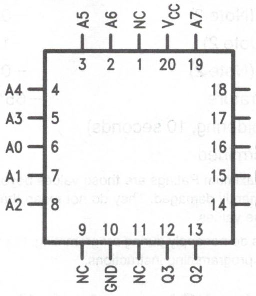

A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 V_{CC}
15 A7
14 A8
13 $\overline{G}$
12 Q0
11 Q1
10 Q2
9 Q3

TL/D/9189–2

Top View

Order Number DM54/74S570J, 570AJ
DM74S570N, 570AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)


A5 3
A6 2
NC 1
V_{CC} 20
A7 19
A4 4
A3 5
A0 6
A1 7
A2 8
18 A8
17 $\overline{G}$
16 Q0
15 NC
14 Q1
9 NC
10 GND
11 NC
12 Q3
13 Q2

TL/D/9189–3

Top View

Order Number DM74S570V, 570AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S570AN	45
DM74S570N	55
DM74S570AJ	45
DM74S570J	55
DM74S570AV	45
DM74S570V	55

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S570AJ	60
DM54S570J	65

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute Maximum Ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S570			DM74S570			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		90	130		90	130	mA

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S570			DM74S570A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		30	45	ns
TEA	TEVQV	Enable Access Time		20	30		15	25	ns
TER	TEXQX	Enable Recovery Time		20	30		15	25	ns
TZX	TEVQX	Output Enable Time		20	30		15	25	ns
TXZ	TEXQZ	Output Disable Time		20	30		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S570			DM54S570A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	65		30	60	ns
TEA	TEVQV	Enable Access Time		20	35		15	35	ns
TER	TEXQX	Enable Recovery Time		20	35		15	35	ns
TZX	TEVQX	Output Enable Time		20	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		20	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S571
(512 x 4) 2048-Bit TTL PROM

General Description

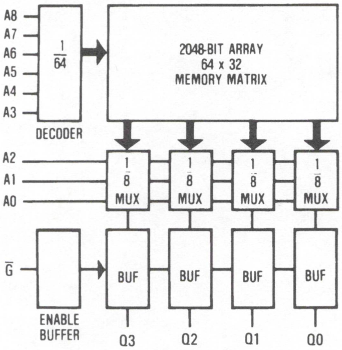
This Schottky memory is organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram


A8
A7
A6
A5
A4
A3
1/64
DECODER
2048-BIT ARRAY
64 x 32
MEMORY MATRIX
A2
A1
A0
1/8 MUX
1/8 MUX
1/8 MUX
1/8 MUX
G̅
ENABLE BUFFER
BUF
BUF
BUF
BUF
Q3
Q2
Q1
Q0

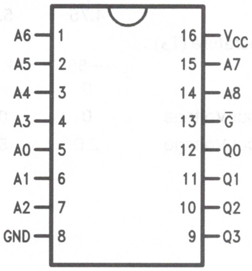
TL/D/9713-1

Pin Names

A0–A8	Address
$\overline{G}$	Output Enable
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

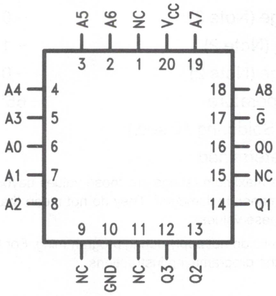

A6
A5
A4
A3
A0
A1
A2
GND
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
V_{CC}
A7
A8
$\overline{G}$
Q0
Q1
Q2
Q3

TL/D/9713–2

Top View

Order Number
DM54/74S571J, 571AJ, 571BJ
DM74S571N, 571AN, 571BN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)


A5
A6
NC
V_{CC}
A7
3
2
1
20
19
A4
A3
A0
A1
A2
4
5
6
7
8
18
17
16
15
14
A8
$\overline{G}$
Q0
NC
Q1
9
10
11
12
13
NC
GND
NC
Q3
Q2

TL/D/9713–3

Top View

Order Number
DM74S571V, 571AV, 571BV
See NS Package Number V20A

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S571AN	45
DM74S571BN	35
DM74S571N	55
DM74S571AJ	45
DM74S571BJ	35
DM74S571J	55
DM74S571AV	45
DM74S571BV	35
DM74S571V	55

Military Temp. Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S571AJ	60
DM54S571BJ	50
DM54S571J	65

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering 10 sec.)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S571			DM74S571			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	µA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	µA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		90	130		90	130	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	µA
					−50			−50	µA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S571			DM74S571A			DM74S571B			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		30	45		30	35	ns
TEA	TEVQV	Enable Access Time		20	30		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		20	30		15	25		15	25	ns
TZX	TEVQX	Output Enable Time		20	30		15	25		15	25	ns
TXZ	TEXQZ	Output Disable Time		20	30		15	25		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S571			DM54S571A			DM54S571B			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	65		30	60		30	50	ns
TEA	TEVQV	Enable Access Time		20	35		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		20	35		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		20	35		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		20	35		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S572 (1024 x 4) 4096-Bit TTL PROM

General Description

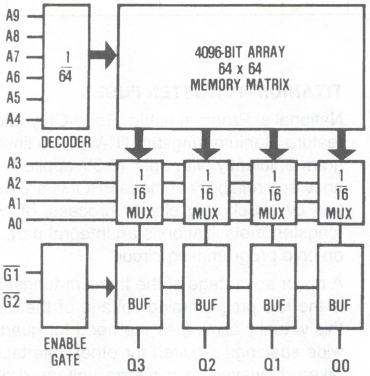
This Schottky memory is organized in the popular 1024 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—45 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open collector outputs

Block Diagram


A9
A8
A7
A6
A5
A4
1/64
DECODER
4096-BIT ARRAY
64 x 64
MEMORY MATRIX
A3
A2
A1
A0
1/16 MUX
1/16 MUX
1/16 MUX
1/16 MUX
$\overline{G1}$
$\overline{G2}$
ENABLE GATE
BUF
BUF
BUF
BUF
Q3
Q2
Q1
Q0

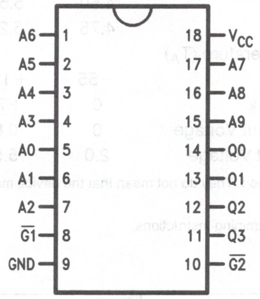
TL/D/9712–1

Pin Names

A0–A9	Addresses
G1, G2	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line-Package

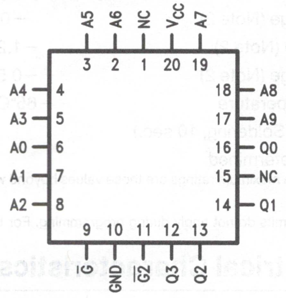

A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
$\overline{G1}$ 8
GND 9
18 V_{CC}
17 A7
16 A8
15 A9
14 Q0
13 Q1
12 Q2
11 Q3
10 $\overline{G2}$

TL/D/9712–2

Top View

Order Number DM54/74S572J, 572AJ, DM74S572N, 572AN
See NS Package Number J18A or N18A

Plastic Leaded Chip Carrier (PLCC)


A5 3
A6 2
NC 1
V_{CC} 20
A7 19
A4 4
A3 5
A0 6
A1 7
A2 8
18 A8
17 A9
16 Q0
15 NC
14 Q1
9 $\overline{G}$
10 GND
11 $\overline{G2}$
12 Q3
13 Q2

TL/D/9712–3

Top View

Order Number DM74S572V, 572AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S572AJ	45
DM74S572J	60
DM74S572AN	45
DM74S572N	60
DM74S572AV	45
DM74S572V	60

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S572AJ	60
DM54S572J	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C
ESD to be determined	

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logic "1" Input Voltage	2.0	5.5	V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S572			DM74S572			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140		100	140	mA

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = +25°C.

AC Electrical Characteristics (With Standard Load and Operating Conditions)

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S572			DM74S572A			Units
			Min	Typ	Max	Min	Typ	Max	
T_{AA}	TAVQV	Address Access Time		40	60		25	45	ns
T_{EA}	TEVQV	Enable Access Time		20	35		15	25	ns
T_{ER}	TEXQX	Enable Recovery Time		20	35		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S572			DM54S572A			Units
			Min	Typ	Max	Min	Typ	Max	
T_{AA}	TAVQV	Address Access Time		40	75		25	60	ns
T_{EA}	TEVQV	Enable Access Time		20	45		15	35	ns
T_{ER}	TEXQX	Enable Recovery Time		20	45		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S573
(1024 x 4) 4096-Bit TTL PROM

General Description

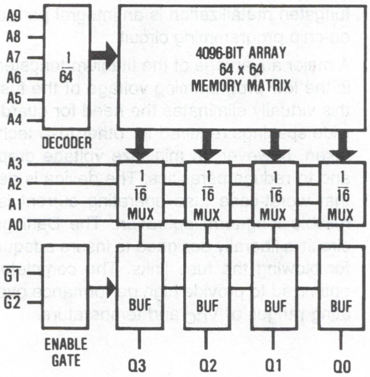
This Schottky memory is organized in the popular 1024 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® Outputs

Block Diagram


A9
A8
A7
A6
A5
A4
1/64
DECODER
4096-BIT ARRAY
64 x 64
MEMORY MATRIX
A3
A2
A1
A0
1/16 MUX
1/16 MUX
1/16 MUX
1/16 MUX
G1
G2
ENABLE GATE
BUF
BUF
BUF
BUF
Q3
Q2
Q1
Q0

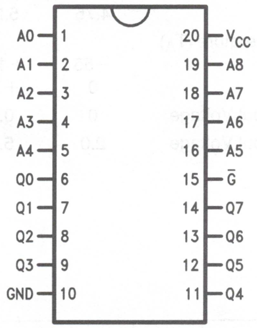
TL/D/9193–1

Pin Names

A0–A9	Addresses
G1–G2	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

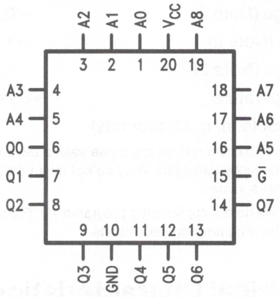

A0 1
A1 2
A2 3
A3 4
A4 5
Q0 6
Q1 7
Q2 8
Q3 9
GND 10
20 V_{CC}
19 A8
18 A7
17 A6
16 A5
15 $\overline{G}$
14 Q7
13 Q6
12 Q5
11 Q4

TL/D/9193-2

Top View

Order Number
DM54/74S573J, 573AJ, 573BJ
DM74S573N, 573AN, 573BN
See NS Package Number J18A or N18A

Plastic Leaded Chip Carrier (PLCC)


A2
A1
A0
V_{CC}
A8
3
2
1
20
19
A3 4
A4 5
Q0 6
Q1 7
Q2 8
18 A7
17 A6
16 A5
15 $\overline{G}$
14 Q7
9
10
11
12
13
Q3
GND
Q4
Q5
Q6

TL/D/9193-3

Top View

Order Number
DM74S573V, 573AV, 573BV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S573AJ	45
DM74S573BJ	35
DM74S573J	60
DM74S573AN	45
DM74S573BN	35
DM74S573N	60
DM74S573AV	45
DM74S573BV	35
DM74S573V	60

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S573AJ	60
DM54S573BJ	50
DM54S573J	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S573			DM74S573			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140		100	140	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S573			DM74S573A			DM74S573B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	60		25	45		25	35	ns
TEA	TEVQV	Enable Access Time		20	35		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		20	35		15	25		15	25	ns
TZX	TEVQX	Output Enable Time		20	35		15	25		15	25	ns
TXZ	TEXQZ	Output Disable Time		20	35		15	25		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S573			DM54S573A			DM54S573B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		25	60		25	50	ns
TEA	TEVQV	Enable Access Time		20	45		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		20	45		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		20	45		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		20	45		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87S180, DM77/87S280 (1024 x 8) 8192-Bit TTL PROMs

General Description

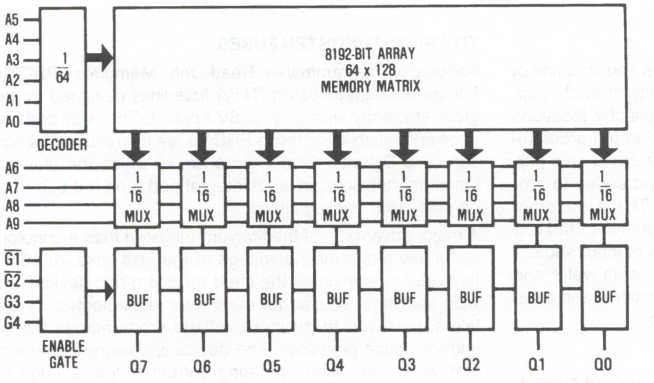
These Schottky memories are organized in the popular 1024 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—55 ns max
  - Enable access—30 ns max
  - Enable recovery—30 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram


A5
A4
A3
A2
A1
A0
1/64
DECODER
8192-BIT ARRAY
64 x 128
MEMORY MATRIX
A6
A7
A8
A9
1/16 MUX
G1
G2
G3
G4
ENABLE GATE
BUF
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

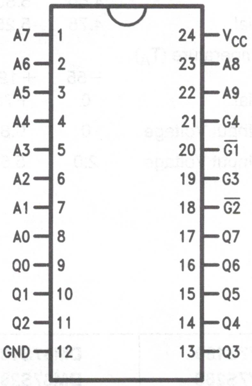
TL/D/9716-1

Pin Names

A0–A9	Addresses
$\overline{G1}$, $\overline{G2}$, G3, G4	Output Enables
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line-Package

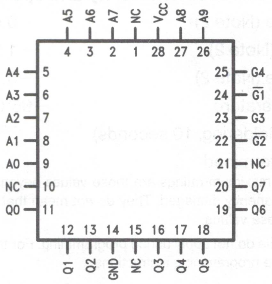

A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
24 V_{CC}
23 A8
22 A9
21 G4
20 $\overline{G1}$
19 G3
18 $\overline{G2}$
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

TL/D/9716-2

Top View

Order Number DM77/87S180J, 280J
DM87S180N, 280N
See NS Package Number J24A, J24F, N24A or N24C

Plastic Leaded Chip Carrier (PLCC)


A5 4
A6 3
A7 2
NC 1
V_{CC} 28
A8 27
A9 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
Q0 11
25 G4
24 $\overline{G1}$
23 G3
22 $\overline{G2}$
21 NC
20 Q7
19 Q6
12 Q1
13 Q2
14 GND
15 NC
16 Q3
17 Q4
18 Q5

TL/D/9716-3

Top View

Order Number DM87S180V
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	24-Pin Standard DIP	24-Pin Narrow DIP	Max Access Time (ns)
DM87S180J	X		55
DM87S180N	X		55
DM87S180V	X		55
DM87S280J		X	55
DM87S280N		X	55

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	24-Pin Standard DIP	24-Pin Narrow DIP	Max Access Time (ns)
DM77S180J	X		75
DM77S280J		X	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S180 DM77S280			DM87S180 DM87S280			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		115	170		115	170	mA

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM87S180 DM87S280			Units
			Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55	ns
TEA	TEVQV	Enable Access Time		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM77S180 DM77S280			Units
			Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75	ns
TEA	TEVQV	Enable Access Time		15	35	ns
TER	TEXQX	Enable Recovery Time		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87S181, DM77/87S281 (1024 x 8) 8192-Bit TTL PROMs

General Description

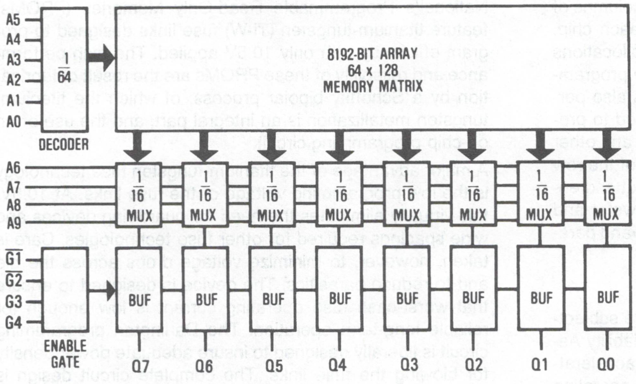
These Schottky memories are organized in the popular 1024 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—45 ns max
  Enable access—30 ns max
  Enable recovery—30 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram


A5
A4
A3
A2
A1
A0
1 of 64
DECODER
8192-BIT ARRAY
64 x 128
MEMORY MATRIX
A6
A7
A8
A9
1 of 16 MUX
BUF
G1
G2
G3
G4
ENABLE GATE
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

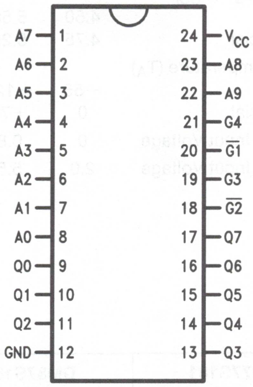
TL/D/9194-1

Pin Names

A0–A9	Addresses
$\overline{G1}$, $\overline{G2}$, G3, G4	Output Enables
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

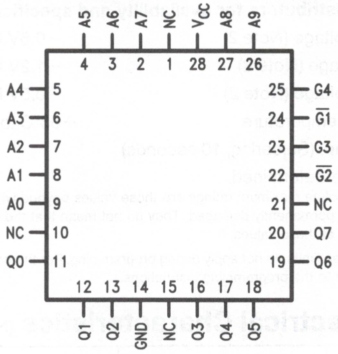

A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
24 V_{CC}
23 A8
22 A9
21 G4
20 $\overline{G1}$
19 G3
18 $\overline{G2}$
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

TL/D/9194–2

Top View

Order Number DM77/87S181J, 281J, 181AJ, 281AJ, DM87S181N, 281N, 181AN, 281AN
See NS Package Number J24A, J24F, N24A or N24C

Plastic Leaded Chip Carrier (PLCC)


A5 4
A6 3
A7 2
NC 1
V_{CC} 28
A8 27
A9 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
Q0 11
25 G4
24 $\overline{G1}$
23 G3
22 $\overline{G2}$
21 NC
20 Q7
19 Q6
12 Q1
13 Q2
14 GND
15 NC
16 Q3
17 Q4
18 Q5

TL/D/9194–3

Top View

Order Number DM87S181V
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	24-Pin Standard DIP	24-Pin Narrow DIP	Max Access Time (ns)
DM87S181AJ	X		45
DM87S181J	X		55
DM87S181AN	X		45
DM87S181N	X		55
DM87S181V	X		55
DM87S281AJ		X	45
DM87S281J		X	55
DM87S281AN		X	45
DM87S281N		X	55

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	24-Pin Standard DIP	24-Pin Narrow DIP	Max Access Time (ns)
DM77S181AJ	X		65
DM77S181J	X		75
DM77S281AJ		X	65
DM77S281J		X	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD to be determined.

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S181 DM77S281			DM87S181 DM87S281			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		115	170		115	170	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM87S181 DM87S281			DM87S181A DM87S281A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		35	45	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM77S181 DM77S281			DM77S181A DM77S281A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		35	65	ns
TEA	TEVQV	Enable Access Time		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National
Semiconductor

DM77/87S184
(2048 x 4) 8192-Bit TTL PROM

General Description

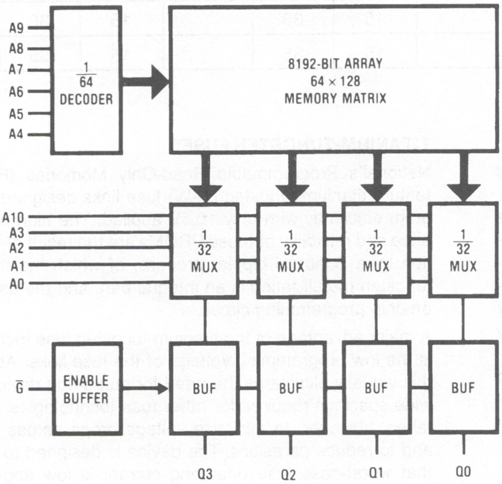
This Schottky memory is organized in the popular 2048 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—55 ns max
  Enable access—25 ns max
  Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram


A9
A8
A7
A6
A5
A4
1/64 DECODER
8192-BIT ARRAY
64 × 128
MEMORY MATRIX
A10
A3
A2
A1
A0
1/32 MUX
1/32 MUX
1/32 MUX
1/32 MUX
G
ENABLE BUFFER
BUF
BUF
BUF
BUF
Q3
Q2
Q1
Q0

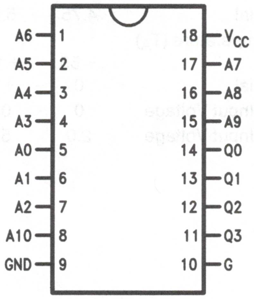
TL/D/9717-1

Pin Names

A0–A10	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

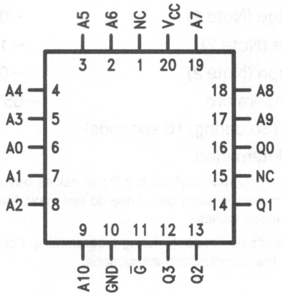

A6
1
A5
2
A4
3
A3
4
A0
5
A1
6
A2
7
A10
8
GND
9
18
V_{CC}
17
A7
16
A8
15
A9
14
Q0
13
Q1
12
Q2
11
Q3
10
G

TL/D/9717-2

Top View

Order Number DM77/87S184J, 184AJ or DM87S184N, 184AN
See NS Package Number J18A or N18A

Plastic Leaded Chip Carrier (PLCC)


A5
A6
NC
V_{CC}
A7
3
2
1
20
19
A4
4
A3
5
A0
6
A1
7
A2
8
18
A8
17
A9
16
Q0
15
NC
14
Q1
9
10
11
12
13
A10
GND
G
Q3
Q2

TL/D/9717-3

Top View

Order Number DM87S184V, 184AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Acces Time (ns)
DM87S184AN	45
DM87S184N	55
DM87S184AJ	45
DM87S184J	55
DM87S184AV	45
DM87S184V	55

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Acces Time (ns)
DM77S184J	70
DM77S184AJ	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined.	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S184			DM87S184			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			26			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140		100	140	mA

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM87S184			DM87S184A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		30	45	ns
TEA	TEVQV	Enable Access Time		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		15	25		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM77S184			DM77S184A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	70		30	60	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87S185 (2048 x 4) 8192-Bit TTL PROM

General Description

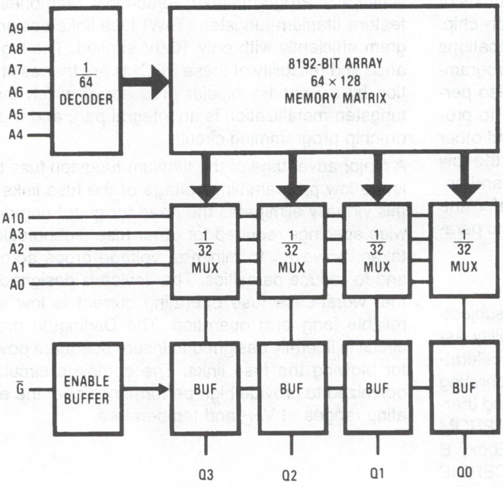
This Schottky memory is organized in the popular 2048 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—35 ns max
  Enable access—25 ns max
  Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram


A9
A8
A7
A6
A5
A4
1/64 DECODER
8192-BIT ARRAY
64 × 128
MEMORY MATRIX
A10
A3
A2
A1
A0
1/32 MUX
1/32 MUX
1/32 MUX
1/32 MUX
G̅
ENABLE BUFFER
BUF
BUF
BUF
BUF
Q3
Q2
Q1
Q0

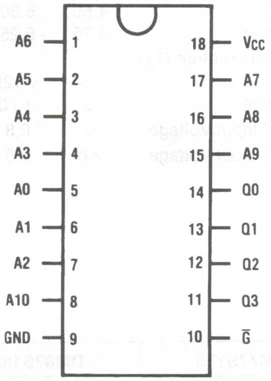
TL/D/9197-1

Pin Names

A0–A10	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line-Package

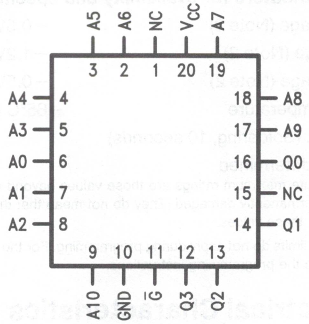

A6
1
A5
2
A4
3
A3
4
A0
5
A1
6
A2
7
A10
8
GND
9
18
VCC
17
A7
16
A8
15
A9
14
Q0
13
Q1
12
Q2
11
Q3
10
G̅

TL/D/9197-2

Top View

Order Number DM77/87S185J, 185AJ, 185BJ
DM87S185N, 185AN, 185BN
See NS Package Number J18A or N18A

Plastic Leaded Chip Carrier (PLCC)


A5
A6
NC
VCC
A7
3
2
1
20
19
A4
4
A3
5
A0
6
A1
7
A2
8
18
A8
17
A9
16
Q0
15
NC
14
Q1
9
10
11
12
13
A10
GND
G̅
Q3
Q2

TL/D/9197-3

Top View

Order Number DM87S185V, 185AV, 185BV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM87S185AJ	45
DM87S185BJ	35
DM87S185J	55
DM87S185AN	45
DM87S185BN	35
DM87S185N	55
DM87S185AV	45
DM87S185BV	35
DM87S185V	55

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM77S185AJ	60
DM77S185BJ	50
DM77S185J	70

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S185			DM87S185			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140		100	140	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM87S185			DM87S185A			DM87S185B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		30	45		25	35	ns
TEA	TEVQV	Enable Access Time		15	25		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		15	25		15	25		15	25	ns
TZX	TEVQX	Output Enable Time		15	25		15	25		15	25	ns
TXZ	TEXQZ	Output Disable Time		15	25		15	25		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM77S185			DM77S185A			DM77S185B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	70		30	60		25	50	ns
TEA	TEVQV	Enable Access Time		15	30		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

3

National Semiconductor

DM77/87SR474
(512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR474 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined micro-programmed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR474 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{\text{GS}}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{\text{G}}$) is held high. The outputs are enabled when $\overline{\text{GS}}$ is brought low before the rising edge of the clock and $\overline{\text{G}}$ is held low. The $\overline{\text{GS}}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

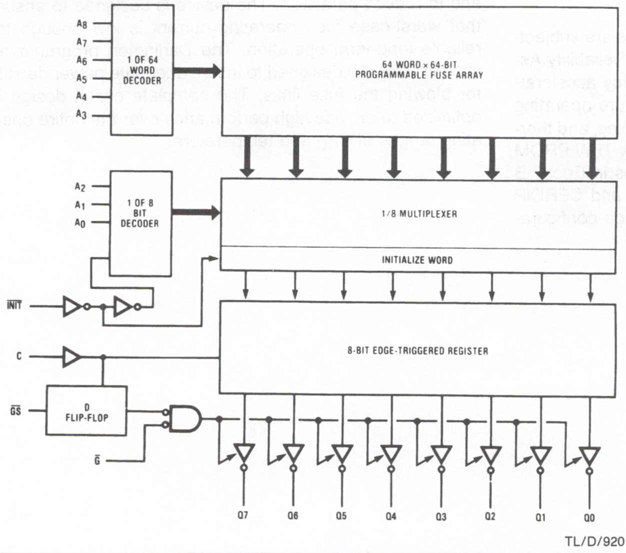
The DM77/87SR474 also features an initialize function, $\overline{\text{INIT}}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{\text{INIT}}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of the $\overline{\text{INIT}}$ is all lows, providing a $\overline{\text{CLEAR}}$ function when not programmed.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable synchronous register INITIALIZE
- 24-pin, 300 mil thin-DIP package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature
- Pinout compatible with DM77SR181 (1k x 8) Registered PROM for future expansion

Block Diagram



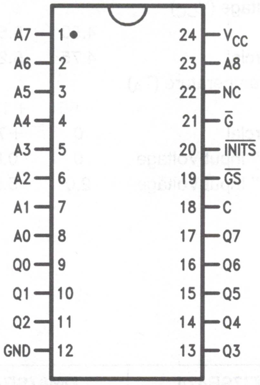
TL/D/9201–1

Pin Names

A0–A8	Addresses
C	Clock
$\overline{\text{G}}$	Output Enable
GND	Ground
$\overline{\text{GS}}$	Synchronous Output Enable
$\overline{\text{INIT}}$	Initialize
NC	No Connection
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line-Package

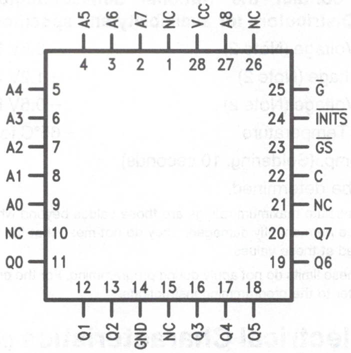

A7 1 • 24 V_{CC}
A6 2 23 A8
A5 3 22 NC
A4 4 21 $\overline{G}$
A3 5 20 $\overline{INITS}$
A2 6 19 $\overline{GS}$
A1 7 18 C
A0 8 17 Q7
Q0 9 16 Q6
Q1 10 15 Q5
Q2 11 14 Q4
GND 12 13 Q3

TL/D/9201-2

Top View

Order Number DM77/87SR474J, 474BJ
DM87SR474N, 474BN
See NS Package Number J24A or N24A

Plastic Chip Carrier (PLCC)


A5 4
A6 3
A7 2
NC 1
V_{CC} 28
A8 27
NC 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
Q0 11
25 $\overline{G}$
24 $\overline{INITS}$
23 $\overline{GS}$
22 C
21 NC
20 Q7
19 Q6
12 Q1
13 Q2
14 GND
15 NC
16 Q3
17 Q4
18 Q5

TL/D/9201-3

Top View

Order Number DM87SR474V, 474BV
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Min Address to CLK Setup Time (ns)
DM87SR474BJ	35
DM87SR474J	50
DM87SR474BN	35
DM87SR474N	50
DM87SR474BV	35
DM87SR474V	50

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Min Address to CLK Setup Time (ns)
DM77SR474BJ	40
DM77SR474J	55

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined.	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77SR474			DM87SR474			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		135	185		135	185	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR474			DM87SR474			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	SR474	55	20		50	20		ns
		SR474B	40	20		35	20		
$t_{H(A)}$	Address to C (High) Hold Time		0	−5		0	−5		ns
$t_{S(\overline{INITS})}$	$\overline{\text{INITS}}$ to C (High) Setup Time		30	20		25	20		ns
$t_{H(\overline{INITS})}$	$\overline{\text{INITS}}$ to C (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)	SR474		15	30		15	27	ns
		SR474B		15	25		15	20	
$t_{WH(C)}$ $t_{WL(C)}$	C Width (High or Low)		25	13		20	13		ns
$t_{S(\overline{GS})}$	$\overline{\text{GS}}$ to C (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{\text{GS}}$ to C (High) Hold Time		5	0		5	0		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Output Active (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{\text{G}}$ (Low) to Output Active (High or Low)			15	30		15	25	ns
$t_{PLZ(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Output Inactive (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{\text{G}}$ (Low) to Output Inactive (TRI-STATE)			15	30		15	25	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87SR476
(512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR476 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined micro-programmed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR476 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

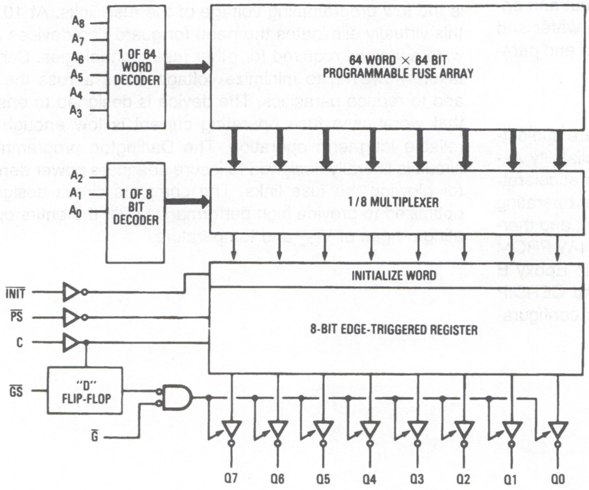
The DM77SR476 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the output register when $\overline{INIT}$ is brought low. The unprogrammed state of the $\overline{INIT}$ is all lows $\overline{PS}$ loads ones into the output registers when brought low.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with AM27S25
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable asynchronous INITIALIZE
- 24-pin, 300 mil thin-dip package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameter's guaranteed over temperature
- Preset input

Block Diagram



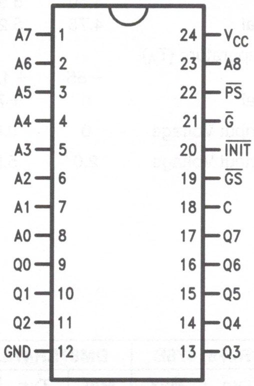
TL/D/9202-1

Pin Names

A0–A8	Addresses
C	Clock
$\overline{G}$	Output Enable
GND	Ground
$\overline{GS}$	Synchronous Output Enable
$\overline{INIT}$	Initialize
$\overline{PS}$	Preset
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

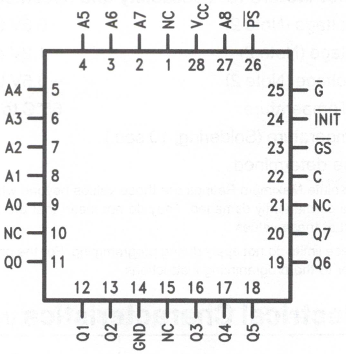

A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
24 VCC
23 A8
22 PS
21 G
20 INIT
19 GS
18 C
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

TL/D/9202-2

Top View

Order Number DM77/87SR476J, 476BJ, DM87SR476N or 476BN
See NS Package Number J24A or N24A

Plastic Chip Carrier (PLCC)


A5 A6 A7 NC VCC A8 PS
4 3 2 1 28 27 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
Q0 11
25 G
24 INIT
23 GS
22 C
21 NC
20 Q7
19 Q6
12 13 14 15 16 17 18
Q1 Q2 GND NC Q3 Q4 Q5

TL/D/9202-3

Top View

Order Number DM87SR476V or 476BV
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Min Address to CLK Setup Time
DM87SR476BJ	35
DM87SR476J	50
DM87SR476BN	35
DM87SR476N	50
DM87SR476BV	35
DM87SR476V	50

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Min Address to CLK Setup Time
DM77SR476BJ	40
DM77SR476J	55

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD to be determined	

Note 1: Absolute Maximum Ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77SR476, 476B			DM87SR476, 476B			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		135	185		135	185	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurements, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR476, 476B			DM87SR476, 476B			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	SR476	55	20		50	20		ns
		SR476B	40	20		35	20		
$t_{H(A)}$	Address to C (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)	SR476		15	30		15	27	ns
		SR476B		15	25		15	20	
$t_{WH(C)}$ $t_{WL(C)}$	C Width (High or Low)		25	13		20	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to C (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to C (High) Hold Time		5	0		5	0		ns
$t_{PLH(\overline{PS})}$	Delay from $\overline{PS}$ (Low) to Output (High)			20	40		20	30	ns
$t_{PLH(\overline{INIT})}$ $t_{PHL(\overline{INIT})}$	Delay from $\overline{INIT}$ (Low) to Output (Low or High)			20	40		20	30	ns
$t_{WL(\overline{PS})}$	$\overline{PS}$ Pulse Width (Low)		15	10		15	10		ns
$t_{WL(\overline{INIT})}$	$\overline{INIT}$ Pulse Width (Low)		15	10		15	10		ns
$t_{S(\overline{PS})}$	$\overline{PS}$ Recovery (High) to C (High)		25	10		20	10		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ Recovery (High) to C (High)		25	10		20	10		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (High or Low)			15	30		15	25	ns
$t_{PZL(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87SR27 (512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR27 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8 bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR27 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

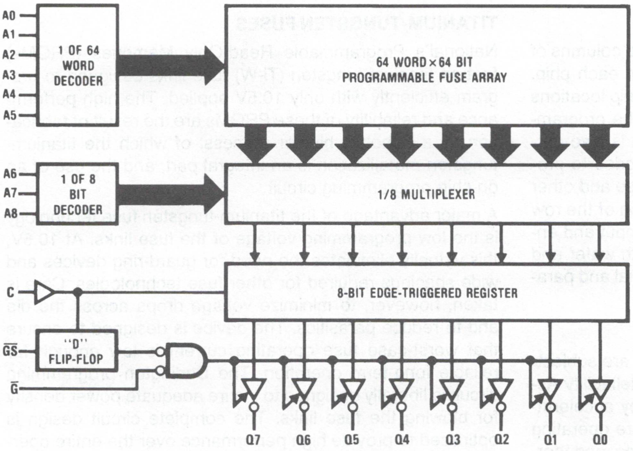
Data is read from the PROM by first applying an address to inputs A0–A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with Am27S27
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- 22-pin 400-mil thin-DIP package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block Diagram



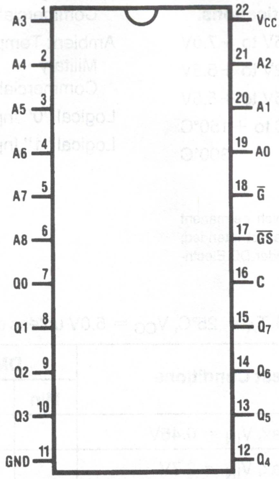
TL/D/6686–1

Pin Names

A0–A8	Addresses
C	Clock
$\overline{G}$	Output Enable
GND	Ground
$\overline{GS}$	Synchronous Output Enable
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagram

Dual-In-Line Package


A3 1
A4 2
A5 3
A6 4
A7 5
A8 6
Q0 7
Q1 8
Q2 9
Q3 10
GND 11
22 V_{CC}
21 A2
20 A1
19 A0
18 $\overline{G}$
17 $\overline{GS}$
16 C
15 Q_7
14 Q_6
13 Q_5
12 Q_4

TL/D/6686-2

Top View

Order Number DM77/87SR27J, DM77/87SR27BJ,
DM87SR27N or DM87SR27BN
See NS Package Number J22A or N22A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Min Address to C Setup Time (ns)
DM87SR27BJ	35
DM87SR27J	50
DM87SR27BN	35
DM87SR27N	50

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Min Address to C Setup Time (ns)
DM77SR27BJ	40
DM77SR27J	55

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 1)	−0.5V to +7.0V
Input Voltage (Note 1)	−1.2V to +5.5V
Output Voltage (Note 1)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operations should be limited to those conditions specified under DC Electrical Characteristics.

Operating Conditions

Supply Voltage (V_{CC})	
Military	4.5V to 5.5V
Commercial	4.75V to 5.25V
Ambient Temperature (T_A)	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Logical "0" Input Voltage	0V to 0.8V
Logical "1" Input Voltage	2.0V to 5.5V

DC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$ unless otherwise specified

Symbol	Parameter	Test Conditions	DM77SR27			DM87SR27			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	µA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	µA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		135	185		135	185	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	µA
					−50			−50	µA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR27			DM87SR27			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	SR27	55	20		50	20		ns
		SR27B	40	20		35	20		
$t_{H(A)}$	Address to C (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)	SR27		15	30		15	27	ns
		SR27B		15	25		15	20	
$t_{WH(C)}$ $t_{WL(C)}$	C Width (High or Low)		25	13		25	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to C (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to C (High) Hold Time		5	0		5	0		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High)			15	30		15	25	ns
$t_{PLZ(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns

Programming Parameters Do not test or you may program the device

Symbol	Parameter	Test Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10	10.5	11	V
I_{CCP}	I_{CC} During Programming	$V_{CC} = 11V$			750	mA
V_{OP}	Required Output Voltage for Programming		10	10.5	11	V
I_{OP}	Output Current While Programming	$V_{OUT} = 11V$			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1		10	V/µs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	µs
V_{CCVL}	Required Low V_{CC} for Verification		3.8	4	4.2	V
V_{CCVH}	Required High V_{CC} for Verification		5.8	6	6.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Functional Description

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

Functional Description (Continued)

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

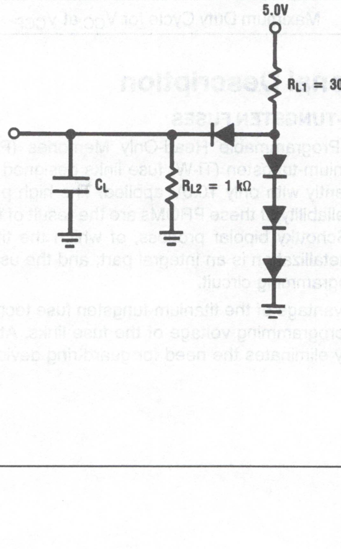
DM77/87SR27 Programming Procedure

National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. To generate high (logical "1") levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed.

1. Programming should be attempted only at ambient temperatures between 15 and 30 degrees Celsius.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedures must be followed:
   - a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to asynchronous chip Enable input $\overline{G}$. Synchronous chip Enable $\overline{GS}$ should be held low throughout the entire programming procedure.
   - b) Increase V_{CC} from nominal 10.5V (±0.5V) with a slew rate between 1.0 V/µs and 10 V/µs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11V.
   - c) Select the output where a logical high is desired by raising that output voltage to 10.5V (±0.5V). Limit the slew rate from 1.0 V/µs to 10 V/µs. This voltage may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum. (Remember that the outputs of the device are disabled at this time.)
   - d) Enable the device by taking the chip Enable $\overline{G}$ to a low level. This is done with a pulse of 10 µs. The 10 µs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
   - e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V (±0.2V) for one verification and to 6.0V (±0.2V) for a second verification. Verification at V_{CC} levels of 4.0V and 6.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. Each data verification must be preceded by a positive going (low to high) clock edge to load the data from the array into the output register. The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.
   - f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   - g) Repeat steps a through e for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enable device is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

AC Test Load



TL/D/6686–3

National Semiconductor

DM77/87SR181
(1024 x 8) 8k-Bit Registered TTL PROM

General Description

The DM77/87SR181 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on chip. This device is organized as 1024-words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined micro-programmed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR181 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{\text{GS}}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{\text{G}}$) is held high. The outputs are enabled when $\overline{\text{GS}}$ is brought low before the rising edge of the clock and $\overline{\text{G}}$ is held low. The $\overline{\text{GS}}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

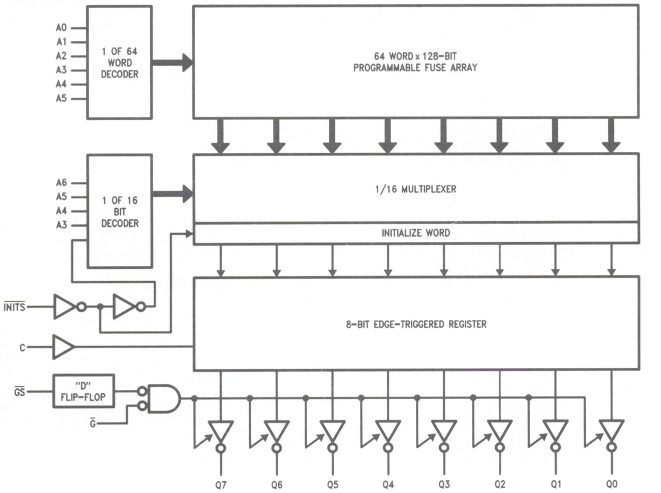
The DM77/87SR181 also features an initialize function $\overline{\text{INIT}}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{\text{INIT}}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of the $\overline{\text{INIT}}$ is all lows.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable register initialize
- 24-pin, 300 mil package
- 40 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block Diagram



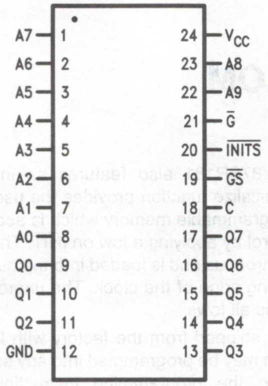
TL/D/9195-1

Pin Names

A0–A9	Addresses
C	Clock
$\overline{\text{G}}$	Output Enable
GND	Ground
$\overline{\text{GS}}$	Synchronous Output Enable
$\overline{\text{INITS}}$	Initialize
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

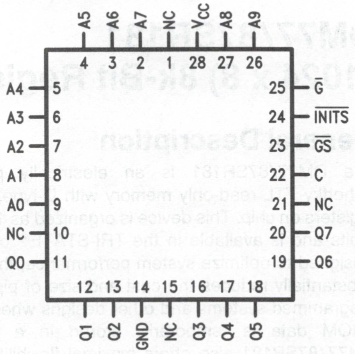

A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
24 V$_{CC}$
23 A8
22 A9
21 $\overline{G}$
20 $\overline{INITS}$
19 $\overline{GS}$
18 C
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

TL/D/9195-2

Top View

Order Number DM77/87SR181J or DM87SR181N
See NS Package Number J24A or N24A

Plastic Leaded Chip Carrier (PLCC)


A5 4
A6 3
A7 2
NC 1
V$_{CC}$ 28
A8 27
A9 26
A4 5
A3 6
A2 7
A1 8
A0 9
NC 10
Q0 11
25 $\overline{G}$
24 $\overline{INITS}$
23 $\overline{GS}$
22 C
21 NC
20 Q7
19 Q6
12 Q1
13 Q2
14 GND
15 NC
16 Q3
17 Q4
18 Q5

TL/D/9195-3

Top View

Order Number DM87SR181V
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number
DM87SR181J
DM87SR181N
DM87SR181V

Military Temp Range (−55°C to +125°C)

Parameter/Order Number
DM77SR181J

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD rating to be determined.

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at those values.

Note 2: These limits do not apply during programming. For the programming settings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77SR181			DM87SR181			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		115	175		115	175	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter	Conditions	DM77SR181			DM87SR181			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	$C_L = 30$ pF	50	20		40	20		ns
$t_{H(A)}$	Address to C (High) Hold Time		0	−5		0	−5		ns
$t_{S(\overline{INITS})}$	$\overline{\text{INITS}}$ to C (High) Setup Time		35	20		30	20		ns
$t_{H(\overline{INITS})}$	$\overline{\text{INITS}}$ to C (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)			15	30		15	20	ns
$t_{WH(C)}$ $t_{WL(C)}$	C Width (High or Low)		25	13		20	13		ns
$t_{S(\overline{GS})}$	$\overline{\text{GS}}$ to C (High) Setup Time		15	0		15	0		ns
$t_{H(\overline{GS})}$	$\overline{\text{GS}}$ to C (High) Hold Time		5	0		5	0		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Active Output (High or Low)	$C_L = 30$ pF		20	30		20	25	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{\text{G}}$ (Low) to Active Output (Low or High)			15	30		15	25	ns
$t_{PLZ(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Inactive Output (TRI-STATE)	$C_L = 5$ pF (Note 1)		20	30		20	25	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{\text{G}}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns

Note: All typical values are for $V_{CC} = 5V$, $T_A = 25°C$.

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

Bipolar PROM Devices in Plastic Leaded Chip Carriers (PLCC)

Introduction of Surface Mount Technology

Recent years have seen rapid advances in microcircuit technology. The integrated circuits of the 1980's are more complex than the circuit boards of the 1960's. It is evident that the next decade will bring demands for packages with higher lead counts and closer lead spacing, both to support the greater system density sought by designers.

National Semiconductor Corporation is committed to surface mount devices, for they provide the most practical solution to these needs. Geared to development of high-complexity semiconductor chips National has placed great emphasis on package development and introducing plastic leaded chip carriers with various number of leads as surface mounted components.

Features of Surface Mount Devices

Surface mount devices have additional features compared to molded Dual-In-Line Packages (DIP):

1. Compact design that saves space during assembly.
2. Mounting on both sides of the substrate.
3. Easier handling and excellent reliability.
4. Automation of the assembly process.
5. Lower board manufacturing costs.
6. Improved operating speed.
7. Increased board density and reduced weight.

Applications

Surface mount devices can be used where substrate size, as well as weight and thickness are limited. The surface mount device can also be used in areas where conventional packages cannot be used. Areas of application include; portable video cassette recorders, video cameras, hand-held computers, personal computers, electronic toys, car electronics, cameras, telephones, and various telecommunication equipment.

Products in PLCC

National Semiconductor has a broad Family of high performance PROMs. All the PAL and PROM products presently offered in DIP packages will now be available in the PLCC (plastic leaded chip carrier) package including the 15 ns industries fastest PAL.

Advantages of PLCC

1. Permits automated assembly.
2. Lower manufacturing costs.
3. Smaller PLCC size, reduces board density and weight.
4. Lower noise and improved frequency response resulting from shorter circuit paths. Automated assembly ensures accurate component placement which improves reliability and provides more consistent product quality.

Additional Information

National Semiconductor offers a variety of technical briefs covering surface mount topics. These include:

STAR™ Tape-and-Reel Shipping System
Order Number 113635

Getting Started in Surface Mount (Equipment Suppliers)
Order Number 570435

A Basic Guide to Surface Mounting of Electronic Components
Order Number 113615

Reliability Report: Small Outline Packages
Order Number 570430

Reliability Report: Plastic Chip Carrier
Order Number 980040

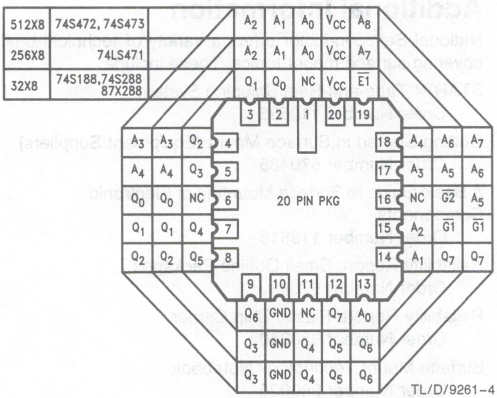
Surface Mount Technology Notebook
Order Number 980020

Plastic Chip Carrier Technology
Order Number 113295

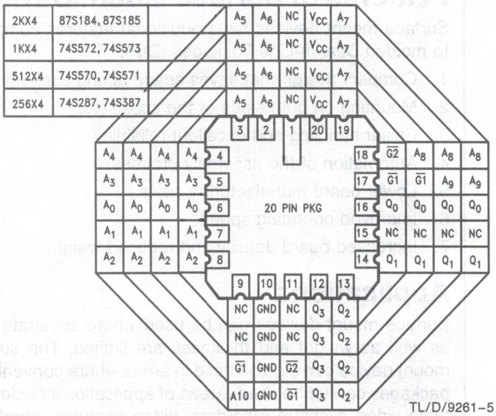
PROM

Series-20 Selection Chart

Device	Size (Bits)	Configuration	TAA (max) in ns			ICC max in mA	DIP pins	PLCC pins
			STD	A-Series	B-Series			
DM74S188 OC DM74S288 TS	256	32 × 8	35	25	—	110	16	20
PL87X288 TS	256	32 × 8	—	—	15	140	16	
DM74S287 TS DM74S387 OC	1K	256 × 4	50	30	—	130	16	
DM74S570 OC DM74S571 TS	2K	512 × 4	55 55	45 45	— 35	130	16	
DM74LS471 TS	2K	256 × 8	60	—	—	100	20	
DM74S572 OC DM74S573 TS	4K	1,024 × 4	60 60	45 45	— 35	140 140	18 18	
DM74S472 TS DM74S473 OC	4K	512 × 8	60 55	45 45	35 —	155 155	20 20	
DM87S184 OC DM87S185 TS	8K	2048 × 4	55 55	45 45	— 35	140 140	18 18	


512X8 74S472, 74S473
256X8 74LS471
32X8 74S188,74S288 87X288
20 PIN PKG

TL/D/9261-4


2KX4 87S184, 87S185
1KX4 74S572, 74S573
512X4 74S570, 74S571
256X4 74S287, 74S387
20 PIN PKG

TL/D/9261-5

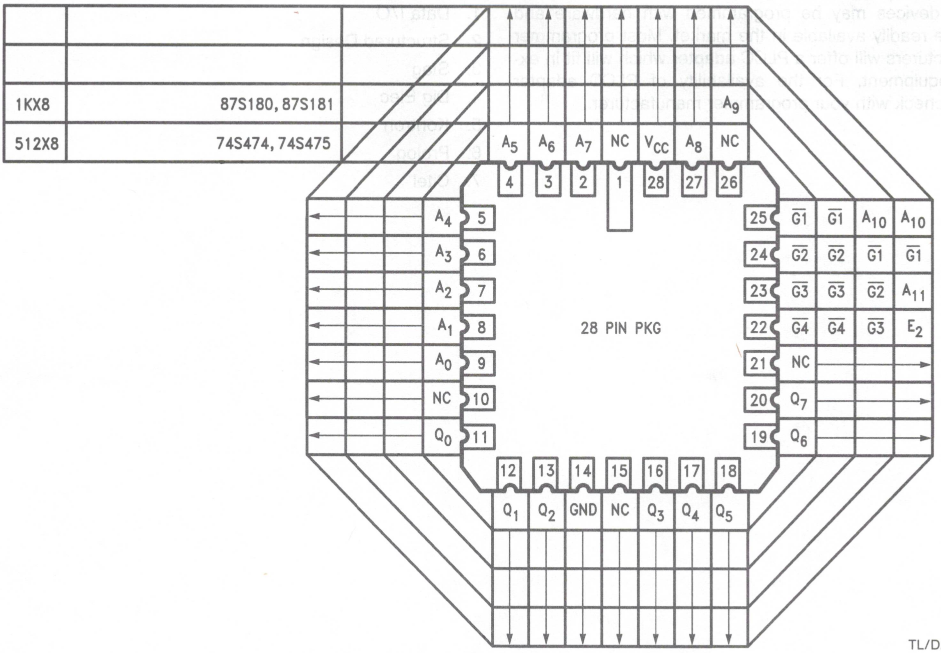
Top View

Series-24 Selection Chart

Device	Size (Bits)	Configuration	TAA (max) in ns			ICC max in mA	DIP pins	PLCC pins
			STD	A-Series	B-Series			
DM74S474 TS DM74S475 OC	4K	512 × 8	65	45	35	170	24	28
DM87SR474 REG DM87SR476 REG	4K	512 × 8	50*	—	35*	170	24	
DM87S180 OC DM87S181 TS DM87SR181 REG	8K	1024 × 8	55 55 40*	— 45 —	— — —	170	24	

*setup time

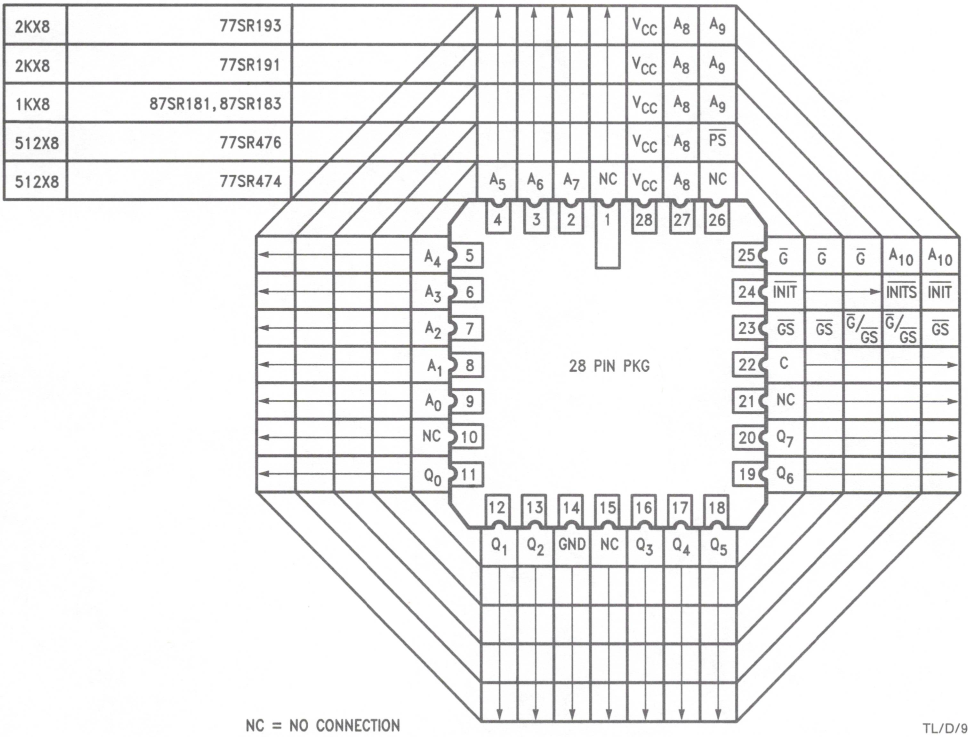
Plastic Leaded Chip Carrier


1KX8
87S180, 87S181
512X8
74S474, 74S475
A_9
A_5 A_6 A_7 NC V_{CC} A_8 NC
4 3 2 1 28 27 26
A_4 5
A_3 6
A_2 7
A_1 8
A_0 9
NC 10
Q_0 11
28 PIN PKG
25 $\overline{G1}$ $\overline{G1}$ A_{10} A_{10}
24 $\overline{G2}$ $\overline{G2}$ $\overline{G1}$ $\overline{G1}$
23 $\overline{G3}$ $\overline{G3}$ $\overline{G2}$ A_{11}
22 $\overline{G4}$ $\overline{G4}$ $\overline{G3}$ E_2
21 NC
20 Q_7
19 Q_6
12 13 14 15 16 17 18
Q_1 Q_2 GND NC Q_3 Q_4 Q_5

TL/D/9261-6

FIGURE 5. Bipolar PROM Pinout

Plastic Leaded Chip Carrier


2KX8 77SR193
2KX8 77SR191
1KX8 87SR181, 87SR183
512X8 77SR476
512X8 77SR474
V_{CC} A_8 A_9
V_{CC} A_8 A_9
V_{CC} A_8 A_9
V_{CC} A_8 $\overline{PS}$
A_5 A_6 A_7 NC V_{CC} A_8 NC
4 3 2 1 28 27 26
A_4 5
A_3 6
A_2 7
A_1 8
A_0 9
NC 10
Q_0 11
28 PIN PKG
25 $\overline{G}$ $\overline{G}$ $\overline{G}$ A_{10} A_{10}
24 $\overline{INIT}$ $\overline{INITS}$ $\overline{INIT}$
23 $\overline{GS}$ $\overline{GS}$ $\overline{G}/\overline{GS}$ $\overline{G}/\overline{GS}$ $\overline{GS}$
22 C
21 NC
20 Q_7
19 Q_6
12 13 14 15 16 17 18
Q_1 Q_2 GND NC Q_3 Q_4 Q_5

NC = NO CONNECTION

TL/D/9261-7

FIGURE 6. Bipolar Registered PROM Pinout

Programming Support

PROM devices may be programmed with hardware and software readily available in the market. Most programmer manufacturers will offer a PLCC adapter which will fit in existing equipment. For the availability of PLCC adapter please check with your programmer manufacturer.

Programming Equipment

1. Data I/O
2. Structured Design
3. Stag
4. Dig Elec
5. Kontron
6. Prolog
7. Citel

Non-Registered PROM Programming Procedure

National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. To generate high (logical "1") levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed:

1. Programming should be attempted only at ambient temperatures between 15°C and 30°C.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more "active low" chip enable inputs.
   b) Increase V_{CC} from nominal to 10.5V (±0.5V) with a slew rate between 1.0 and 10.0 V/µs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0V.
   c) Select the output where a logical high is desired by raising that output voltage to 10.5V (±0.5V). Limit the slew rate from 1.0 to 10.0 V/µs. This voltage change may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum. (Remember that the outputs of the device are disabled at this time).
   d) Enable the device by taking the chip enable(s) to a low level. This is done with a pulse of 10 µs. The 10 µs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V (±0.2V) for one verification and to 6.0V (±0.2V) for a second verification. Verification at V_{CC} levels of 4.0V and 6.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.
   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled device is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

Programming Parameters Do not test or you may program the device

Symbol	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} during Programming	$V_{CC} = 11V$			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	$V_{OUT} = 11V$			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/µs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	µs
V_{CCV}	Required V_{CC} for Verification		5.8	6.0	6.2	V
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Non-Registered PROM

T_1 = 100 ns Min.

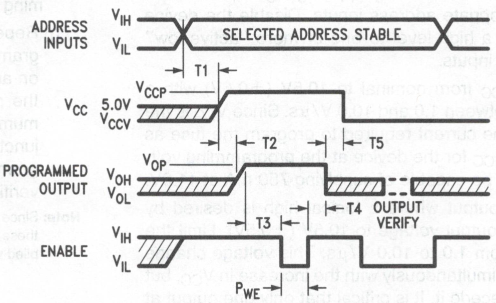
T_2 = 5 µs Min. T2 may be > 0 if V_{CCP} rises at the same rate or faster than (V_{OP})

T_3 = 100 ns Min.

T_4 = 100 ns Min.

T_5 = 100 ns Min.

P_{WE} is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has been programmed.


ADDRESS INPUTS
V_{IH}
V_{IL}
SELECTED ADDRESS STABLE
T1
V_{CCP}
V_{CC}
5.0V
V_{CCV}
T2
T5
V_{OP}
PROGRAMMED OUTPUT
V_{OH}
V_{OL}
T4
OUTPUT VERIFY
T3
ENABLE
V_{IH}
V_{IL}
P_{WE}

NOTE: ENABLE WAVEFORM FOR AN ACTIVE LOW ENABLE.
SOME PROMS HAVE MORE THAN ONE CHIP ENABLE.
HOLD ALL OTHER ENABLE(S) TO ACTIVE STATE(S).

TL/00/2506-1

Registered PROM Programming Procedure

National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. To generate high (logical "1") levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed:

1. Programming should be attempted only at ambient temperatures between 15°C and 30°C.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to asynchronous chip Enable input $\overline{G}$. $\overline{GS}$ is held low during the entire programming time.

   b) Increase V_{CC} from nominal to 10.5V ($\pm$0.5V) with a slew rate between 1.0 and 10.0 V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11V.

   c) Select the output where a logical high is desired by raising that output voltage to 10.5V ($\pm$0.5V). Limit the slew rate from 1.0 to 10.0 V/μs. This voltage change may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum. (Remember that the outputs of the device are disabled at this time).

   d) Enable the device by taking the chip enable ($\overline{G}$) to a low level. This is done with a pulse of 10 μs. The 10 μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.

   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V ($\pm$0.2V) for one verification and to 6.0V ($\pm$0.2V) for a second verification. Verification at V_{CC} levels of 4.0V and 6.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. Each data verification must be preceded by a positive going (low to high) clock edge to load the data from the array into the output register. The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.

   f) The initialize word is programmed by setting $\overline{INIT}$ input to a logic low and programming the initialize word output by output in the same manner as any other address. This can be accomplished by inverting the highest order address input from the PROM programmer and applying it to the $\overline{INIT}$ input.

   g) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.

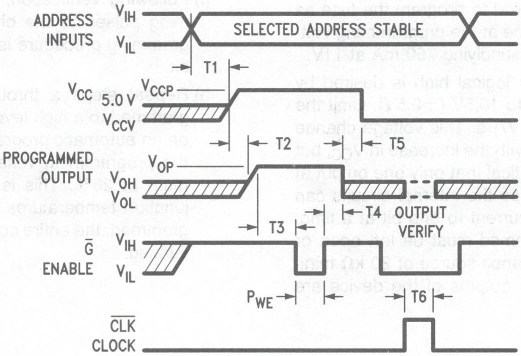
   h) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Programming Parameters Do not test or you may program the device

Symbol	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} during Programming	$V_{CC} = 11V$			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	$V_{OUT} = 11V$			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/µs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	µs
V_{CCVH}	Required High V_{CC} for Verification		5.8	6.0	6.2	V
V_{CCVL}	Required Low V_{CC} for Verification*		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

*See DM87SR191/193 and DM77SR191/193 for correct voltage.

Programming Waveforms Registered PROM


ADDRESS INPUTS
V_{IH}
V_{IL}
SELECTED ADDRESS STABLE
T1
V_{CC}
5.0 V
V_{CCP}
V_{CCV}
T2
T5
PROGRAMMED OUTPUT
V_{OP}
V_{OH}
V_{OL}
T3
T4
OUTPUT VERIFY
$\overline{G}$ ENABLE
V_{IH}
V_{IL}
P_{WE}
T6
$\overline{CLK}$ CLOCK

TL/00/2506-2

T_1 = 100 ns Min.

T_2 = 5 µs Min. (T2 may be > 0 if V_{CCP} rises at the same rate or faster than V_{OP}.)

T_3 = 100 ns Min.

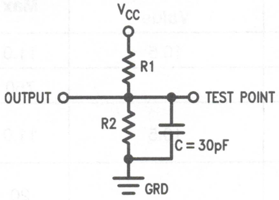
T_4 = 100 ns Min.

T_5 = 100 ns Min.

T_6 = 50 ns Min.

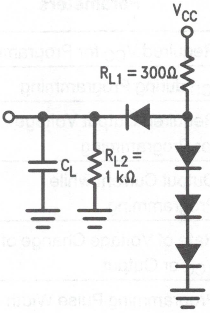
Standard Test Loads

Non-Registered PROMs


V_{CC}
R1
OUTPUT
TEST POINT
R2
C = 30pF
GRD

TL/00/2506-3

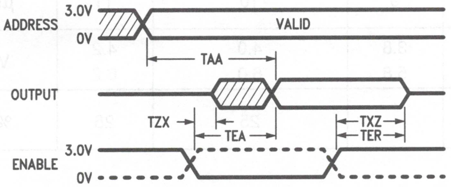
Registered PROMs


V_{CC}
$R_{L1} = 300\Omega$
C_L
$R_{L2} = 1\ k\Omega$

TL/00/2506-8

Switching Time Waveforms

Non-Registered PROM


ADDRESS
3.0V
0V
VALID
TAA
OUTPUT
TZX
TEA
TXZ
TER
ENABLE
3.0V
0V

TL/00/2506-4

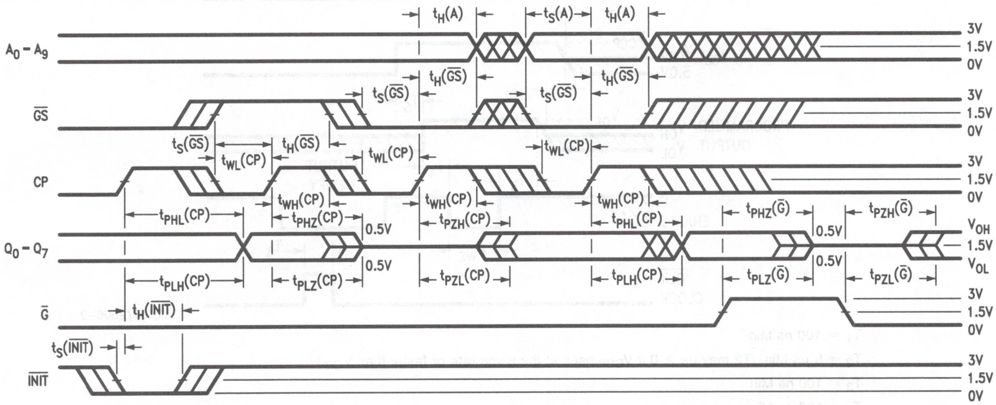
*Device input waveform characteristics are;
Repetition rate = 1 MHz
Source impedance = 50Ω
Rise and Fall times = 2.5 ns max.
(1.0 to 2.0 volt levels)

*TAA is measured with stable enable inputs.

*TEA and TER are measured from the 1.5 volt level on inputs and outputs with all address and enable inputs stable at applicable levels.

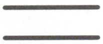
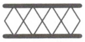
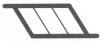
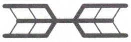
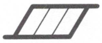
*For I_{OL} = 16 mA, R1 = 300Ω and R2 = 600Ω.
*for I_{OL} = 12 mA, R1 = 400Ω and R2 = 800Ω.
*"C" includes scope and jig capacitance.

Switching Waveforms Registered PROM


$A_0 - A_9$
$\overline{GS}$
CP
$Q_0 - Q_7$
$\overline{G}$
$\overline{INIT}$
$t_H(A)$
$t_S(A)$
$t_H(A)$
$t_S(\overline{GS})$
$t_H(\overline{GS})$
$t_S(\overline{GS})$
$t_H(\overline{GS})$
$t_S(\overline{GS})$
$t_H(\overline{GS})$
$t_{WL}(CP)$
$t_{WL}(CP)$
$t_{WL}(CP)$
$t_{WH}(CP)$
$t_{WH}(CP)$
$t_{WH}(CP)$
$t_{PHL}(CP)$
$t_{PHZ}(CP)$
$t_{PZH}(CP)$
$t_{PHL}(CP)$
$t_{PHZ}(\overline{G})$
$t_{PZH}(\overline{G})$
0.5V
0.5V
0.5V
0.5V
$t_{PLH}(CP)$
$t_{PLZ}(CP)$
$t_{PZL}(CP)$
$t_{PLH}(CP)$
$t_{PLZ}(\overline{G})$
$t_{PZL}(\overline{G})$
$t_H(\overline{INIT})$
$t_S(\overline{INIT})$
3V
1.5V
0V
V_{OH}
1.5V
V_{OL}

TL/00/2506-5

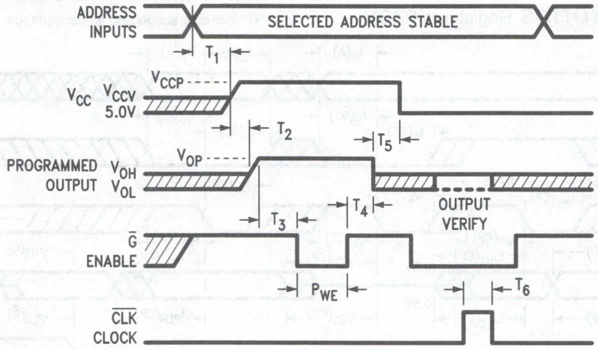
Key To Timing Diagram

Waveform	Inputs	Outputs	Waveform	Inputs	Outputs
	Must Be Steady	Will Be Steady		Don't Care: Any Change Permitted	Changing: State Unknown
	May Change from H to L	Will Be Changing from H to L		Does Not Apply	Center Line Is High Impedance "OFF" State
	May Change from L to H	Will Be Changing from L to H			

Programming Parameters Do not test or you may program the device

Symbol	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} during Programming	$V_{CC} = 11V$			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	$V_{OUT} = 11V$			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8 5.8	4.0 6.0	4.2 6.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Registered PROM


ADDRESS INPUTS
SELECTED ADDRESS STABLE
T_1
V_{CCP}
V_{CC}
V_{CCV}
5.0V
T_2
T_5
V_{OP}
PROGRAMMED OUTPUT
V_{OH}
V_{OL}
T_4
OUTPUT VERIFY
T_3
$\overline{G}$ ENABLE
P_{WE}
T_6
$\overline{CLK}$ CLOCK

TL/00/2506-9

T_1 = 100 ns Min.

T_2 = 5 μs Min. (T2 may be > 0 if V_{CCP} rises at the same rate or faster than V_{OP}.)

T_3 = 100 ns Min.

T_4 = 100 ns Min.

T_5 = 100 ns Min.

T_6 = 50 ns Min.

Approved Programmers for NSC PROMs

Manufacturer	**System #**
DATA I/O	5/17/19/29A
PRO-LOG	M910,M980
KONTRON	MPP80S
STAG	PPX
AIM	RP400
DIGELEC	UP803
STARPLEX™	

Quality Enhancement Programs For Bipolar Memory

A+ PROGRAM*			B+ PROGRAM		
Test	**Condition**	**Guaranteed LOT AQL 5**	**Test**	**Condition**	**Guaranteed LOT AQL 5**
D.C Parametric and Functionality	25°C	0.05	D.C Parametric and Functionality	25°C	0.05
	Each Temperature Extreme	0.05		Each Temperature Extreme	0.05
A.C. Parametric	25°C	0.4	A.C Parametric	25°C	0.4
Mechanical	Critical	0.01	Mechanical	Critical	0.01
	Major	0.28		Major	0.28
Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4	Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4
	Gross	0.4		Gross	0.4

*Includes 160 hours of burn-in at 125°C.

Section 4

ECL I/O Static RAMs

4

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BICMOS SRAMS (ECL I/O)

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National
Semiconductor

BiCMOS ECL I/O SRAM Selection Guide

Part Number	Organization	I/O Level	V_{EE}	Access (ns)	Pins	Temperature Range
NM5100	256k x 1	100K	−5.2V ±5%	15	24	0°C to +85°C
NM100500	256k x 1	100K	−4.2V to −4.8V	15	24	0°C to +85°C
NM5104	64k x 4	100K	−5.2V ±5%	12, 15	28	0°C to +85°C
NM100504	64k x 4	100K	−4.2V to −4.8V	15	28	0°C to +85°C
NM100494	16k x 4	10K	−4.2V to −4.8V	15, 18	28	0°C to +85°C
NM10494	16k x 4	100K	−5.2V ±5%	10, 12, 15	28	0°C to +75°C
NM100492	2k x 9	100K	−4.2V to −4.8V	7, 10	64	0°C to +75°C
NM4492	2k x 9	100K	−5.2V ±5%	5, 7, 10	64	0°C to +75°C

BiCMOS ECL I/O UV EPROM Selection Guide

Part Number	Organization	I/O Level	V_{EE}	Access (ns)	Pins	Temperature Range
NM10E149	256 x 4	10K	−5.2V ±5%	5, 7, 10	16	0°C to +75°C
NM100E149	256 x 4	100K	−4.2V to −4.8V	5, 7, 10	16	0°C to +75°C

National Semiconductor

NM5100/NM100500 ECL I/O 256k BiCMOS SRAM 262,144 x 1 Bit

General Description

The NM5100 and NM100500 are a 262,144-bit fully static, asynchronous, random access memories organized as 262,144 words by 1 bit. The devices are based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

The NM5100 operates with a supply voltage of −5.2V ±5%, yet the input and output voltage levels are temperature compensated 100k ECL compatible. The NM100500 operates with a −4.2V to −4.8V supply voltage.

Reading the memory is accomplished by pulling the chip select ($\overline{S}$) pin LOW while the write enable ($\overline{W}$) pin remains HIGH allowing the memory contents to be displayed on the output pin (Q). The output pin will remain inactive (LOW) if either the chip select ($\overline{S}$) pin is HIGH or the write enable ($\overline{W}$) pin is LOW.

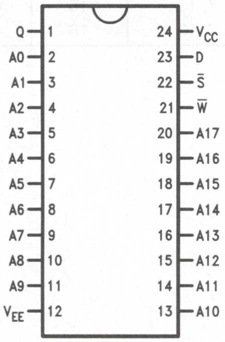
Writing to the device is accomplished by having the chip select ($\overline{S}$) and the write enable ($\overline{W}$) pins LOW. Data on the input pin will then be written into the memory address specified on the address pins (A0–A17).

Features

- 15 ns/18 ns speed grades over the commercial temperature range
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- Temperature compensated F100k ECL I/O
- Power supply −5.2V ±5% (NM5100)
- Power supply −4.2V to −4.8V (NM100500)
- Low power dissipation <1.1W
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 24-pin flatpack

Connection Diagrams

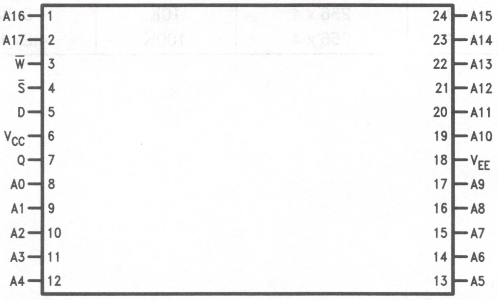
400 Mil Ceramic DIP



TL/D/9451–1

Top View

365 x 535 Ceramic Flatpack (30 Mil Lead Pitch)



TL/D/9451–2

Top View

Pin Names

A0–A17	Address Inputs
$\overline{S}$	Chip Select
$\overline{W}$	Write Enable
Q	Data Out
D	Data In
V_{CC}	Ground
V_{EE}	Power

Absolute Maximum Ratings

Above which useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Static Discharge Voltage (Per MIL-STD 883)	>2001V
Maximum Junction Temperature (T_J)	+150°C
Output Current (DC Output HIGH)	−50 mA
Latch-Up Current	>200 mA

These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Test Conditions

Input Pulse Levels	*Figure 1*
Input Rise and Fall Times	0.7 ns
Output Timing Referrence Levels	50% of Input
AC Test Circuit	*Figure 2*

Capacitance Tested by Sample Basis

Symbol	Parameter	Max	Units
C_{IN}	Input Pin Capacitance	5.0	pF
C_{OUT}	Output Pin Capacitance	8.0	pF

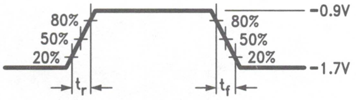
Operating Voltage

Device	Voltage
NM5100	$V_{EE} = -5.2V \pm 5\%$
NM100500	$V_{EE} = -4.2V$ to $-4.8V$

DC Electrical Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$, Loading with 50Ω to −2.0V	−1025	−880	mV
V_{OL}	Output LOW Voltage		−1810	−1620	mV
V_{OHC}	Output HIGH Voltage	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$, Loading with 50Ω to −2.0V	−1025		mV
V_{OLC}	Output LOW Voltage			−1620	mV
V_{IH}	Input HIGH Voltage		−1165	−880	mV
V_{IL}	Input LOW Voltage		−1810	−1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH(Min)}$		220	μA
I_{IL}	Input LOW Current	$V_{IN} = V_{IL(Max)}$	−50	170	μA
I_{EE}	Power Supply Current	f_o = 50 MHz	−200		mA

All voltages are referenced to V_{CC} pin = 0V.



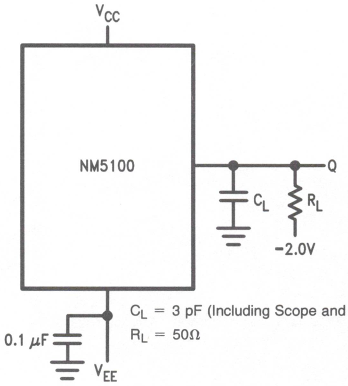
TL/D/9451–3

t_R = Rise Time

t_F = Fall Time

50% = Timing Reference Levels

FIGURE 1. Input Levels



C_L = 3 pF (Including Scope and Jig)

R_L = 50Ω

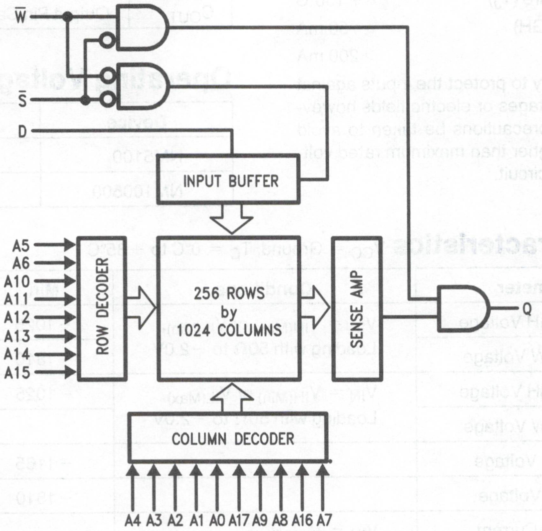
TL/D/9451–4

FIGURE 2. AC Test Circuit

Truth Table

$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Q	Read

Logic Diagram


$\overline{W}$
$\overline{S}$
D
INPUT BUFFER
A5
A6
A10
A11
A12
A13
A14
A15
ROW DECODER
256 ROWS by 1024 COLUMNS
SENSE AMP
Q
COLUMN DECODER
A4 A3 A2 A1 A0 A17 A9 A8 A16 A7

TL/D/9451-5

Note: A5 = MSB
A4 = MSB

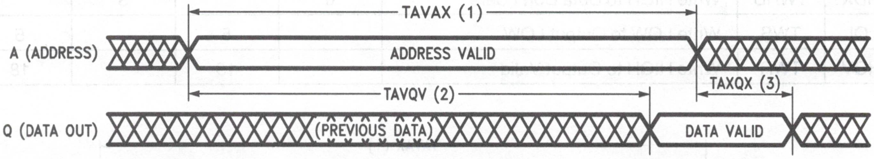
Read Cycles

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	
1	TAVAX	TRC	Address Valid to Address Invalid	15		18		ns
2	TAVQV	TAA	Address Valid to Output Valid		15		18	ns
3	TAXQX	TOH	Address Invalid to Output Invalid	3		3		ns
4	TSLSH	TRC	Chip Select LOW to Chip Select HIGH	7		7		ns
5	TSLQV	TACS	Chip Select LOW to Output Valid		5		5	ns
6	TSHQL	TRCS	Chip Select HIGH to Output LOW		4		4	ns

Read Cycle 1

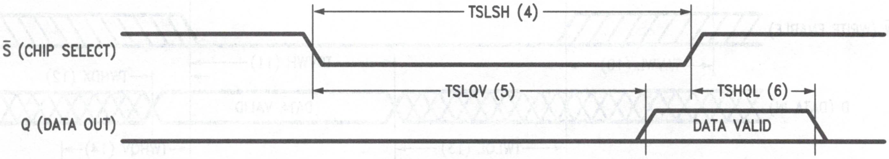
Where $\overline{S}$ is active prior to or within TAVQV-TSLQV after address valid.


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TAVQV (2)
TAXQX (3)
Q (DATA OUT)
(PREVIOUS DATA)
DATA VALID

TL/D/9451-6

Read Cycle 2

Where address is valid a minimum of TAVQV-TSLQV prior to $\overline{S}$ becoming active.


TSLSH (4)
$\overline{S}$ (CHIP SELECT)
TSLQV (5)
TSHQL (6)
Q (DATA OUT)
DATA VALID

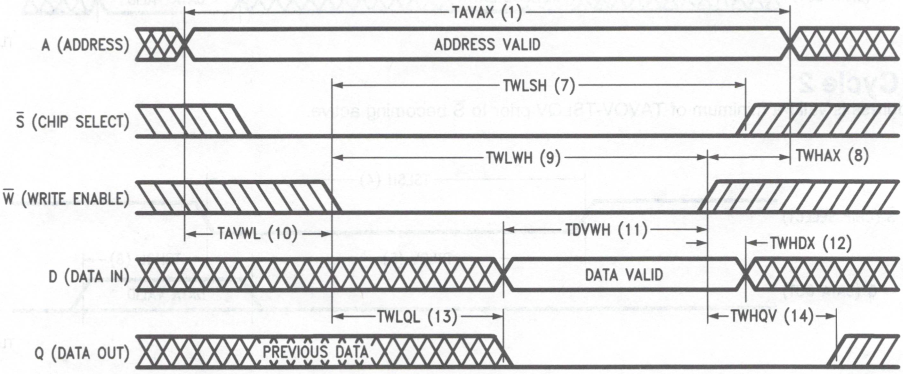
TL/D/9451-7

Write Cycle 1

This write cycle is $\overline{W}$ controlled, where $\overline{S}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data out (Q) may become active and requires observance of TWLQL to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{S}$ becoming inactive (HIGH).

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	
1	TAVAX	TWC	Address Valid to Address Invalid	15		18		ns
7	TWLSH		Write Enable LOW to Chip Select HIGH	10		12		ns
8	TWHAX	TWHA	Write HIGH to Address Don't Care	0		3		ns
9	TWLWH	TW	Write LOW to Write HIGH	10		12		ns
10	TAVWL	TWSA	Address Valid to Write LOW	0		2		ns
11	TDVWH		Data Valid to Write HIGH	10		14		ns
12	TWHDX	TWHD	Write HIGH to Data Don't Care	0		3		ns
13	TWLQL	TWS	Write LOW to Output LOW		5		5	ns
14	TWHQV	TWR	Write HIGH to Output Valid		15		18	ns


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TWLSH (7)
S̄ (CHIP SELECT)
TWLWH (9)
TWHAX (8)
W̄ (WRITE ENABLE)
TAVWL (10)
TDVWH (11)
TWHDX (12)
D (DATA IN)
DATA VALID
TWLQL (13)
TWHQV (14)
Q (DATA OUT)
PREVIOUS DATA

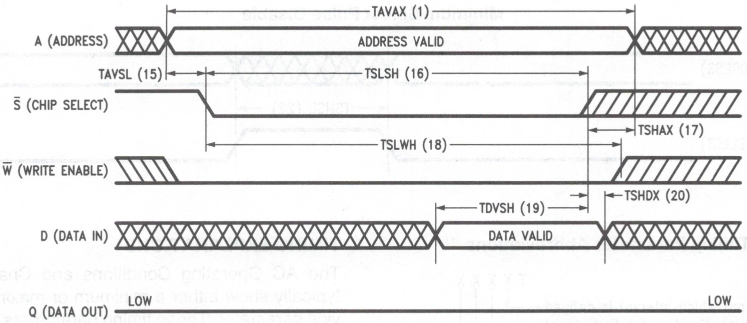
TL/D/9451-8

Write Cycle 2

This write cycle is $\overline{\text{S}}$ controlled, where $\overline{\text{W}}$ is active prior to, or coincident with, $\overline{\text{S}}$ becoming active (LOW). Write cycle 2 has identical specifications to write cycle 1 with the exceptions of $\overline{\text{W}}$ and $\overline{\text{S}}$ being interchanged. This write cycle may be more convenient for common I/O applications because data bus restrictions are alleviated.

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	
15	TAVSL	TWSA	Address Valid to Chip Select LOW	0		2		ns
16	TSLSH		Chip Select LOW to Chip Select HIGH	10		12		ns
17	TSHAX	TWHA	Chip Select HIGH to Address Don't Care	0		3		ns
18	TSLWH		Chip Select LOW to Write Enable HIGH	10		12		ns
19	TDVSH		Data Valid to Chip Select HIGH	10		14		ns
20	TSHDX	TWHD	Chip Select HIGH to Data Don't Care	0		3		ns


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TAVSL (15)
TSLSH (16)
S̄ (CHIP SELECT)
TSHAX (17)
TSLWH (18)
W̄ (WRITE ENABLE)
TSHDX (20)
TDVSH (19)
D (DATA IN)
DATA VALID
LOW
Q (DATA OUT)
LOW

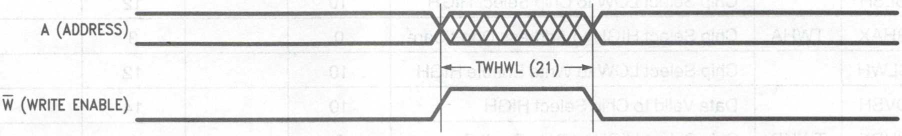
TL/D/9451-9

Consecutive Write Cycles

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

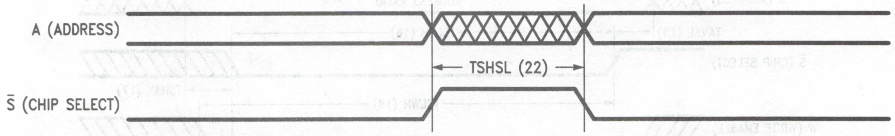
No.	Symbol		Parameter	15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	
21	TWHWL	/TWP	Write Enable HIGH to Write Enable LOW	4		4		ns
22	TSHSL	/TSP	Chip Select HIGH to Chip Select LOW	4		4		ns

Minimum Write Pulse Disable


A (ADDRESS)
TWHWL (21)
W̄ (WRITE ENABLE)

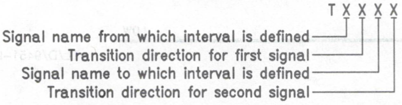
TL/D/9451-10

Minimum Select Pulse Disable


A (ADDRESS)
TSHSL (22)
S̄ (CHIP SELECT)

TL/D/9451-11

Standard Timing Parameter Abbreviations


T X X X X
Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

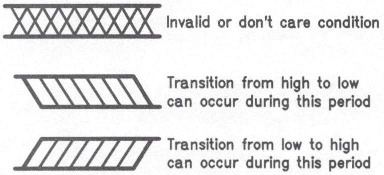
TL/D/9451-12

The transition definitions used in this data sheet are.

H = Transition to HIGH State
L = Transition to LOW State
V = Transition to Valid State
X = Transition to Invalid or Don't Care Condition

TIMING EXPLANATIONS

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for a device parameter. Those timing parameters which show a minimum value do so because the system must supply at least that much time, even though most devices do not need the full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory devices (i.e., access times) are specified as a maximum time because the device will never provide the data later than this stated value, and usually, much sooner.


Invalid or don't care condition
Transition from high to low can occur during this period
Transition from low to high can occur during this period

TL/D/9451-13

Ordering Information

Part Number	Temperature Range	Package Type	Ordering Code
NM5100	0°C to +85°C	24 Pin Ceramic DIP	NM5100D15/18
NM5100	0°C to +85°C	24 Pin Flatpack	NM5100F15/18
NM100500	0°C to +85°C	24 Pin Ceramic DIP	NM100500D15/18
NM100500	0°C to +85°C	24 Pin Flatpack	NM100500F15/18

National Semiconductor

NM100504/NM5104 256k BiCMOS SRAM 64k x 4

General Description

The NM5104 and NM100504 are 262,144-bit fully static, asynchronous, random access memories organized as 65,536 words by 4 bits. The devices are based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

The NM5104 operates with a supply voltage of −5.2V ±5%, yet the input and output voltage levels are temperature compensated 100K ECL compatible. The NM100504 operates with a −4.2V to −4.8V supply voltage.

Reading the memory is accomplished by pulling the chip select ($\overline{\text{S}}$) pin LOW while the write enable ($\overline{\text{W}}$) pin remains HIGH allowing the memory contents to be displayed on the output pins (Q0–Q3). The output pins will remain inactive (LOW) if either the chip select ($\overline{\text{S}}$) pin is HIGH or the write enable ($\overline{\text{W}}$) pin is LOW.

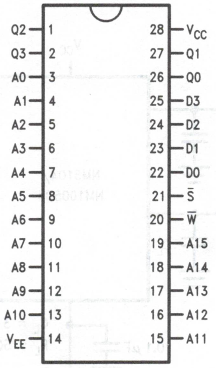
Writing to the device is accomplished by having the chip select ($\overline{\text{S}}$) and the write enable ($\overline{\text{W}}$) pins LOW. Data on the input pins will then be written into the memory address specified on the address pins (A0–A15).

Features

- Speed Grades: 12 ns/15 ns (NM5104)
- Speed Grades: 15 ns/18 ns (NM100504)
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- Temperature compensated F100K ECL I/O
- Power supply −5.2V to ±5% (NM5104)
- Power supply −4.2V to −4.8V (NM100504)
- Low power dissipation <1.4W @ 50 MHz
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 28-pin flatpak and 28-pin ceramic DIP

Connection Diagrams

28-Pin Ceramic DIP


Q2 1
Q3 2
A0 3
A1 4
A2 5
A3 6
A4 7
A5 8
A6 9
A7 10
A8 11
A9 12
A10 13
VEE 14
28 VCC
27 Q1
26 Q0
25 D3
24 D2
23 D1
22 D0
21 S̄
20 W̄
19 A15
18 A14
17 A13
16 A12
15 A11

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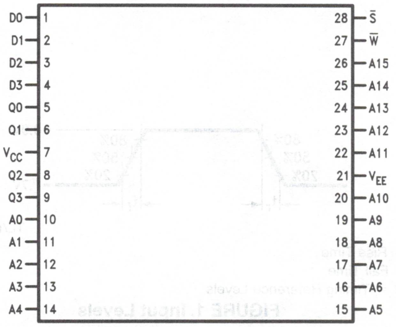
Top View

28-Pin Ceramic Flatpak
(30 Mil Lead Pitch)


D0 1
D1 2
D2 3
D3 4
Q0 5
Q1 6
VCC 7
Q2 8
Q3 9
A0 10
A1 11
A2 12
A3 13
A4 14
28 S̄
27 W̄
26 A15
25 A14
24 A13
23 A12
22 A11
21 VEE
20 A10
19 A9
18 A8
17 A7
16 A6
15 A5

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Top View

Pin Names

A0–A15	Address Inputs
$\overline{\text{S}}$	Chip Select
$\overline{\text{W}}$	Write Enable
Q0–Q3	Data Out
D0–D3	Data In
V_{CC}	Ground
V_{EE}	Power

Absolute Maximum Ratings

above which useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Static Discharge Voltage (Per MIL-STD 883)	>2001V
Maximum Junction Temperature (T_J)	+150°C
Output Current (DC Output HIGH)	−50 mA
Latch-Up Current	>200 mA

These devices contain circuitry to protect the inputs against damage to due to high static voltages or electric fields however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Test Conditions

Input Pulse Levels	*Figure 1*
Input Rise and Fall times	0.7 ns
Output Timing Reference Levels	50% of Input
AC Test Circuit	*Figure 2*

Capacitance Tested by Sample Basis

Symbol	Parameter	Max	Units
C_{IN}	Input Pin Capacitance	5.0	pF
C_{OUT}	Output Pin Capacitance	8.0	pF

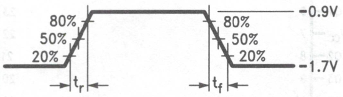
Operating Voltage

Device	Voltage
NM5104	$V_{EE} = -5.2V \pm 5\%$
NM100504	$V_{EE} = -4.2V$ to $-4.8V$

DC Electrical Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output HIGH Voltage	Loading with 50Ω to −2.0V	−1025	−880	mV
V_{OL}	Output LOW Voltage		−1810	−1620	mV
V_{IH}	Input HIGH Voltage		−1165	−880	mV
V_{IL}	Input LOW Voltage		−1810	−1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH(Min)}$		50	µA
I_{IL}	Input LOW Current	$V_{IN} = V_{IL(Max)}$	−50	50	µA
I_{EE}	Power Supply Current	f_o = 50 MHz	−250		mA

All voltages are referenced to V_{CC} pin = 0V.



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t_R = Rise Time
t_F = Fall Time
50% = Timing Reference Levels

FIGURE 1. Input Levels

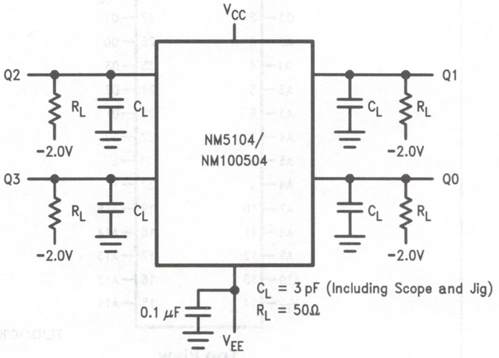

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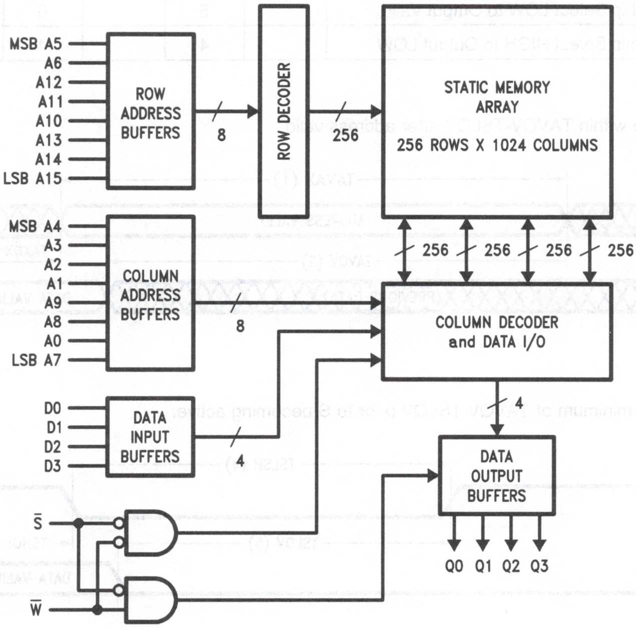
FIGURE 2. AC Test Circuit

Truth Table

$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Q	Read

Logic Diagram


MSB A5
A6
A12
A11
A10
A13
A14
LSB A15
ROW ADDRESS BUFFERS
8
ROW DECODER
256
STATIC MEMORY ARRAY
256 ROWS X 1024 COLUMNS
256
256
256
256
MSB A4
A3
A2
A1
A9
A8
A0
LSB A7
COLUMN ADDRESS BUFFERS
8
COLUMN DECODER and DATA I/O
4
D0
D1
D2
D3
DATA INPUT BUFFERS
4
DATA OUTPUT BUFFERS
Q0 Q1 Q2 Q3
$\overline{S}$
$\overline{W}$

TL/D/10390-5

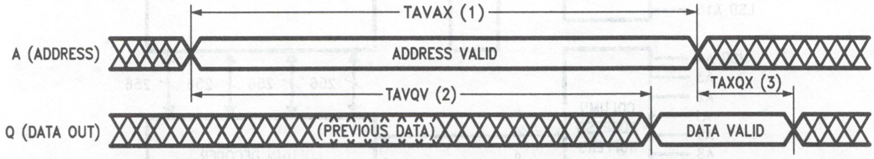
Read Cycles

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	12 ns Device		15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	Min	Max	
1	TAVAX	TRC	Address Valid to Address Invalid	12		15		18		ns
2	TAVQV	TAA	Address Valid to Output Valid		12		15		18	ns
3	TAXQX	TOH	Address Invalid to Output Invalid	3		3		3		ns
4	TSLSH	TRC	Chip Select LOW to Chip Select HIGH	7		7		7		ns
5	TSLQV	TACS	Chip Select LOW to Output Valid		5		5		5	ns
6	TSHQL	TRCS	Chip Select HIGH to Output LOW		4		4		4	ns

Read Cycle 1

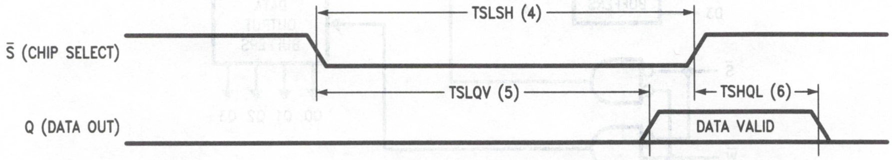
Where $\overline{S}$ is active prior to within TAVQV-TSLQV after address valid.


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TAXQX (3)
TAVQV (2)
Q (DATA OUT)
(PREVIOUS DATA)
DATA VALID

TL/D/10390-6

Read Cycle 2

Where address is valid a minimum of TAVQV-TSLQV prior to $\overline{S}$ becoming active.


TSLSH (4)
$\overline{S}$ (CHIP SELECT)
TSLQV (5)
TSHQL (6)
Q (DATA OUT)
DATA VALID

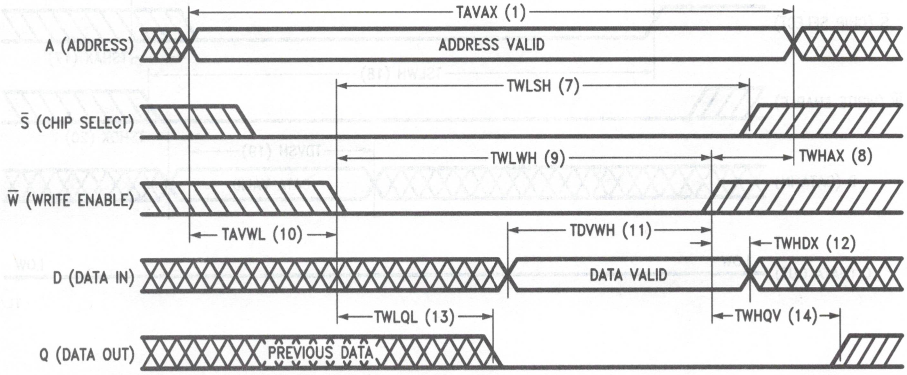
TL/D/10390-7

Write Cycle 1

This write cycle is $\overline{W}$ controlled, where $\overline{S}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data out (Q) may become active and requires observance of TWLQL to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{S}$ becoming inactive (HIGH).

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	12 ns Device		15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	Min	Max	
1	TAVAX	TWC	Address Valid to Address Invalid	12		15		18		ns
7	TWLSH		Write Enable LOW to Chip Select HIGH	9		10		12		ns
8	TWHAX	TWHA	Write HIGH to Address Don't Care	0		0		3		ns
9	TWLWH	TW	Write LOW to Write HIGH	9		10		12		ns
10	TAVWL	TWSA	Address Valid to Write LOW	0		0		2		ns
11	TDVWH		Data Valid to Write HIGH	9		10		14		ns
12	TWHDX	TWHD	Write HIGH to Data Don't Care	0		0		3		ns
13	TWLQL	TWS	Write LOW to Output LOW		5		5		5	ns
14	TWHQV	TWR	Write HIGH to Output Valid		12		15		18	ns


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TWLSH (7)
S̅ (CHIP SELECT)
TWLWH (9)
TWHAX (8)
W̅ (WRITE ENABLE)
TAVWL (10)
TDVWH (11)
TWHDX (12)
D (DATA IN)
DATA VALID
TWLQL (13)
TWHQV (14)
Q (DATA OUT)
PREVIOUS DATA

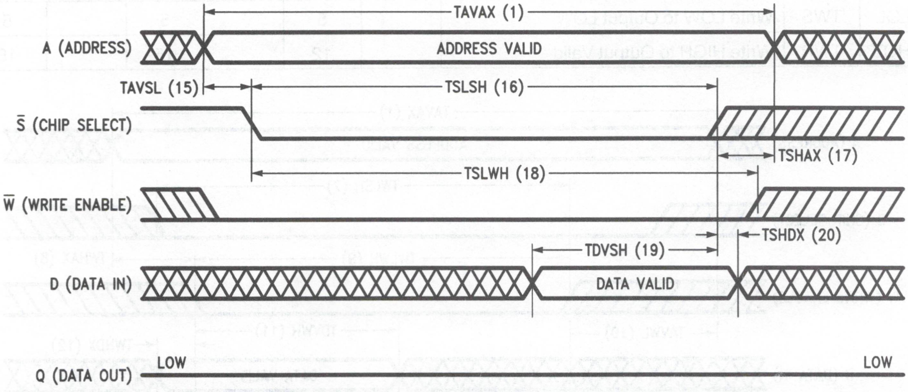
TL/D/10390–8

Write Cycle 2

This write cycle is $\overline{S}$ controlled, where $\overline{W}$ is active prior to, or coincident with, $\overline{S}$ becoming active (LOW). Write cycle 2 has indentical specifications to write cycle 1 with the exceptions of $\overline{W}$ and $\overline{S}$ being interchanged. This write cycle may be more convenient for common I/O applications because data bus restrictions are alleviated.

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	12 ns Device		15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	Min	Max	
15	TAVSL	TWSA	Address Valid to Chip Select LOW	0		0		2		ns
16	TSLSH		Chip Select LOW to Chip Select HIGH	9		10		12		ns
17	TSHAX	TWHA	Chip Select HIGH to Address Don't Care	0		0		3		ns
18	TSLWH		Chip Select LOW to Write Enable HIGH	9		10		12		ns
19	TDVSH		Data Valid to Chip Select HIGH	9		10		14		ns
20	TSHDX	TWHD	Chip Select HIGH to Data Don't Care	0		0		3		ns


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TAVSL (15)
TSLSH (16)
$\overline{S}$ (CHIP SELECT)
TSHAX (17)
TSLWH (18)
$\overline{W}$ (WRITE ENABLE)
TSHDX (20)
TDVSH (19)
D (DATA IN)
DATA VALID
LOW
LOW
Q (DATA OUT)

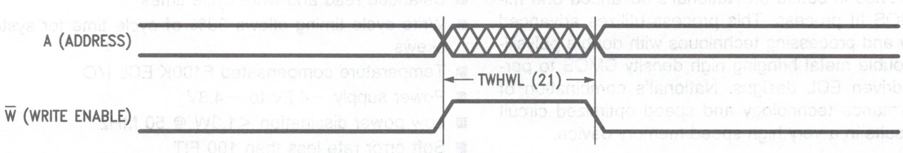
TL/D/10390–9

Consecutive Write Cycles

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

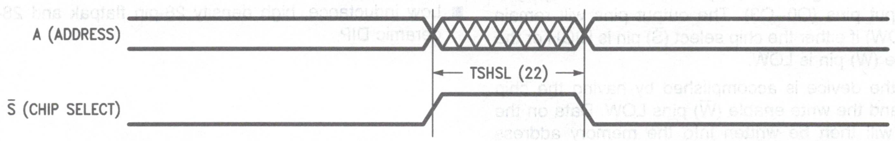
No.	Symbol		Parameter	12 ns Device		15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	Min	Max	
21	TWHWL	$\overline{\text{TWP}}$	Write Enable HIGH to Write Enable LOW	3		4		4		ns
22	TSHSL	$\overline{\text{TSP}}$	Chip Select HIGH to Chip Select LOW	3		4		4		ns

Minimum Write Pulse Disable


A (ADDRESS)
W̄ (WRITE ENABLE)
TWHWL (21)

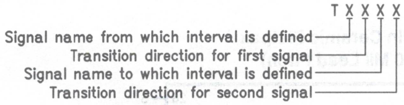
TL/D/10390-10

Minimum Select Pulse Disable


A (ADDRESS)
TSHSL (22)
S̄ (CHIP SELECT)

TL/D/10390-11

Standard Timing Parameter Abbreviations


T X X X X
Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

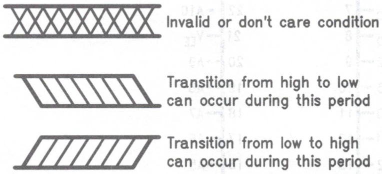
TL/D/10390-12

The transition definitions used in this data sheet are:

H = Transition to HIGH State
L = Transition to LOW State
V = Transition to Valid State
X = Transition to Invalid or Don't Care Condition

TIMING EXPLANATIONS

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for a device parameter. Those timing parameters which show a minimum value do so because the system must supply at least that much time, even though most devices do not need the full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory devices (i.e., access times) are specified as a maximum time because the device will never provide the data later than this stated value, and usually, much sooner.


Invalid or don't care condition
Transition from high to low can occur during this period
Transition from low to high can occur during this period

TL/D/10390-13

Ordering Information

Part Number	Temperature Range	Package Type	Ordering Code
NM5104	0°C to +85°C	28-Pin Ceramic DIP	NM5104D12/15
NM5104	0°C to +85°C	28-Pin Flatpak	NM5104F12/15
NM100504	0°C to +85°C	28-Pin Ceramic DIP	NM100504D15/18
NM100504	0°C to +85°C	28-Pin Flatpak	NM100504F15/18

National Semiconductor

NM100494 64k BiCMOS SRAM 16k x 4 Bit

General Description

The NM100494 is a 65,536-bit fully static, asynchronous, random access memory organized as 16,384 words by 4 bits. The device is based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

The NM100494 operates with a −4.2V to −4.8V supply voltage. Reading the memory is accomplished by pulling the chip select ($\overline{S}$) pin LOW while the write enable ($\overline{W}$) pin remains HIGH allowing the memory contents to be displayed on the output pins (Q0–Q3). The output pins will remain inactive (LOW) if either the chip select ($\overline{S}$) pin is HIGH or the write enable ($\overline{W}$) pin is LOW.

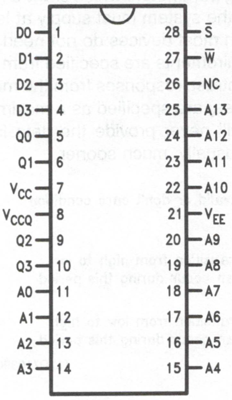
Writing to the device is accomplished by having the chip select ($\overline{S}$) and the write enable ($\overline{W}$) pins LOW. Data on the input pins will then be written into the memory address specified on the address pins (A0–A13).

Features

- 15 ns/18 ns speed grades over the commercial temperature range
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- Temperature compensated F100K ECL I/O
- Power supply −4.2V to −4.8V
- Low power dissipation <1.3W @ 50 MHz
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 28-pin flatpak and 28-pin ceramic DIP

Connection Diagrams

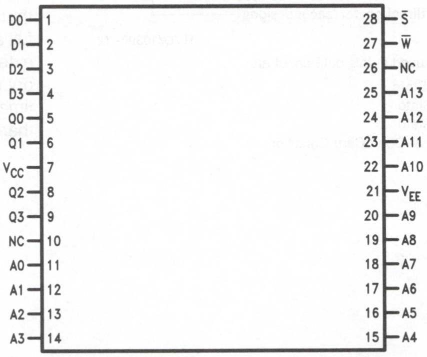
28-Pin Ceramic DIP


D0 1
D1 2
D2 3
D3 4
Q0 5
Q1 6
VCC 7
VCCQ 8
Q2 9
Q3 10
A0 11
A1 12
A2 13
A3 14
28 S̅
27 W̅
26 NC
25 A13
24 A12
23 A11
22 A10
21 VEE
20 A9
19 A8
18 A7
17 A6
16 A5
15 A4

TL/D/10391-2

Top View

28-Pin Ceramic Flatpak
(30 Mil Lead Pitch)


D0 1
D1 2
D2 3
D3 4
Q0 5
Q1 6
VCC 7
Q2 8
Q3 9
NC 10
A0 11
A1 12
A2 13
A3 14
28 S̅
27 W̅
26 NC
25 A13
24 A12
23 A11
22 A10
21 VEE
20 A9
19 A8
18 A7
17 A6
16 A5
15 A4

TL/D/10391-3

Top View

Pin Names

A0–A13	Address Inputs
$\overline{S}$	Chip Select
$\overline{W}$	Write Enable
Q0–Q3	Data Out
D0–D3	Data In
V_{CC}	Ground
V_{EE}	Power

Absolute Maximum Ratings

above which useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Static Discharge Voltage (Per MIL-STD 883)	>2001V
Maximum Junction Temperature (T_J)	+150°C
Output Current (DC Output HIGH)	−50 mA
Latch-Up Current	>200 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Test Conditions

Input Pulse Levels	*Figure 1*
Input Rise and Fall Times	0.7 ns
Output Timing Reference Levels	50% of Input
AC Test Circuit	*Figure 2*

Capacitance Tested by Sample Basis

Symbol	Parameter	Max	Units
C_{IN}	Input Pin Capacitance	5.0	pF
C_{OUT}	Output Pin Capacitance	8.0	pF

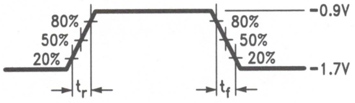
Operating Voltage

Device	Voltage
NM100494	V_{EE} = −4.2V to −4.8V

DC Electrical Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output HIGH Voltage	Loading with 50Ω to −2.0V	−1025	−880	mV
V_{OL}	Output LOW Voltage		−1810	−1620	mV
V_{IH}	Input HIGH Voltage		−1165	−880	mV
V_{IL}	Input LOW Voltage		−1810	−1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH(Min)}$		50	μA
I_{IL}	Input LOW Current	$V_{IN} = V_{IL(Max)}$	−50	50	μA
I_{EE}	Power Supply Current	f_o = 50 MHz	−240		mA

All voltages are referenced to V_{CC} pin = 0V.



TL/D/10391-4

t_R = Rise Time
t_F = Fall Time
50% = Timing Reference Levels

FIGURE 1. Input Levels

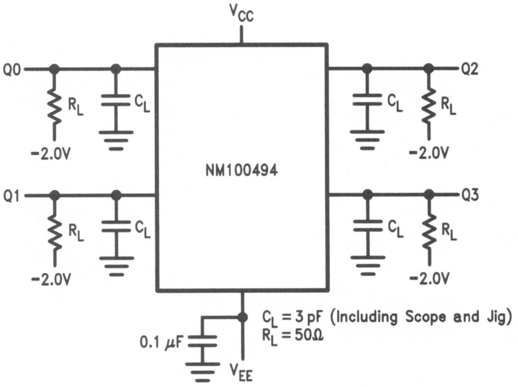


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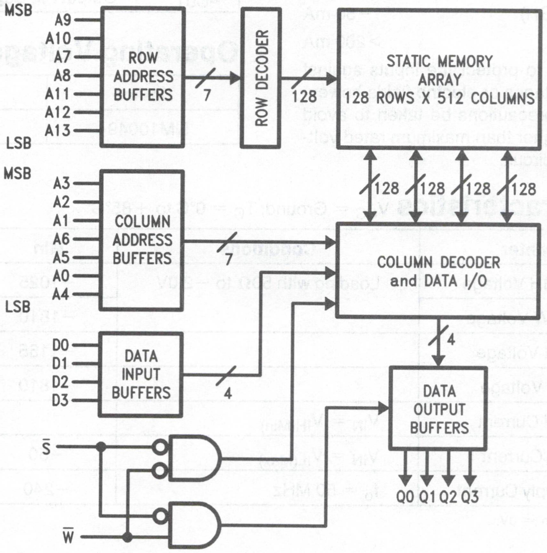
FIGURE 2. AC Test Circuit

Truth Table

$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Q	Read

Logic Diagram


MSB
A9
A10
A7
A8
A11
A12
A13
LSB
ROW ADDRESS BUFFERS
7
ROW DECODER
128
STATIC MEMORY ARRAY
128 ROWS X 512 COLUMNS
128
128
128
128
MSB
A3
A2
A1
A6
A5
A0
A4
LSB
COLUMN ADDRESS BUFFERS
7
COLUMN DECODER and DATA I/O
4
D0
D1
D2
D3
DATA INPUT BUFFERS
4
DATA OUTPUT BUFFERS
Q0 Q1 Q2 Q3
S̄
W̄

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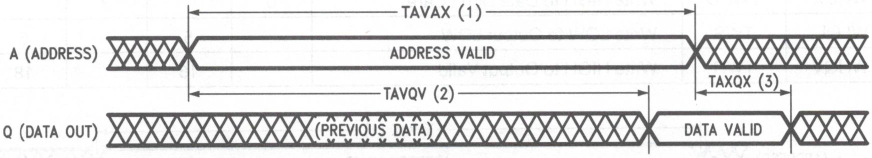
Read Cycles

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	
1	TAVAX	TRC	Address Valid to Address Invalid	15		18		ns
2	TAVQV	TAA	Address Valid to Output Valid		15		18	ns
3	TAXQX	TOH	Address Invalid to Output Invalid	3		3		ns
4	TSLSH	TRC	Chip Select LOW to Chip Select HIGH	7		7		ns
5	TSLQV	TACS	Chip Select LOW to Output Valid		5		5	ns
6	TSHQL	TRCS	Chip Select HIGH to Output LOW		4		4	ns

Read Cycle 1

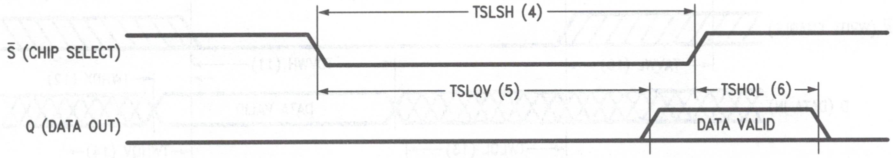
Where $\overline{S}$ is active prior to or within TAVQV-TSLQV after address valid.


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TAVQV (2)
TAXQX (3)
Q (DATA OUT)
(PREVIOUS DATA)
DATA VALID

TL/D/10391-7

Read Cycle 2

Where address is valid a minimum of TAVQV-TSLQV prior to $\overline{S}$ becoming active.


TSLSH (4)
$\overline{S}$ (CHIP SELECT)
TSLQV (5)
TSHQL (6)
Q (DATA OUT)
DATA VALID

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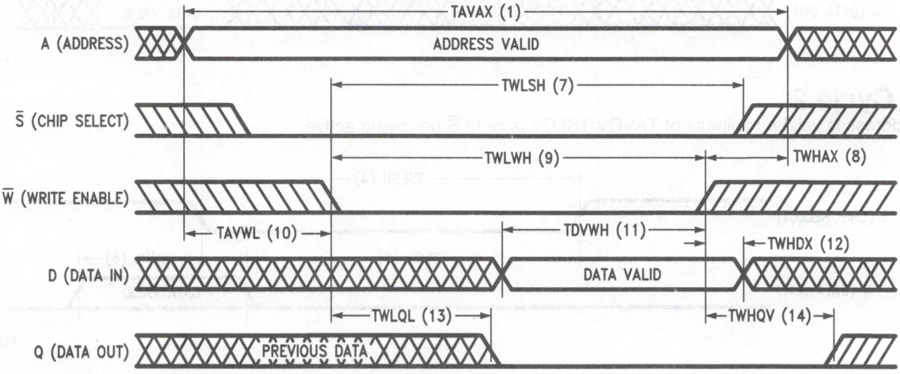
Write Cycle 1

This write cycle is $\overline{W}$ controlled, where $\overline{S}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data out (Q) may become active and requires observance of TWLQL to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{S}$ becoming inactive (HIGH).

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	
1	TAVAX	TWC	Address Valid to Address Invalid	15		18		ns
7	TWLSH		Write Enable LOW to Chip Select HIGH	10		12		ns
8	TWHAX	TWHA	Write HIGH to Address Don't Care	0		3		ns
9	TWLWH	TW	Write LOW to Write HIGH	10		12		ns
10	TAVWL	TWSA	Address Valid to Write LOW	0		2		ns
11	TDVWH		Data Valid to Write HIGH	10		14		ns
12	TWHDX	TWHD	Write HIGH to Data Don't Care	0		3		ns
13	TWLQL	TWS	Write LOW to Output LOW		5		5	ns
14	TWHQV	TWR	Write HIGH to Output Valid		15		18	ns


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TWLSH (7)
S̄ (CHIP SELECT)
TWLWH (9)
TWHAX (8)
W̄ (WRITE ENABLE)
TAVWL (10)
TDVWH (11)
TWHDX (12)
D (DATA IN)
DATA VALID
TWLQL (13)
TWHQV (14)
Q (DATA OUT)
PREVIOUS DATA

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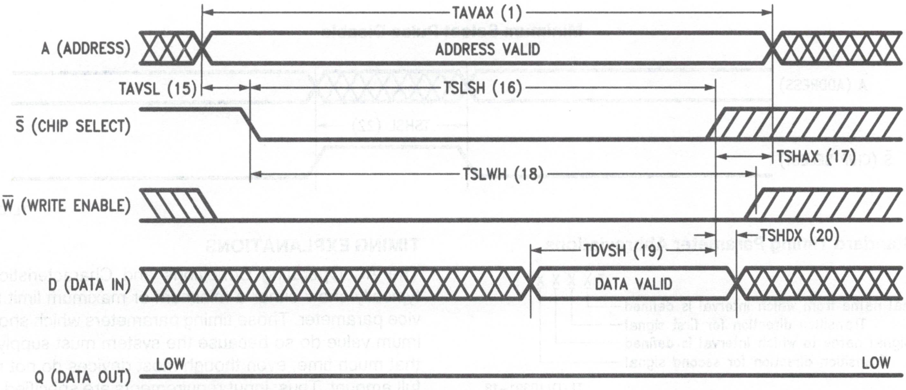
Write Cycle 2

This write cycle is $\overline{S}$ controlled, where $\overline{W}$ is active prior to, or coincident with, $\overline{S}$ becoming active (LOW). Write cycle 2 has indentical specifications to write cycle 1 with the exceptions of $\overline{W}$ and $\overline{S}$ being interchanged. This write cycle may be more convenient for common I/O applications because data bus restrictions are alleviated.

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	
15	TAVSL	TWSA	Address Valid to Chip Select LOW	0		2		ns
16	TSLSH		Chip Select LOW to Chip Select HIGH	10		12		ns
17	TSHAX	TWHA	Chip Select HIGH to Address Don't Care	0		3		ns
18	TSLWH		Chip Select LOW to Write Enable HIGH	10		12		ns
19	TDVSH		Data Valid to Chip Select HIGH	10		14		ns
20	TSHDX	TWHD	Chip Select HIGH to Data Don't Care	0		3		ns


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TAVSL (15)
TSLSH (16)
S̄ (CHIP SELECT)
TSHAX (17)
TSLWH (18)
W̄ (WRITE ENABLE)
TSHDX (20)
TDVSH (19)
D (DATA IN)
DATA VALID
LOW
Q (DATA OUT)
LOW

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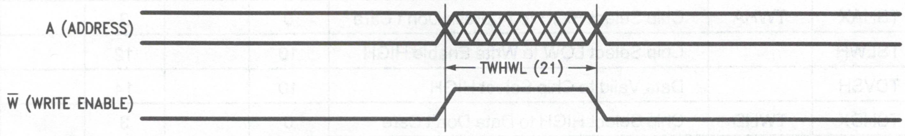
Consecutive Write Cycles

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	
21	TWHWL	$\overline{\text{TWP}}$	Write Enable HIGH to Write Enable LOW	4		4		ns
22	TSHSL	$\overline{\text{TSP}}$	Chip Select HIGH to Chip Select LOW	4		4		ns

Minimum Write Pulse Disable


A (ADDRESS)
TWHWL (21)
W̄ (WRITE ENABLE)

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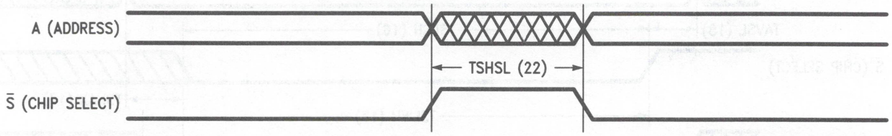
Minimum Select Pulse Disable


A (ADDRESS)
TSHSL (22)
S̄ (CHIP SELECT)

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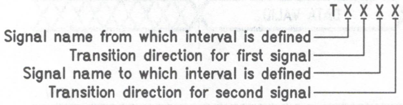
Standard Timing Parameter Abbreviations


T X X X X
Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

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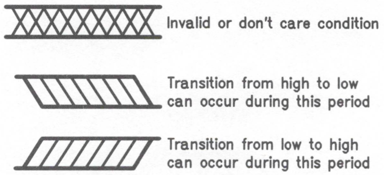
The transition definitions used in this data sheet are:

H = Transition to HIGH State
L = Transition to LOW State
V = Transition to Valid State
X = Transition to Invalid or Don't Care Condition

TIMING EXPLANATIONS

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for a device parameter. Those timing parameters which show a minimum value do so because the system must supply at least that much time, even though most devices do not need the full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory devices (i.e., access times) are specified as a maximum time because the device will never provide the data later than this stated value, and usually, much sooner.


Invalid or don't care condition
Transition from high to low can occur during this period
Transition from low to high can occur during this period

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Ordering Information

Part Number	Temperature Range	Package Type	Ordering Code
NM100494	0°C to +85°C	28-Pin Ceramic DIP	NM100494D15/18
NM100494	0°C to +85°C	28-Pin Flatpak	NM100494F15/18

National Semiconductor

NM10494 64k BiCMOS SRAM 16k x 4 Bit

General Description

The NM10494 is a 65,536-bit fully static, asynchronous, random access memory organized as 16,384 words by 4 bits. The device is based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

The NM10494 operates with a supply voltage of −5.2V ±5%, and the input and output voltage levels are 10k ECL I/O compatible.

Reading the memory is accomplished by pulling the chip select ($\overline{S}$) pin LOW while the write enable ($\overline{W}$) pin remains HIGH allowing the memory contents to be displayed on the output pins (Q0–Q3). The output pins will remain inactive (LOW) if either the chip select ($\overline{S}$) pin is HIGH or the write enable ($\overline{W}$) pin is LOW.

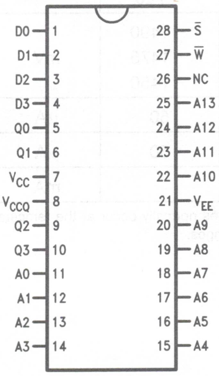
Writing to the device is accomplished by having the chip select ($\overline{S}$) and the write enable ($\overline{W}$) pins LOW. Data on the input pins will then be written into the memory address specified on the address pins (A0–A13).

Features

- 10 ns/12 ns/15 ns speed grades over the commercial temperature range
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- 10k ECL I/O
- Power supply −5.2V ±5%
- Low power dissipation <1.3W @ 50 MHz
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 28-pin flatpak and 28-pin ceramic DIP

Connection Diagrams

28-Pin Ceramic DIP


D0 1
D1 2
D2 3
D3 4
Q0 5
Q1 6
V_{CC} 7
V_{CCQ} 8
Q2 9
Q3 10
A0 11
A1 12
A2 13
A3 14
28 $\overline{S}$
27 $\overline{W}$
26 NC
25 A13
24 A12
23 A11
22 A10
21 V_{EE}
20 A9
19 A8
18 A7
17 A6
16 A5
15 A4

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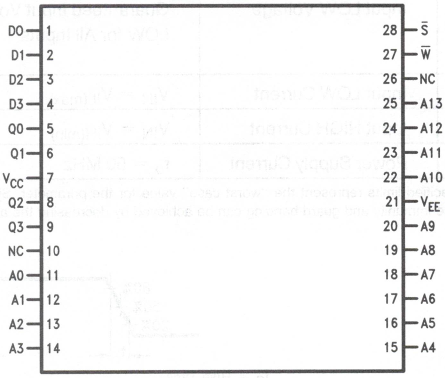
Top View

28-Pin Ceramic Flatpak (30 Mil Lead Pitch)


D0 1
D1 2
D2 3
D3 4
Q0 5
Q1 6
V_{CC} 7
Q2 8
Q3 9
NC 10
A0 11
A1 12
A2 13
A3 14
28 $\overline{S}$
27 $\overline{W}$
26 NC
25 A13
24 A12
23 A11
22 A10
21 V_{EE}
20 A9
19 A8
18 A7
17 A6
16 A5
15 A4

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Top View

Pin Names

A0–A13	Address Inputs
$\overline{S}$	Chip Select
$\overline{W}$	Write Enable
Q0–Q3	Data Out
D0–D3	Data In
V_{CC}	Ground
V_{EE}	Power

Absolute Maximum Ratings

Above which useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Static Discharge Voltage (Per MIL-STD 883)	>2001V
Maximum Junction Temperature (T_J)	+150°C
Output Current (DC Output HIGH)	−50 mA
Latch-Up Current	>200 mA

These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Test Conditions

Input Pulse Levels	*Figure 1*
Input Rise and Fall Times	0.7 ns
Output Timing Reference Levels	50% of Input
AC Test Circuit	*Figure 2*

Capacitance Tested by Sample Basis

Symbol	Parameter	Max	Units
C_{IN}	Input Pin Capacitance	5.0	pF
C_{OUT}	Output Pin Capacitance	8.0	pF

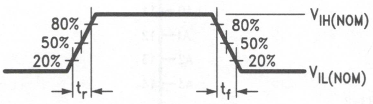
Operating Voltage

Device	Voltage
NM10494	$V_{EE} = -5.2V \pm 5\%$

DC Electrical Characteristics $V_{EE} = -5.2V$, $V_{CC} = V_{CCQ} = GND$, $T_C = 0°C$ to $+75°C$ (Note)

Symbol	Parameter	Conditions	Min	Max	Units	T_C
V_{OH}	Output HIGH Voltage	Loading is 50Ω to −2.0V	−1000	−840		0°C
			−960	−810	mV	+25°C
			−900	−720		+75°C
V_{OL}	Output LOW Voltage		−1870	−1665		0°C
			−1850	−1650	mV	+25°C
			−1830	−1625		+75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage HIGH for All Inputs	−1145	−840		0°C
			−1105	−810	mV	+25°C
			−1045	−720		+75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage LOW for All Inputs	−1870	−1490		0°C
			−1850	−1475	mV	+25°C
			−1830	−1450		+75°C
I_{IL}	Input LOW Current	$V_{IN} = V_{IL(max)}$	−50	50	μA	
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH(min)}$		50	μA	
I_{EE}	Power Supply Current	$f_o = 50$ MHz	−240		mA	

Note: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.



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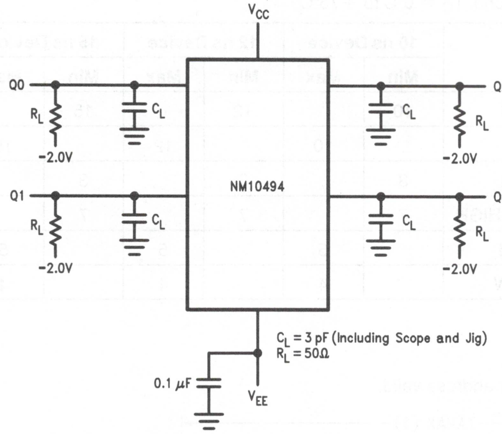
t_R = Rise Time
t_F = Fall Time
50% = Timing Reference Levels
$V_{IH(NOM)} = (V_{IH(MIN)} + V_{IH(MAX)})/2$
$V_{IL(NOM)} = (V_{IL(MIN)} + V_{IL(MAX)})/2$

FIGURE 1. Input Levels

DC Electrical Characteristics (Continued)


V_{CC}
Q0
Q1
Q2
Q3
R_L
C_L
-2.0V
NM10494
0.1 µF
V_{EE}

C_L = 3 pF (Including Scope and Jig)
R_L = 50Ω

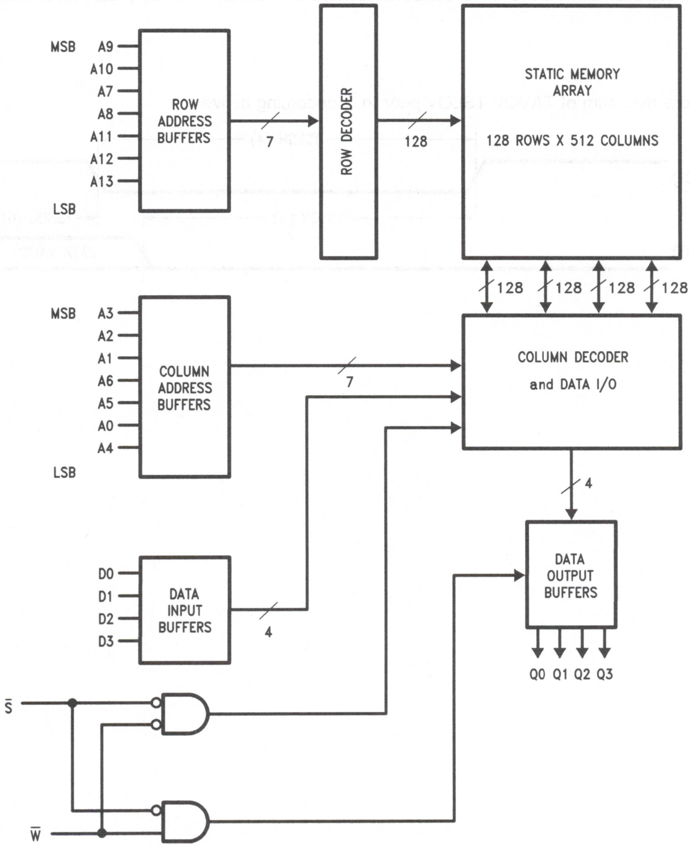
TL/D/10393-5

FIGURE 2. AC Test Circuit

Truth Table

$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Q	Read

Logic Diagram


MSB
A9
A10
A7
A8
A11
A12
A13
LSB
ROW ADDRESS BUFFERS
7
ROW DECODER
128
STATIC MEMORY ARRAY
128 ROWS X 512 COLUMNS
128
128
128
128
MSB
A3
A2
A1
A6
A5
A0
A4
LSB
COLUMN ADDRESS BUFFERS
7
COLUMN DECODER and DATA I/O
4
D0
D1
D2
D3
DATA INPUT BUFFERS
4
DATA OUTPUT BUFFERS
Q0 Q1 Q2 Q3
S̄
W̄

TL/D/10393-6

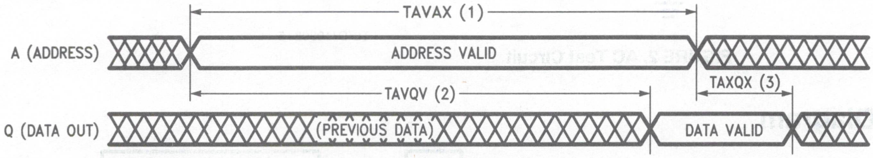
Read Cycles

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +75°C

No.	Symbol		Parameter	10 ns Device		12 ns Device		15 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	Min	Max	
1	TAVAX	TRC	Address Valid to Address Invalid	10		12		15		ns
2	TAVQV	TAA	Address Valid to Output Valid		10		12		15	ns
3	TAXQX	TOH	Address Invalid to Output Invalid	3		3		3		ns
4	TSLSH	TRC	Chip Select LOW to Chip Select HIGH	7		7		7		ns
5	TSLQV	TACS	Chip Select LOW to Output Valid		5		5		5	ns
6	TSHQL	TRCS	Chip Select HIGH to Output LOW		4		4		4	ns

Read Cycle 1

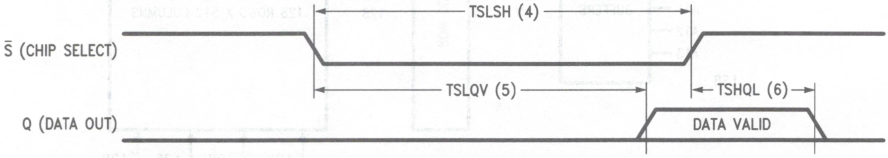
Where $\overline{S}$ is active prior to or within TAVQV-TSLQV after address valid.


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TAVQV (2)
TAXQX (3)
Q (DATA OUT)
(PREVIOUS DATA)
DATA VALID

TL/D/10393-7

Read Cycle 2

Where address is valid a minimum of TAVQV-TSLQV prior to $\overline{S}$ becoming active.


TSLSH (4)
S̄ (CHIP SELECT)
TSLQV (5)
TSHQL (6)
Q (DATA OUT)
DATA VALID

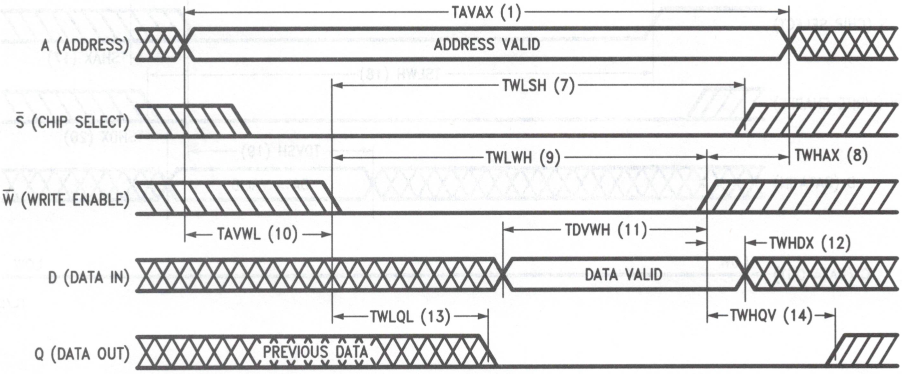
TL/D/10393-8

Write Cycle 1

This write cycle is $\overline{W}$ controlled, where $\overline{S}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data out (Q) may become active and requires observance of TWLQL to avoid data bus contention in common I/O applications. At the end of the write cycle the data may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{S}$ becoming inactive (HIGH).

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +75°C

No.	Symbol		Parameter	10 ns Device		12 ns Device		15 ns Device		Units
	Std.	**Alt.**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
1	TAVAX	TWC	Address Valid to Address Invalid	10		12		15		ns
7	TWLSH		Write Enable LOW to Chip Select HIGH	7		8		10		ns
8	TWHAX	TWHA	Write HIGH to Address Don't Care	0		0		0		ns
9	TWLWH	TW	Write LOW to Write HIGH	7		8		10		ns
10	TAVWL	TWSA	Address Valid to Write LOW	0		0		0		ns
11	TDVWH		Data Valid to Write HIGH	7		8		10		ns
12	TWHDX	TWHD	Write HIGH to Data Don't Care	0		0		0		ns
13	TWLQL	TWS	Write LOW to Output LOW		5		5		5	ns
14	TWHQV	TWR	Write HIGH to Output Valid		10		12		15	ns


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TWLSH (7)
S̄ (CHIP SELECT)
TWLWH (9)
TWHAX (8)
W̄ (WRITE ENABLE)
TAVWL (10)
TDVWH (11)
TWHDX (12)
D (DATA IN)
DATA VALID
TWLQL (13)
TWHQV (14)
Q (DATA OUT)
PREVIOUS DATA

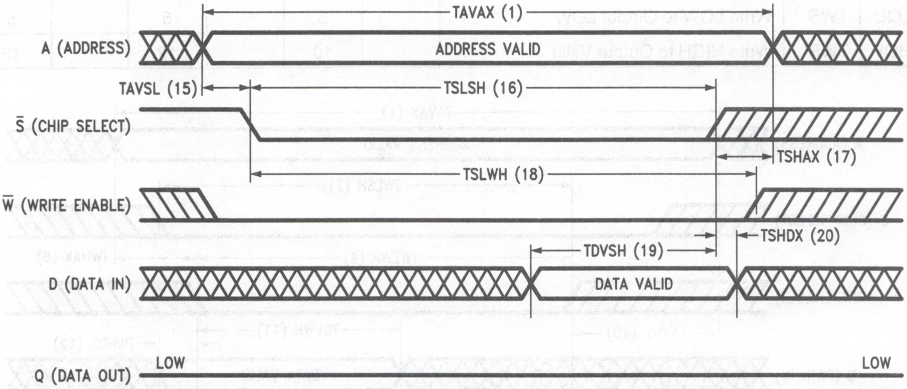
TL/D/10393-9

Write Cycle 2

This write cycle is $\overline{S}$ controlled, where $\overline{W}$ is active prior to, or coincident with, $\overline{S}$ becoming active (LOW). Write cycle 2 has identical specifications to write cycle 1 with the exceptions of $\overline{W}$ and S being interchanged. This write cycle may be more convenient for common I/O applications because data bus restrictions are alleviated.

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +75°C

No.	Symbol		Parameter	10 ns Device		12 ns Device		15 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	Min	Max	
15	TAVSL	TWSA	Address Valid to Chip Select LOW	0		0		0		ns
16	TSLSH		Chip Select LOW to Chip Select HIGH	7		8		10		ns
17	TSHAX	TWHA	Chip Select HIGH to Address Don't Care	0		0		0		ns
18	TSLWH		Chip Select LOW to Write Enable HIGH	7		8		10		ns
19	TDVSH		Data Valid to Chip Select HIGH	7		8		10		ns
20	TSHDX	TWHD	Chip Select HIGH to Data Don't Care	0		0		0		ns


TAVAX (1)
A (ADDRESS)
ADDRESS VALID
TAVSL (15)
TSLSH (16)
$\overline{S}$ (CHIP SELECT)
TSHAX (17)
TSLWH (18)
$\overline{W}$ (WRITE ENABLE)
TSHDX (20)
TDVSH (19)
D (DATA IN)
DATA VALID
Q (DATA OUT)
LOW
LOW

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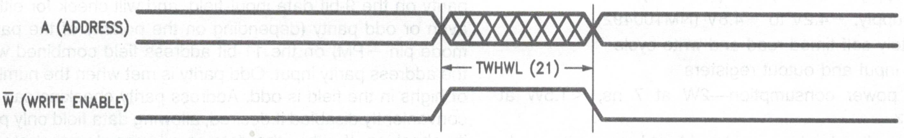
Consecutive Write Cycles

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +75°C

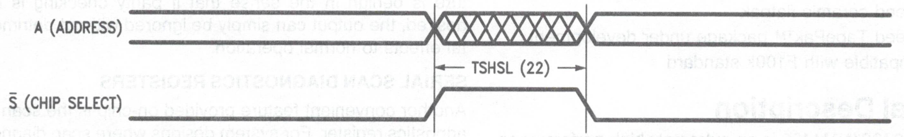
No.	Symbol		Parameter	10 ns Device		12 ns Device		15 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	Min	Max	
21	TWHWL	$\overline{\text{TWP}}$	Write Enable HIGH to Write Enable LOW	2		3	4			ns
22	TSHSL	$\overline{\text{TSP}}$	Chip Select HIGH to Chip Select LOW	2		3		4		ns

Minimum Write Pulse Disable


A (ADDRESS)
TWHWL (21)
W̄ (WRITE ENABLE)

TL/D/10393-11

Minimum Select Pulse Disable


A (ADDRESS)
TSHSL (22)
S̄ (CHIP SELECT)

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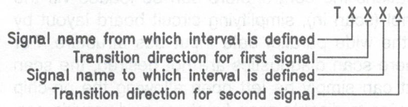
Standard Timing Parameter Abbreviations


T X X X X
Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

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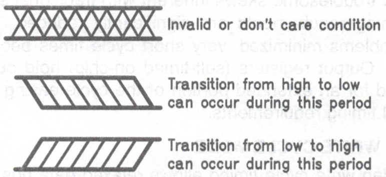
The transition definitions used in this data sheet are.

H = Transition to HIGH State
L = Transition to LOW State
V = Transition to Valid State
X = Transition to Invalid or Don't Care Condition

TIMING EXPLANATIONS

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for a device parameter. Those timing parameters which show a minimum value do so because the system must supply at least that much time, even though most devices do not need the full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory devices (i.e., access times) are specified as a maximum time because the device will never provide the data later than this stated value, and usually, much sooner.


Invalid or don't care condition
Transition from high to low can occur during this period
Transition from low to high can occur during this period

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Ordering Information

Part Number	Temperature Range	Package Type	Ordering Code
NM10494	0°C to +75°C	28-Pin Ceramic DIP	NM10494D10/D12/D15
NM10494	0°C to +75°C	28-Pin Flatpak	NM10494F10/F12/F15

National Semiconductor

PRELIMINARY

NM100492/NM4492 2k x 9 Advanced Self-Timed SRAM

Features

- Extremely fast access time
  - 5 ns Max (NM4492)
  - 7 ns Max (NM100492)
- Power supply: −5.2V ± 5% (NM4492)
- Power supply: −4.2V to −4.8V (NM100492)
- Completely self-timed read and write cycle
- On-chip input and output registers
- Modest power consumption—2W at 7 ns, <1.5W at 100 MHz
- On-chip parity checking—with odd address parity mode pin
- Clock enable input simplifies pipeline control
- Scan diagnostics supported by on-chip scan registers
- High speed ceramic flatpak
- High speed TapePak™ package under development
- I/O compatible with F100k standard

General Description

The NM100492/NM4492 is an extremely high performance 2k x 9 SRAM. It is the first of a family of similar 9-bit wide SRAMs designed specifically for very high speed ECL computer applications such as register files, writable control stores, cache RAMs, cache tag RAMs, and address translation lookaside buffers. The NM100492/NM4492 offers several features which are very desirable in such applications.

ADVANCED SELF-TIMED ARCHITECTURE

This advanced self-timed RAM simplifies the system design of extremely fast memory arrays by minimizing the impact of timing skews on the cycle time of the memory array. All input signals (address, data and control signals) are registered on-chip by a transition of the clock. By registering all inputs with minimal setup and hold times (setup + hold = 2 ns) the troublesome skews inherent with traditional static RAM timing requirements are significantly reduced. With skew problems minimized, very short cycle times become practical. Output registers (self-timed on-chip) hold output data valid for an extended portion of the cycle easing system read timing requirements.

HIDDEN WRITE CYCLE MODE

The hidden write cycle timing allows relaxed data bus timing. This will often ease system setup and hold requirements for the data output bus. Hidden write timing is essentially a technique for interleaving reads and writes. This advanced self-timed SRAM supports hidden write timing more conveniently in the system than first generation self-timed SRAM's, due to the unique control signal functions defined for write enable ($\overline{W}$) and chip select ($\overline{S}$). By keeping the output register active (with the last read data) during a write cycle, this device greatly simplifies the timing of interleaved memory architectures. This mode may be very useful in cache and register file applications, where multiple sources and/or destinations may be interleaved within each machine cycle.

PARITY CHECKING

The device also offers several convenient features which may be useful in specific applications. One such feature is the on-chip parity checking function. For systems where parity checking is desirable this device will check for odd parity on the 9-bit data input field, and will check for either even or odd parity (depending on the polarity of the parity mode pin −PM) on the 11-bit address field combined with the address parity input. Odd parity is met when the number of highs in the field is odd. Address parity checking can be conveniently disabled if desired, allowing data field only parity checking. If either the data or address demonstrates a parity error, then the parity error output flag is set. The polarity of the error output flag facilitates emitter dot ORing several error outputs for minimal delay. The parity checking feature is benign in the sense that if parity checking is not desired, the output can simply be ignored without detrimental effects to normal operation.

SERIAL SCAN DIAGNOSTICS REGISTERS

Another convenient feature provided on-chip is the scan diagnostics register. For system designs where scan diagnostics are included, this device allows observing the state of the input registers (scan out) and forcing the state of the input and output registers (scan in). For writable control store applications the control store can be loaded via the serial channel (scan in), simplifying circuit board layout by eliminating the wide parallel data input bus structure. For systems where scan diagnostics are not desired, the scan enable input can simply be left open allowing the on-chip pulldown device to disable scan functions and provide normal SRAM functionality.

PIPELINE CONTROL

Yet a third convenient feature is the clock enable input. This control simplifies starting and stopping pipeline operations in pipelined systems. It reduces, and may eliminate, the need to gate the clock signal external to the RAM. This feature is also benign since the on-chip pulldown device will ensure normal operation if the clock enable is not used.

MODEST POWER CONSUMPTION

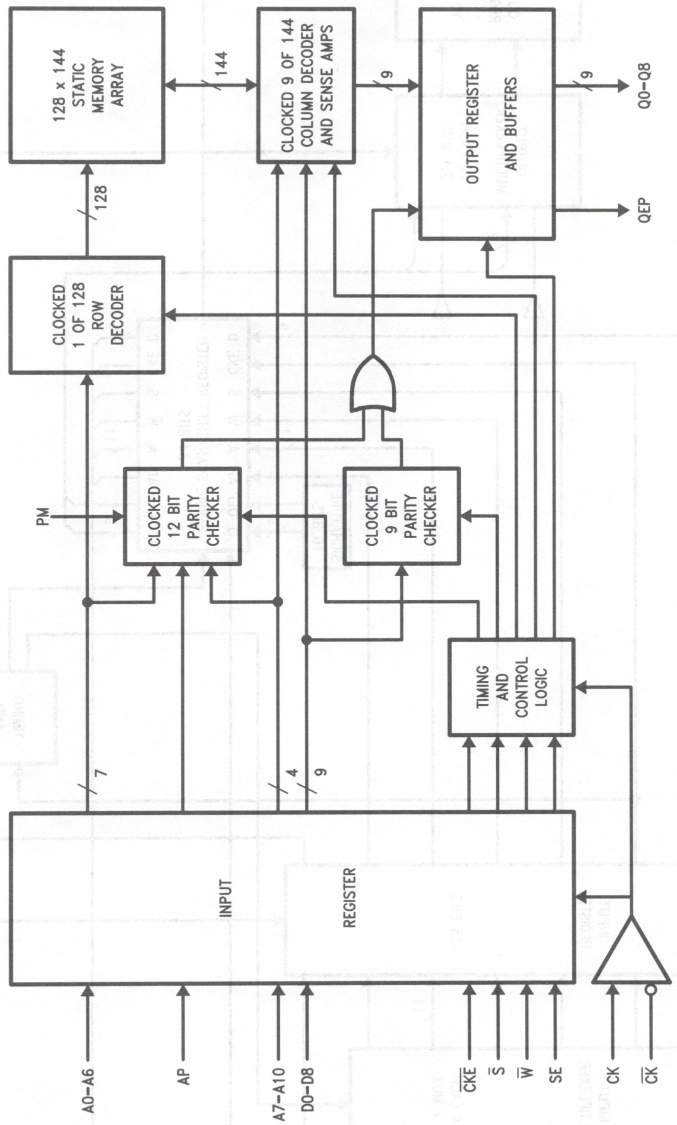
Modest power consumption is achieved without compromising device speed through very unique and innovative circuit design techniques (patents applied for). Power consumption is predominately dependent on clock frequency (1/cycle time) allowing a reduction in power at lower operating frequency.

F100K COMPATIBLE I/O

The device is I/O compatible with standard temperature compensated F100K ECL logic, allowing trouble free interfacing in high performance ECL systems.

Functional Block Diagram

Scan Functions Excluded


128 x 144 STATIC MEMORY ARRAY
144
CLOCKED 9 OF 144 COLUMN DECODER AND SENSE AMPS
9
OUTPUT REGISTER AND BUFFERS
9
Q0–Q8
QEP
128
CLOCKED 1 OF 128 ROW DECODER
PM
CLOCKED 12 BIT PARITY CHECKER
CLOCKED 9 BIT PARITY CHECKER
TIMING AND CONTROL LOGIC
7
4
9
INPUT REGISTER
A0–A6
AP
A7–A10
D0–D8
$\overline{\text{CKE}}$
$\overline{\text{S}}$
$\overline{\text{W}}$
SE
CK
$\overline{\text{CK}}$

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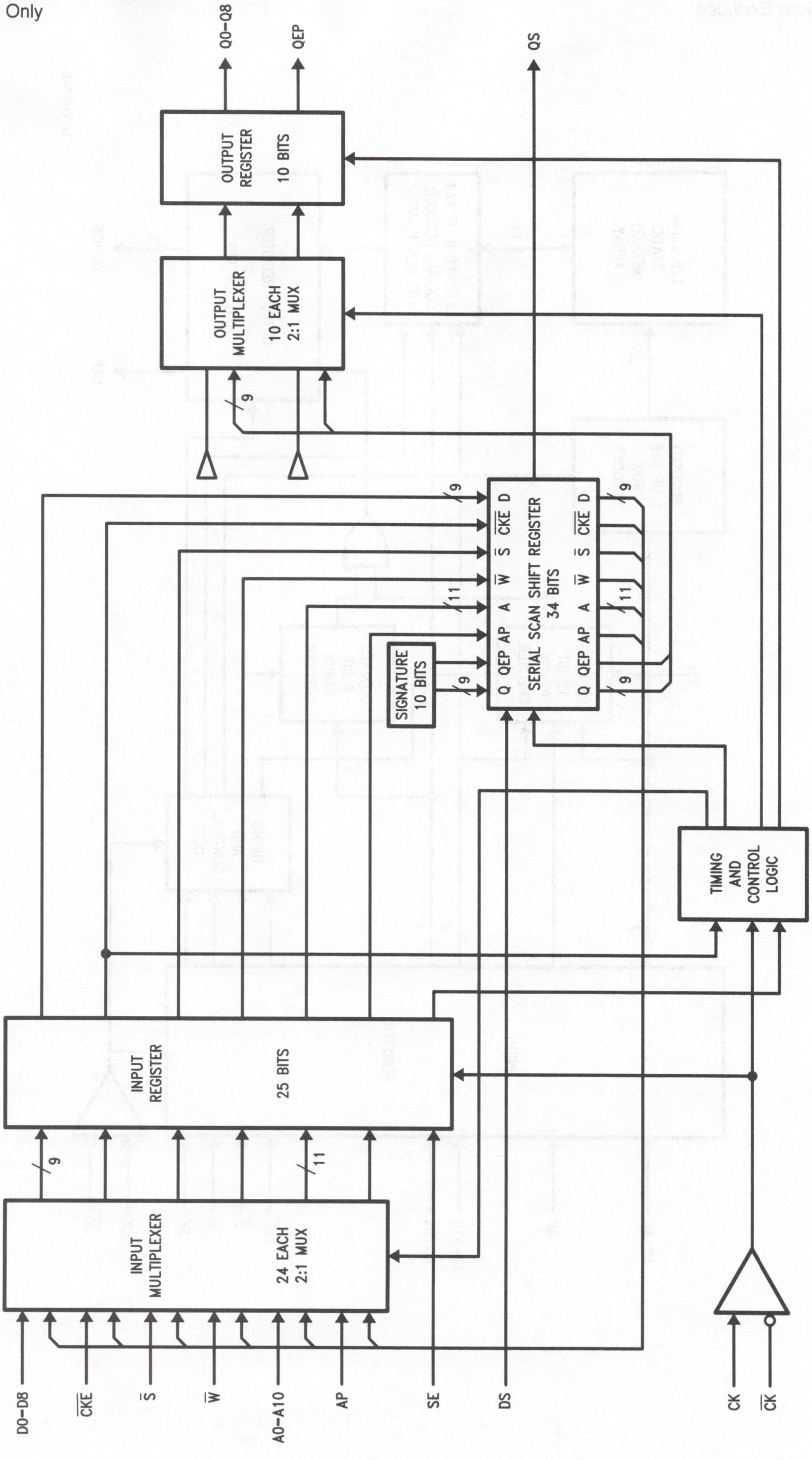
Functional Block Diagram (Continued)

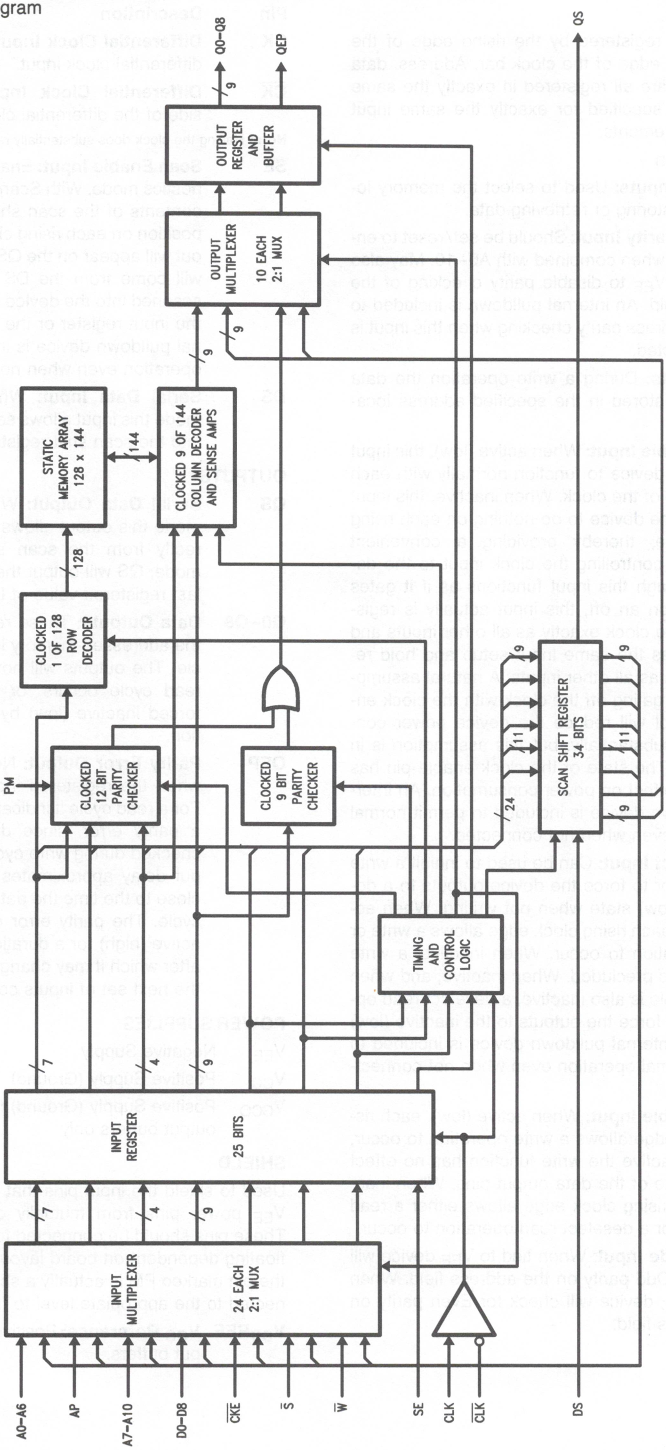
Scan Functions Only


Q0–Q8
QEP
QS
OUTPUT REGISTER 10 BITS
OUTPUT MULTIPLEXER 10 EACH 2:1 MUX
9
SERIAL SCAN SHIFT REGISTER 34 BITS
Q QEP AP A W̄ S̄ CKE D
Q QEP AP A W̄ S̄ CKE D
9
11
9
11
9
9
SIGNATURE 10 BITS
TIMING AND CONTROL LOGIC
INPUT REGISTER 25 BITS
9
11
INPUT MULTIPLEXER 24 EACH 2:1 MUX
D0–D8
CKE
S̄
W̄
A0–A10
AP
SE
DS
CK
CK̄

TL/D/9748-2

Functional Block Diagram (Continued)

Complete Functional Diagram


A0–A6
AP
A7–A10
D0–D8
$\overline{\text{CKE}}$
$\overline{\text{S}}$
$\overline{\text{W}}$
SE
CLK
$\overline{\text{CLK}}$
DS
INPUT MULTIPLEXER
24 EACH 2:1 MUX
INPUT REGISTER
25 BITS
7
4
9
CLOCKED 1 OF 128 ROW DECODER
128
STATIC MEMORY ARRAY 128 x 144
144
CLOCKED 9 OF 144 COLUMN DECODER AND SENSE AMPS
CLOCKED 12 BIT PARITY CHECKER
PM
CLOCKED 9 BIT PARITY CHECKER
TIMING AND CONTROL LOGIC
SCAN SHIFT REGISTER 34 BITS
24
11
9
OUTPUT MULTIPLEXER
10 EACH 2:1 MUX
OUTPUT REGISTER AND BUFFER
Q0–Q8
QEP
QS

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Advanced Self-Timed RAM Pin Descriptions

INPUTS

All input signals are registered by the rising edge of the clock, and the falling edge of the clock bar. Address, data in, and control lines are all registered in exactly the same manner, and are all specified for exactly the same input setup and hold requirements.

Pin	Description
A0–A10	**Address Inputs:** Used to select the memory location for storing or retrieving data.
AP	**Address Parity Input:** Should be set/reset to ensure parity when combined with A0–10. May also be tied to V_{EE} to disable parity checking of the address field. An internal pulldown is included to disable address parity checking when this input is not connected.
D0–D8	**Data Inputs:** During a write operation the data inputs are stored in the specified address location.
$\overline{\text{CKE}}$	**Clock Enable Input:** When active (low), this input allows the device to function normally with each rising edge of the clock. When inactive, this input will force the device to do nothing on each rising clock edge, thereby providing a convenient means for controlling the clock input to the device. Although this input functions as if it gates the clock on an off, this input actually is registered by the clock exactly as all other inputs and as such has the same input setup and hold requirements as all other inputs. A natural assumption is that gating off the clock with the clock enable control will reduce the device power consumption substantially; but this assumption is in fact false. The state of the clock enable pin has very little effect on power consumption. An internal pulldown device is included to permit normal operation even when not connected.
$\overline{\text{S}}$	**Chip Select Input:** Can be used to inhibit a write operation or to force the device outputs to a deselected (low) state when not writing. When active (low), each rising clock edge allows a write or read operation to occur. When inactive, a write operation is precluded. When inactive, and when Write Enable is also inactive, a deselect read operation will force the outputs to the inactive (low) state. An internal pulldown device is included to permit normal operation even when not connected.
$\overline{\text{W}}$	**Write Enable Input:** When active (low), each rising clock edge allows a write operation to occur, but when active the write function has no effect on the state of the data output pins. When inactive, each rising clock edge allows either a read operation or a deselect read operation to occur.
PM	**Parity Mode Input:** When tied to V_{EE} device will check for Odd parity on the address field. When tied to V_{CC} device will check for Even parity on the address field.

Pin	Description
CK	**Differential Clock Input:** The "true" side of the differential clock input.
$\overline{\text{CK}}$	**Differential Clock Input:** The "complement" side of the differential clock input.

Note: Halting the clock does substantially reduce power consumption.

Pin	Description
SE	**Scan Enable Input:** Enables the serial scan diagnostics mode. With Scan Enable active (high), the contents of the scan shift register is shifted one position on each rising clock edge. The bit shifted out will appear on the QS pin and the bit shifted in will come from the DS pin. Information serially scanned into the device can be loaded into either the input register or the output register. An internal pulldown device is included to permit normal operation even when not connected.
DS	**Serial Data Input:** When in scan diagnostics mode this input allows serial shifting external data into the scan shift register.

OUTPUTS

Pin	Description
QS	**Serial Data Output:** When in scan diagnostics mode this output allows reading internal data directly from the scan shift register. In normal mode, QS will output the same logic level as the last registered value of D8.
Q0–Q8	**Data Outputs:** These represent the contents of the addressed memory location during a read cycle. The outputs will not change unless another read cycle occurs, or unless the outputs are forced inactive (low) by a deselect read operation.
QEP	**Parity Error Output:** Normally low, it goes high when the registered inputs have a parity error. For a read cycle it indicates the address input has a parity error, since data input parity is only checked during write cycles. The parity error output delay approximates access time, appearing close to the time the data word appears in a read cycle. The parity error output signal will remain active (high) for a duration of the one cycle time, after which it may change back to inactive (low) if the next set of inputs contains no parity errors.

POWER SUPPLIES

V_{EE}	Negative Supply
V_{CC}	Positive Supply (Ground)
V_{CCQ}	Positive Supply (Ground) for output buffers only

SHIELD

Used to shield the input pins that are adjacent to V_{CC} and V_{EE} power pins from mutually coupled inductive noise. These pins should be connected to a DC power level or left floating dependent on board layout convenience. Note that the pin marked PM is actually a shield pin but must be connected to the appropiate level to facilitate parity.

V_{CC}REF	**V_{CC} Reference:** Positive supply reference for input buffers.

Truth Tables

Recall that all inputs are registered by a rising clock edge. The following truth tables illustrate device operation if the inputs shown are registered; the outputs shown will appear at access time.

NORMAL OPERATIONS

Normal operations are defined by SE = low for prior and current cycle.

Inputs								Outputs		Type of Operation
$\overline{\text{CKE}}$	$\overline{\text{S}}$	$\overline{\text{W}}$	A	AP	PM	D	Data Parity	Q	QEP	
H	X	X	X	X	X	X	(X)	NC	NC	No Operation
L	L	H	V	O	L	X	(X)	V	L	Read
L	L	H	V	E	H	X	(X)	V	L	Read
L	H	H	X	X	X	X	(X)	L	L	Deselect
L	L	H	V	E	L	X	(X)	V	H	Read, A Parity Error
L	L	H	V	O	H	X	(X)	V	H	Read, A Parity Error
L	L	L	V	O	L	V	(O)	NC	L	Write
L	L	L	V	E	H	V	(O)	NC	L	Write
L	H	L	X	X	X	X	(X)	NC	L	Write Inhibit
L	L	L	V	E	L	V	(O)	NC	H	Write, A Parity Error
L	L	L	V	O	H	V	(O)	NC	H	Write, A Parity Error
L	L	L	V	O	L	V	(E)	NC	H	Write, D Parity Error
L	L	L	V	E	H	V	(E)	NC	H	Write, D Parity Error

Special Characters: O = Odd, E = Even, NC = No Change

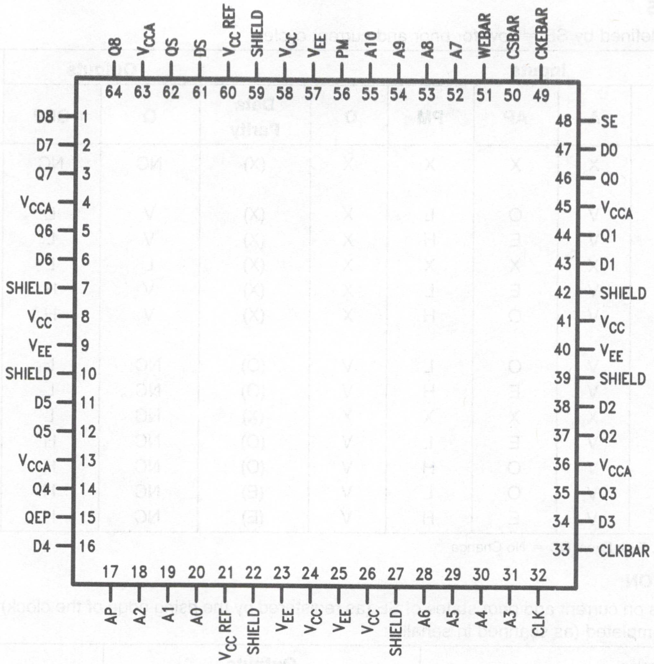
SCAN MODE OPERATION

Scan operation depends on current and prior states of SE (as registered by the rising edge of the clock), and on the state of the $\overline{\text{CKE}}$ bit after scan is completed (as scanned in serially):

Inputs				Outputs			Type of Operation
Prior SE	Current SE	Scanned $\overline{\text{CKE}}$	DS	QS	Q	QEP	
L	L	X	X	D8	X	X	Normal Operation
L	H	X	X	D7	NC	NC	Enter scan mode and do first shift
H	H	X	V	V	NC	NC	Serial shift on each clock
H	L	L	X	V	V/NC	V/NC	Exit scan mode; do last shift and then execute instruction scanned into input register; if read or deselect Q and QEP will update, else no change
H	L	H	X	V	V	V	Exit scan mode; do last shift and then copy scan register into Q and QEP; do not execute input instruction

Connection Diagram

Pin Out


1 D8
2 D7
3 Q7
4 V_{CCA}
5 Q6
6 D6
7 SHIELD
8 V_{CC}
9 V_{EE}
10 SHIELD
11 D5
12 Q5
13 V_{CCA}
14 Q4
15 QEP
16 D4
17 AP
18 A2
19 A1
20 A0
21 V_{CC} REF
22 SHIELD
23 V_{EE}
24 V_{CC}
25 V_{EE}
26 V_{CC}
27 SHIELD
28 A6
29 A5
30 A4
31 A3
32 CLK
33 CLKBAR
34 D3
35 Q3
36 V_{CCA}
37 Q2
38 D2
39 SHIELD
40 V_{EE}
41 V_{CC}
42 SHIELD
43 D1
44 Q1
45 V_{CCA}
46 Q0
47 D0
48 SE
49 CKEBAR
50 CSBAR
51 WEBAR
52 A7
53 A8
54 A9
55 A10
56 PM
57 V_{EE}
58 V_{CC}
59 SHIELD
60 V_{CC} REF
61 DS
62 QS
63 V_{CCA}
64 Q8

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Top View

Note: Pin 26 is reserved for (A11).
Pin 57 is reserved for (A12).

Absolute Maximum Ratings Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C Max
Case Temperature under Bias	0°C to +75°C
V_{EE} Potential (to Ground)	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} − 0.5V to +0.5V
Output Current (DC, High)	−50 mA Max

Power consumption of the device is primarily a function of the clock frequency. Linear derating of the operating current specified less the quiescent current specified by 1.25 mA/MHz will result in a reasonable approximation at the frequency of interest (lower frequency results in lower power).

Operating Voltage

Device	Voltage
NM4492	V_{EE} = −5.2V ±5%
NM100492	V_{EE} = −4.2V to −4.8V

DC Characteristics T_C = 0°C to +75°C

Symbol	Parameter	Conditions	Min	Max	Units
I_{EEO}	Operating Current (−5)	T_{CHCH} = 5 ns	−500		mA
I_{EEO}	Operating Current (−7)	T_{CHCH} = 7 ns	−400		mA
I_{EEO}	Operating Current (−10)	T_{CHCH} = 10 ns	−330		mA
I_{EEQ}	Quiescent Current	Clock = V_{IL}/V_{IH}	−120		mA
I_{IL}	Input Low Current		−50	+170	µA
I_{IH}	Input High Current			+220	µA
V_{OH}	Output HIGH Voltage	50Ω to −2V	−1025	−880	mV
V_{OL}	Output LOW Voltage	50Ω to −2V	−1810	−1620	mV
V_{OHC}	Output HIGH Corner V	50Ω to −2V	−1025		mV
V_{OLC}	Output LOW Corner V	50Ω to −2V		−1620	mV
V_{IH}	Input HIGH Voltage		−1165	−880	mV
V_{IL}	Input LOW Voltage		−1810	−1475	mV

Read Cycle

DESCRIPTION

A read cycle is performed when the following conditions are present at the time the clock rising edge registers the inputs: $\overline{CKE}$ = Low, $\overline{S}$ = Low, $\overline{W}$ = High, SE = Low and was low for the previous cycle also. At access time the outputs become valid, making a single glitch free transition from the previous state to the new state. A deselect read cycle is very similar to a read cycle except that $\overline{S}$ = High, and the outputs all go inactive (low) at access time. The minimum read cycle time realized in an application is largely a function of the system skews between inputs, and of setup and hold requirements of the device to which the RAM provides data. If the address field and address parity bit combine to parity then the parity error output will not assert, remaining low. The parity error output timing closely approximates access time and meets the same specifications.

AC Characteristics

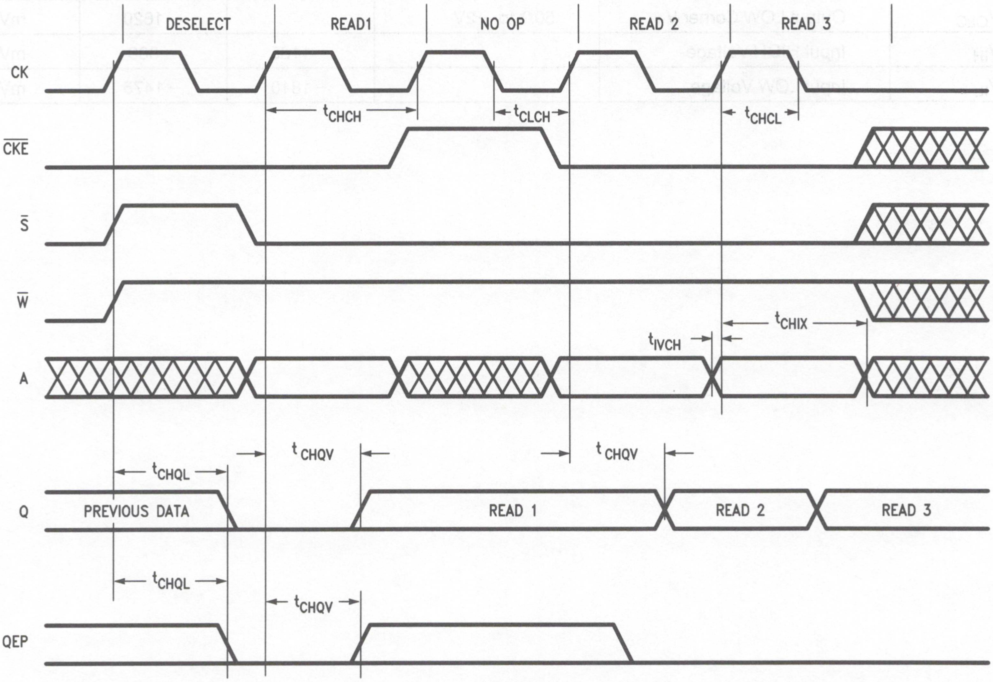
T_C = 0°C to +75°C. Input levels are −0.9V and −1.7V. Timing References are −1.3V (Note 1).

Symbol	Parameter	5 ns (Prelim)		7 ns Device		10 ns Device		Units
		Min	Max	Min	Max	Min	Max	
t_{CHCH}	Cycle Time	5		7		10		ns
t_{CHQV}	Access Time (Note 2)	2.5	5	2.5	7	2.5	10	ns
t_{CHQL}	Disable Time	2.5	5	2.5	7	2.5	10	ns
t_{IVCH}	Input Setup Time	0		0		0		ns
t_{CHIX}	Input Hold Time	2		2.5		3		ns
t_{CHCL}	Clock High Pulse Width	1.5		1.5		2		ns
t_{CLCH}	Clock Low Pulse Width	1.5		1.5		2		ns
t_{CHQEPV}	Parity Access (Note 2)	2.5	5	2.5	7	2.5	10	ns

Output Load: 3.0 pF and 50Ω to −2.0V

Note 1: All maximum timing specs are referenced to the latter of CLK and $\overline{CLK}$, whichever occurs later. All minimum timing specs are referenced to the earlier of CLK and $\overline{CLK}$. CLK and $\overline{CLK}$ must cross each other between 10% and 90% of AC input levels.

Note 2: Maximum access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.



TL/D/9748-5

Write Cycle

DESCRIPTION

A write cycle is performed when the following conditions are present at the time the clock rising edge registers the inputs: $\overline{CKE}$ = Low, $\overline{S}$ = Low, $\overline{W}$ = Low, SE = Low and was low for the previous cycle also. The minimum write cycle time realized in an application is largely a function of the system skews on the inputs. Notice that a write cycle will not cause a change in any output except the parity error output; data outputs remain unchanged in any case. During writes parity is checked on both the address field (combined with the address parity input) and the data field. The parity error output will not assert if both fields show parity. The parity error output timing closely approximates access time and meets the same access time specifications.

AC Characteristics

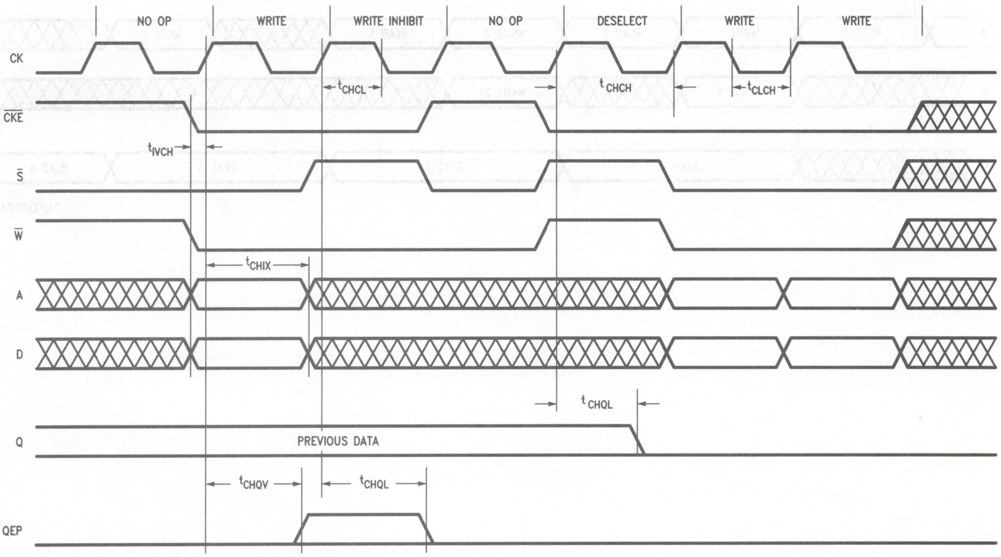
T_C = 0°C to +75°C. Input levels are −0.9V and −1.7V. Timing References are −1.3V (Note 1).

Symbol	Parameter	5 ns (Prelim)		7 ns Device		10 ns Device		Units
		Min	Max	Min	Max	Min	Max	
t_{CHCH}	Cycle Time	5		7		10		ns
t_{IVCH}	Input Setup Time	0		0		0		ns
t_{CHIX}	Input Hold Time	2		2.5		3		ns
t_{CHCL}	Clock High Pulse Width	1.5		1.5		2		ns
t_{CLCH}	Clock Low Pulse Width	1.5		1.5		2		ns
t_{CHQV}	Parity Access Time	2.5	5	2.5	7	2.5	10	ns
t_{CHQL}	Disable Time	2.5	5	2.5	7	2.5	10	ns

Output Load: 3.0 pF and 50Ω to −2.0V

Note 1: All maximum timing specs are referenced to the latter of CLK and $\overline{CLK}$, whichever occurs later. All minimum timing specs are referenced to the earlier of CLK and $\overline{CLK}$. CLK and $\overline{CLK}$ must cross each other between 10% and 90% of AC input levels.

Note 2: Maximum access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.



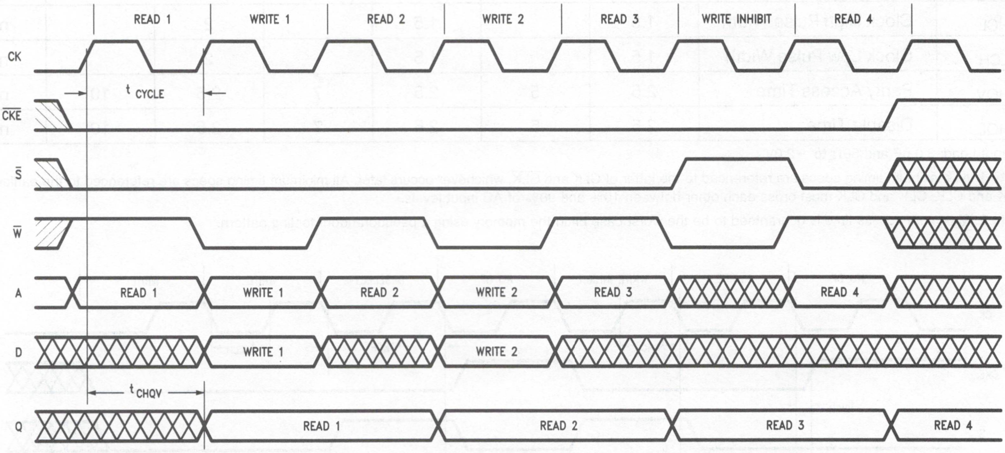
TL/D/9748-6

Hidden Write Cycle

The hidden write cycle allows the SRAM to be operated at twice the bandwidth of the data output bus. With relaxed data bus timing (relative to the SRAM address & control input timing) system constraints of setup and hold times may be much more easily met. Hidden write is a technique for interleaving read and write cyles in such a way that the write cycle timing has no effect on the data output bus (read timing). To allow hidden write operation the definition of the functions performed by select ($\overline{S}$) and write ($\overline{W}$) are subtly but importantly different than implemented on common SRAMs.

With hidden write timing there are no unusual restrictions. Consecutive read and write cycles may be at different or at the same address location. If a read is not desired at any given moment a read deselect or a no op may be executed instead. Similarly, if a write is unnecessary a write inhibit or no op may be substituted.

Hidden write can provide throughput enhancement in certain cases. If, for example, the RAM is utilized as a register file, and provides data to a pipelined ALU implemented in a gate array. If the ALU data input register requires 3 ns setup and 3 ns hold, the total data input window required is 4 ns wide. The SRAM maximum access is 7 ns, and the minimum access time is 2.5 ns; the difference is the guaranteed data output valid window. In this example the SRAM must be operated at greater than 9 ns cycle time to allow room for data and clock skews. Depending on system details maybe 10 or 11 ns cycle could be practical. In contrast, using hidden write timing the memory could be run at 7 ns cycles with the data output bus cycle times of 14 ns, easing the ALU setup and hold times while allowing a store and a fetch every 14 ns.



TL/D/9748–7

Scan Mode

DESCRIPTION

The scan mode allows serial input and output for diagnostics or for loading RAM (e.g., in a writable control store application). In overview:

1. The first clock cycle with scan active (SE = High) causes the device to enter scan mode and serially shift.
2. Succeeding clock cycles with scan active cause serial shifting, and
3. The first clock cycle with scan inactive (SE = Low) causes the device to shift and then execute (conditionally) either the scanned in instruction or to force the outputs to a scanned in test vector (see truth table).

Several devices can be linked serially in a scan chain. A detailed description follows:

1. Scan bits are transferred from the input register to the scan serial register at the end of every regular read or write cycle. The device also transfers a fixed scan signature into the remaining bits of the serial scan register in preparation to also shift this data out (the remaining bits are those bits of the serial shift register which correspond with the output register).
2. On the first and each succeeding clock rising edge with scan active (SE = High) the device will shift the serial shift register one bit.
   A. The state of DS is shifted into the chain.
   B. The last bit of the chain is shifted out on QS.
   C. The other outputs remain unchanged. The rest of the RAM executes a no operation. It will not write regardless of the state of the bit in the WE location of the input register.
   D. Any number of shifts can occur in scan mode; two to infinite shifts are possible.
3. The first rising clock edge with scan inactive (SE = Low) causes the device to shift the scan chain and exit scan mode and to conditionally either:
   A. Execute the scanned in instruction (e.g., read, write, deselect) with normal timing response (access, cycle) only if the scanned in bit in the $\overline{\text{CKE}}$ location of the input register is active ($\overline{\text{CKE}}$ = Low). The output may be affected, according to the instruction executed. The contents of the scan register bits corresponding to the output register are ignored.

   Or:

   B. Transfer the contents of the scan register into the output buffer, and ignore the contents of the input register, only if the scanned in bit in the $\overline{\text{CKE}}$ location of the input register is inactive ($\overline{\text{CKE}}$ = High).
4. The second and succeeding clock cycles after scan is inactive (SE = Low) are defined as normal mode operations and do not cause any scan functions.

The scan sequence is:

Input DS
to Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, QEP,
to AP, A2, A1, A0, A6, A5, A4, A3, A10, A9, A8, A7,
to $\overline{\text{WE}}$, $\overline{\text{CS}}$, $\overline{\text{CKE}}$,
to D0, D1, D2, D3, D4, D5, D6, D7, D8,
to QS Output

The scan logic is designed to output a sequence of bits recognizable as a scan signature, intended as an aid in fault detection in those cases where the fault causes a malfunction in the serial scan chain. This bit sequence can be easily recognized by the scan diagnostics processor as it is shifted out, providing a reasonably sure method of determining where and/or if the serial scan chain is defective. The scan signature bit sequence corresponds to the outputs:

Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	QEP
H	L	L	H	L	H	L	H	H	L

AC Characteristics

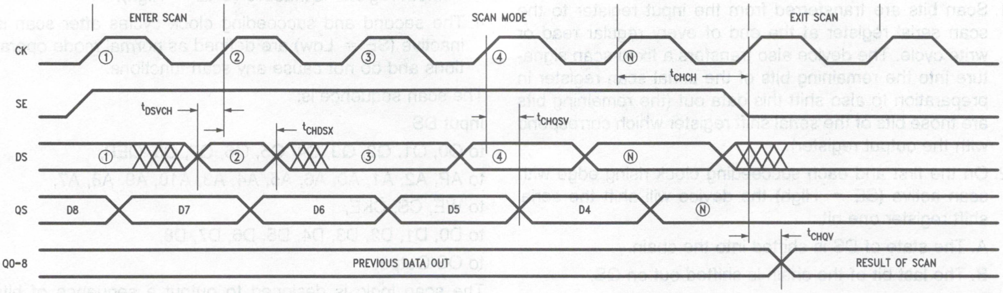
T_C = 0°C to +75°C. Input levels are −0.9V and −1.7V. Timing References are −1.3V (Note 1).

Symbol	Parameter	5 ns (Prelim)		7 ns Device		10 ns Device		Units
		Min	Max	Min	Max	Min	Max	
t_{CHCH}	Serial Scan Mode Cycle Time	5		7		10		ns
t_{DSVCH}	Serial Data Setup Time	0		0		0		ns
t_{CHDSX}	Serial Data Hold Time	2.0		2.5		3		ns
t_{CHQSV}	Serial Output Delay Time (Note 2)	2.5	5	2.5	7	2.5	10	ns

Output Load: 3.0 pF and 50Ω to −2.0V

Note 1: All maximum timing specs are referenced to the latter of CLK and $\overline{\text{CLK}}$, whichever occurs later. All minimum timing specs are referenced to the earlier of CLK and $\overline{\text{CLK}}$. CLK and $\overline{\text{CLK}}$ must cross each other between 10% and 90% of AC input levels.

Note 2: Maximum access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.



ENTER SCAN
SCAN MODE
EXIT SCAN
CK
SE
DS
QS
Q0–8
①
②
③
④
Ⓝ
t_{DSVCH}
t_{CHDSX}
t_{CHQSV}
t_{CHCH}
t_{CHQV}
D8
D7
D6
D5
D4
PREVIOUS DATA OUT
RESULT OF SCAN

TL/D/9748–8

National Semiconductor

PRELIMINARY

NM10E149
256 x 4-Bit ECL EPROM

General Description

The NM10E149 is a fully decoded high-speed 1024-bit ultraviolet Erasable and electrically Programmable Read Only Memory (EPROM) device, organized 256 words by four bits. This device is well suited for ECL logic replacement applications such as programmable decoders and arbitrary function elements. It is also very useful as high speed fixed control store memory for microcoded machines. The NM10E149 is voltage compensated and compatible with the 10K family. This device is enabled when $\overline{CS}$ is LOW. Prior to programming, all outputs are active HIGH in the enabled state. Programmed bits will furnish LOW levels at corresponding outputs. When the device is disabled ($\overline{CS}$ is HIGH) all outputs are LOW.

The NM10E149 has easy TTL compatible programming and verify modes. Programming occurs when V_{PP} is at 12.5V and $\overline{CS}$ is at a TTL LOW. Verify occurs when V_{PP} and $\overline{CS}$ are at a TTL LOW.

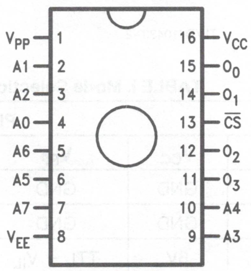
The enhanced testability provided by the erasable technology of the NM10E149 ensures that only the highest quality product leaves the factory. Users, as a result, save significantly in cost and time relative to currently available bipolar fuse link PROM alternatives. These conventional one-time-programmable devices must rely on special test bits outside the main memory array to verify programmability and adherence to parametric specifications. Consequently, users must bear the burden of yield loss at programming due to untested bad bits and then must employ expensive and time consuming parametric tests (and again suffer yield loss) after programming. Instead, with the NM10E149, the entire memory array is tested at the factory for programmability, followed by complete DC and AC parametric tests performed using data stored in the actual memory array, which is especially critical for these speed sensitive ECL devices. This way, users are assured optimum programming yield and can minimize post-programming parametric tests. The NM10E149's advanced technology and innovative design present a clear choice for high performance with low cost of ownership.

Features

- BiCMOS III process
- Fast address access time 5 ns, 7 ns, 10 ns max
- Operating power: 730 mW max, 500 mW typ
- Compatible with 10K ECL
- U.V. erasable
- Eraseable cell technology allows complete testing—ensuring superior quality
- Open-emitter outputs for memory expansion
- Standard 16-pin dual-in-line package
- Full address decoding on chip
- CMOS EPROM compatible programming
- NM10E149 power supply = −5.2V ±5%

Connection Diagram

Dual-In-Line Package

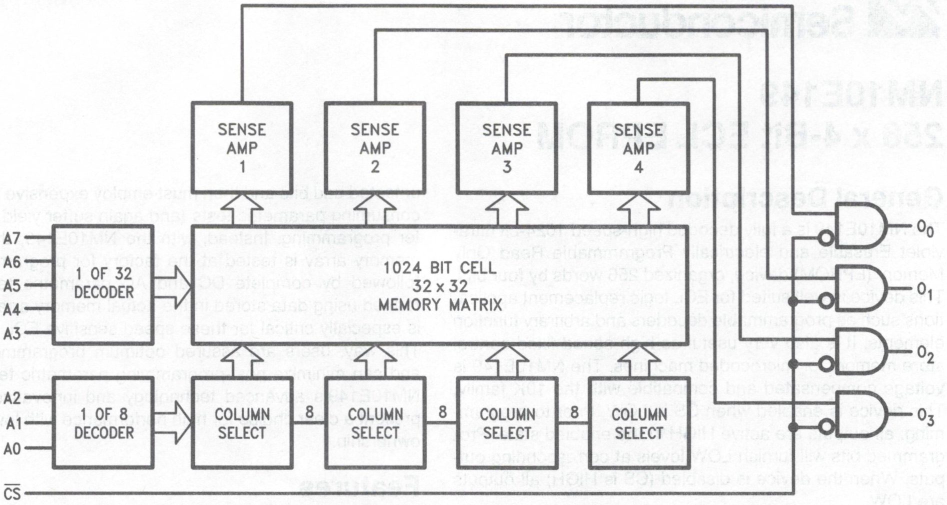


TL/D/10433-1

Pin Names

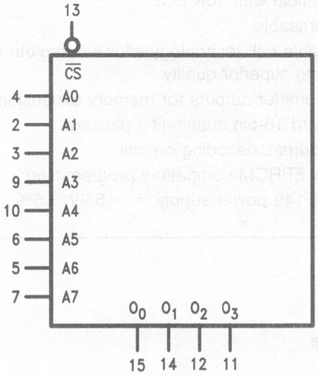
$\overline{CS}$	Chip Select Input
A_0–A_7	Address Inputs
O_0–O_3	Data Outputs

Logic Diagram


SENSE AMP 1
SENSE AMP 2
SENSE AMP 3
SENSE AMP 4
A7
A6
A5
A4
A3
1 OF 32 DECODER
1024 BIT CELL 32 x 32 MEMORY MATRIX
A2
A1
A0
1 OF 8 DECODER
COLUMN SELECT
8
COLUMN SELECT
8
COLUMN SELECT
8
COLUMN SELECT
CS
O0
O1
O2
O3

TL/D/10433-3

Logic Symbol


13
CS
4
A0
2
A1
3
A2
9
A3
10
A4
6
A5
5
A6
7
A7
O0
O1
O2
O3
15
14
12
11

TL/D/10433-2

Functional Description

The NM10E149 is a fully decoded BiCMOS erasable programmable read only memory organized 256 words by four bits per word. Word selection is achieved by means of an 8-bit address, A0 through A7. As in conventional ROM operation, the chip is selected, a binary address is applied to A0 through A7, and data is valid at the outputs after TAVQV.

DEVICE OPERATION

The six modes of operation of the NM10E149 are listed in Table I. For the read mode with 10K ECL levels, V_{CC} and V_{PP} are grounded and V_{EE} is supplied at a nominal −5.2V. In the programming and verify modes with TTL I/O levels, V_{EE} is tied to ground, V_{CC} is supplied at 6.0V, and V_{PP} swings from a TTL LOW to 12.5V.

TABLE I. Mode Selection

Mode	Pin				
	V_{EE}	V_{CC}	V_{PP}	$\overline{CS}$	Outputs
ECL Read	−5.2V	GND	GND	ECL − V_{IL}	ECL Data Out
ECL Deselect	−5.2V	GND	GND	ECL − V_{IH}	ECL − V_{OL}
TTL Verify	GND	6V	TTL − V_{IL}	TTL − V_{IL}	TTL Data Out
TTL Deselect	GND	6V	TTL − V_{IL}	TTL − V_{IH}	TRI-STATE
Program	GND	6V	12.5V	TTL − V_{IL}	TTL Data In
Program Inhibit	GND	6V	12.5V	TTL − V_{IH}	TRI-STATE

Functional Description (Continued)

ECL Read Mode

In the ECL read mode, the device's outputs are enabled when $\overline{CS}$ is LOW. When disabled ($\overline{CS}$ HIGH), all outputs are forced LOW.

An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications, such as memory expansion, the outputs of many NM10E149 devices can be tied together in a wired-OR. For large memories using this arrangement, the fast chip select access time permits the decoding of $\overline{CS}$ from the address without increasing address access time.

Regardless of the output configuration, an external 50Ω termination resistor to −2V, or an equivalent network, must be used to provide a LOW at the output.

TTL PROGRAMMING

CAUTION: Exceeding 13V on pin 1 (V_{PP}) will damage the NM10E149.

Initially and after each erasure, all bits of the NM10E149 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NM10E149 is in the programming mode when the V_{PP} power supply is at 12.5V. To prevent damage to the device, V_{CC} should be stable at 6V before applying the 12.5V, and V_{PP} should have a maximum of 0.25V of overshoot when switching. Before V_{PP} is supplied with the high voltage, the data output bus must be in a high impedance mode. This requirement prevents bus driver conflicts when, during V_{PP}'s ramp to 12.5V, the device momentarily passes through the ECL read mode with outputs enabled. After V_{PP} has reached 12.5V and is stable, the data to be programmed is applied four bits in parallel to the data output pins.

When the address and data are at stable TTL levels, an active LOW TTL program pulse is applied to the $\overline{CS}$ input. A program pulse must be applied to each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NM10E149 is designed to be programmed interactively, where each address programs with a series of 1.0 ms pulses until it verifies. The NM10E149 must not be programmed with a DC signal applied to the $\overline{CS}$ input.

Programming multiple NM10E149's in parallel with the same data can easily be accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NM10E149's may be connected together when they are programmed with the same data. A LOW level TTL pulse applied to the $\overline{CS}$ input programs the paralleled devices.

TTL Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify mode is attained when V_{PP} is at a TTL LOW and the outputs are enabled by $\overline{CS}$ being at a TTL LOW level.

ERASURE CHARACTERISTICS

The erasure characteristics of the NM10E149 are such that erasure begins to occur when the device is exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the (3000Å–4000Å) range.

After programming, opaque labels should be placed over the NM10E149 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NM10E149 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intenisty × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NM10E149 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NM10E149 erasure time for various light intensities.

TABLE II. Minimum NM10E149 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated supply transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between supply and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between supply and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +125°C
Maximum Junction Temperature	+125°C Max
Case Temperature under Bias	0°C to +85°C
Supply Voltage Range (V_{CC}–V_{EE})	−0.5V to +7V
V_{PP} w.r.t. V_{EE} ($4.2V \leq V_{CC} \leq 6.25V$)	−0.5V to +13.0V
Input Voltage	$V_{EE} - 0.5V$ to $V_{CC} + 0.5V$
Output Current (ECL Mode)	−50 mA Max
Output Current (TTL Mode)	±60 mA

Operating Conditions

ECL Operating Range	$V_{EE} = -5.46V$ to $-4.94V$
ECL Temperature Range	$T_C = 0°C$ to $+75°C$
TTL Operating Range	$V_{CC} = 4.2V$ to $6.25V$
TTL Temperature Range	$T_C = 20°C$ to $30°C$

ECL Read Operation

DC Electrical Characteristics $V_{EE} = -5.2V$, $V_{CC} = V_{PP} = $ GND, $T_C = 0°C$ to $+75°C$

Symbol	Parameter	Conditions		T_C	Min	Max	Units
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$	Loading is 50Ω to −2V	0°C	−1000	−840	mV
				+25°C	−960	−810	
				+75°C	−900	−720	
V_{OL}	Output LOW Voltage			0°C	−1870	−1665	mV
				+25°C	−1850	−1650	
				+75°C	−1830	−1625	
V_{OHC}	Output HIGH Voltage	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$		0°C	−1020		mV
				+25°C	−980		
				+75°C	−920		
V_{OLC}	Output LOW Voltage			0°C		−1645	mV
				+25°C		−1630	
				+75°C		−1605	
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage HIGH for All Inputs		0°C	−1145	−840	mV
				+25°C	−1105	−810	
				+75°C	−1045	−720	
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage LOW for All Inputs		0°C	−1870	−1490	mV
				+25°C	−1850	−1475	
				+75°C	−1830	−1450	
I_{IL}	Input LOW Current	$V_{IN} = V_{IL(Min)}$			−50	170	μA
I_{IH}	Input HIGH Current All Inputs	$V_{IN} = V_{IH(Max)}$				220	μA
I_{EE}	Power Supply Current	Inputs and Outputs Open			−140		mA

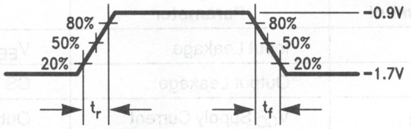
AC Electrical Characteristics V_{EE} −5.2V ±5%, $V_{CC} = V_{PP} = $ GND, $T_C = 0°C$ to $+75°C$

Symbol	Parameter	−5		−7		−10		Units
		Min	Max	Min	Max	Min	Max	
TAVQV	Address Access Time		5		7		10	ns
TAXQX	Address Change to Output Change	1.0		1.0		1.0		ns
TSLQV	Chip Select Access		4		5		6	ns
TSHQL	$\overline{CS}$ to Output Disable		3		4		5	ns
TSHQX	$\overline{CS}$ High to Output Change	0		0		0		ns

ECL Read Operation (Continued)

AC Test Conditions

Input Pulse Levels	*Figure 1*
Input Rise and Fall Times	0.7 ns
Output Timing Reference Levels	50% of Input
AC Test Circuit	*Figure 2*


80%
50%
20%
80%
50%
20%
-0.9V
-1.7V
t_r
t_f

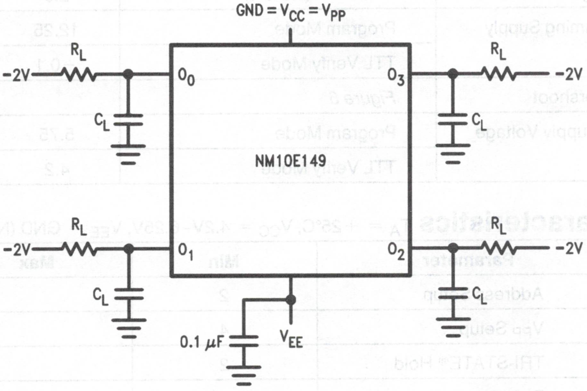
TL/D/10433-6

t_r = Rise Time

t_f = Fall Time

50% = Timing Reference Levels

FIGURE 1. Input Levels


GND = V_{CC} = V_{PP}
R_L
-2V
O_0
C_L
O_3
R_L
-2V
C_L
NM10E149
R_L
-2V
O_1
C_L
O_2
R_L
-2V
C_L
0.1 µF
V_{EE}

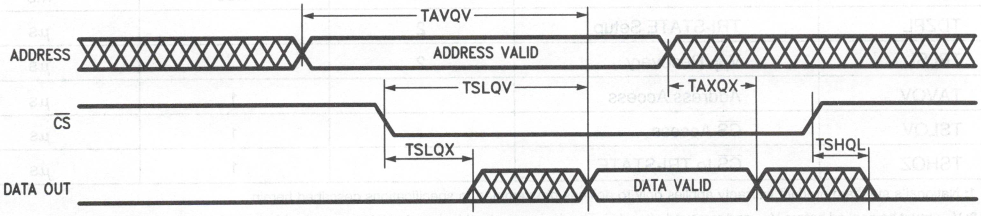
TL/D/10433-7

Notes:

$C_L \leq 5$ pF including Fixture and Stray Capacitance

$R_L = 50\Omega$ to $-2.0V$

FIGURE 2. AC Test Circuit


TAVQV
ADDRESS
ADDRESS VALID
TAXQX
TSLQV
CS
TSLQX
TSHQL
DATA OUT
DATA VALID

TL/D/10433-5

FIGURE 3. ECL Read Cycle

TTL Programming/Verify Operation (Notes 1, 2, 3)

DC Characteristics $T_A = +25°C, V_{CC} = 4.2V–6.25V, V_{EE} = GND$

Symbol	Parameter	Conditions	Min	Max	Units
I_{LI}	Input Leakage	$V_{EE} \leq V_{IN} \leq V_{CC}$		±100	μA
I_{LO}	Output Leakage	$CS = V_{IH}, V_{EE} \leq V_{IN} \leq V_{CC}$		±100	μA
I_{CC}	V_{CC} Supply Current	Outputs Open		140	mA
I_{PP}	V_{PP} Supply Current			30	mA
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA (Note 4)		0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA (Note 4)	2.4		V
V_{IL}	Input Low Level	(Note 4)	−0.1	0.8	V
V_{IH}	Input High Level	(Note 4)	2.0	V_{CC}	V
V_{PP}	Programming Supply Voltage	Program Mode	12.25	12.75	V
		TTL Verify Mode	−0.1	0.8	
V_{PPOS}	V_{PP} Overshoot	*Figure 6*		0.25	V
V_{CC}	Power Supply Voltage	Program Mode	5.75	6.25	V
		TTL Verify Mode	4.2	6.25	

AC Electrical Characteristics $T_A = +25°C, V_{CC} = 4.2V–6.25V, V_{EE} = GND$ (Notes 1,2,3,4)

Symbol	Parameter	Min	Max	Units
TAVSL	Address Setup	2		μs
TPHSL	V_{PP} Setup	4		μs
TPHDV	TRI-STATE® Hold	2		μs
TDVSL	Data Setup	2		μs
TSHAX	Address Hold	0		μs
TSHPL	V_{PP} Hold	4		μs
TSHDX	Data Hold	2		μs
TSLSH	$\overline{CS}$ Pulse Width	0.8	1.05	ms
TDZPL	TRI-STATE Setup	2		μs
TPLSL	V_{PP} Recovery	2		μs
TAVQV	Address Access		1	μs
TSLQV	$\overline{CS}$ Access		1	μs
TSHQZ	$\overline{CS}$ to TRI-STATE		1	μs

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied before V_{PP} and removed after V_{PP}. The device must not be inserted into or removed from a socket with voltage applied to V_{PP} or V_{CC}.

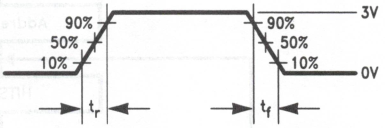
Note 3: The absolute maximum voltage which may be applied to the V_{PP} pin during programming is 13V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding the 13V maximum specification. At least a 0.1 μF capacitor is required to decouple V_{PP} and V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: These parameters are sampled only, and are not 100% tested.

TTL Programming/Verify Operation (Continued)

AC Test Conditions

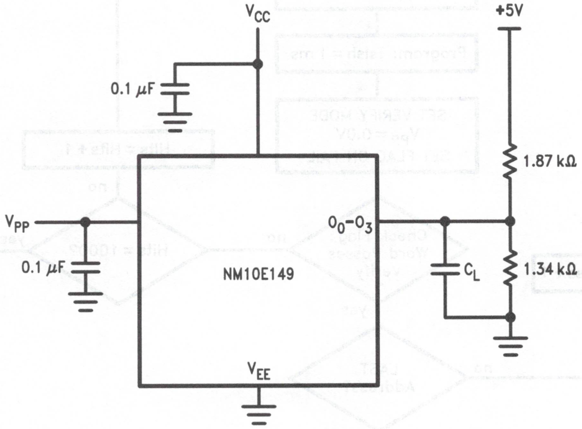
Input Pulse Levels	*Figure 4*
Input Rise and Fall Times	3 ns
Output Timing Reference Levels	50% of Input
AC Test Circuit	*Figure 5*


3V
0V
90%
50%
10%
90%
50%
10%
t_r
t_f

TL/D/10433-9

t_r = Rise Time
t_f = Fall Time
50% = Timing Reference Levels

FIGURE 4. Input Levels


V_{CC}
+5V
0.1 µF
1.87 kΩ
V_{PP}
O_0–O_3
0.1 µF
NM10E149
C_L
1.34 kΩ
V_{EE}

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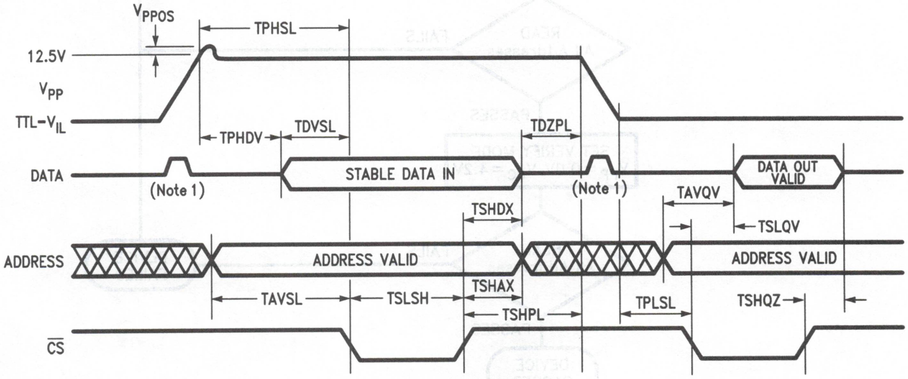
Notes: C_L = 30 pF including fixture and stray capacitance

FIGURE 5. AC Test Circuit


V_{PPOS}
TPHSL
12.5V
V_{PP}
TTL-V_{IL}
TPHDV
TDVSL
TDZPL
DATA
STABLE DATA IN
DATA OUT VALID
(Note 1)
(Note 1)
TAVQV
TSHDX
TSLQV
ADDRESS
ADDRESS VALID
ADDRESS VALID
TSHAX
TAVSL
TSLSH
TPLSL
TSHQZ
TSHPL
CS

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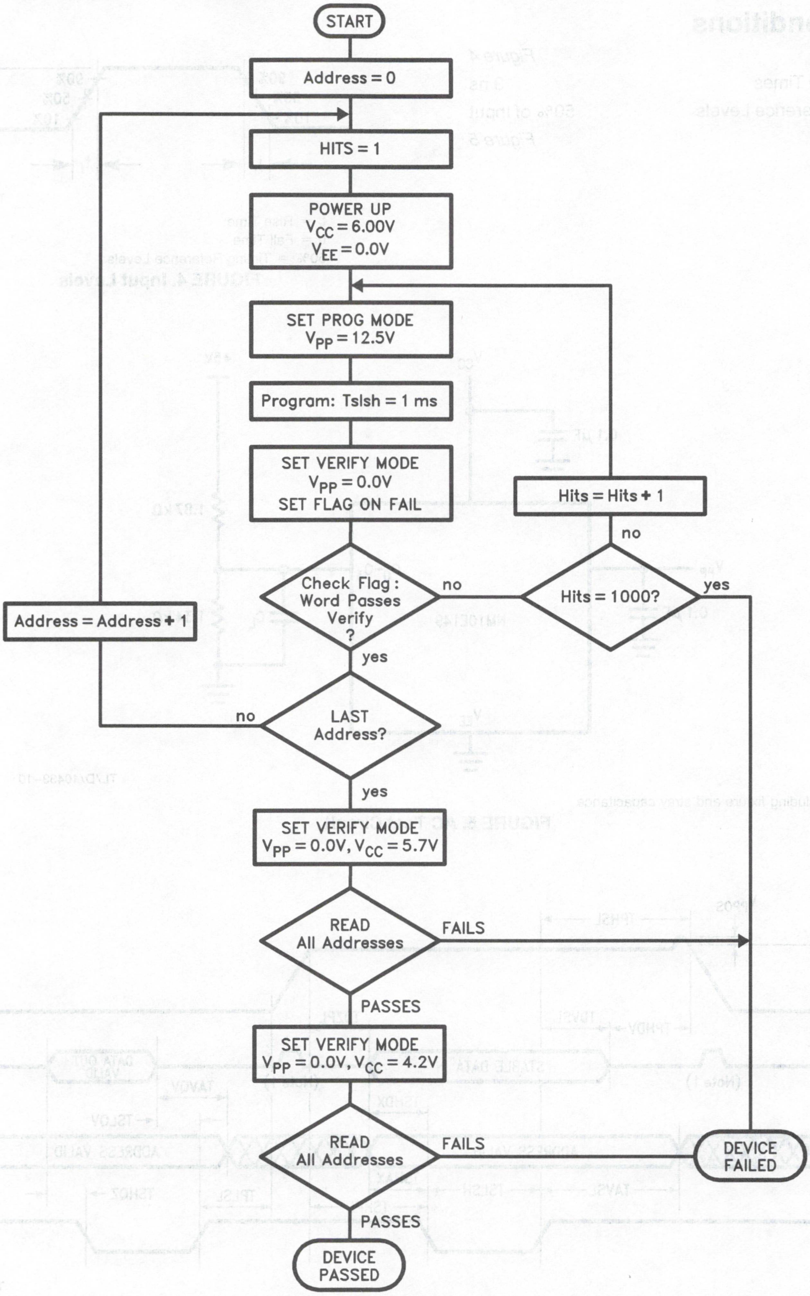
Note 1: When V_{PP} is transitioning between its low and high voltage, the device passes through the ECL read mode, with the ECL outputs enabled and driving the equivalent of a TTL HIGH.

FIGURE 6. TTL Programming/Verify Cycle

Programming/Verify Algorithm


START
Address = 0
HITS = 1
POWER UP
V_{CC} = 6.00V
V_{EE} = 0.0V
SET PROG MODE
V_{PP} = 12.5V
Program: Tslsh = 1 ms
SET VERIFY MODE
V_{PP} = 0.0V
SET FLAG ON FAIL
Hits = Hits + 1
no
Check Flag: Word Passes Verify ?
no
Hits = 1000?
yes
Address = Address + 1
yes
no
LAST Address?
yes
SET VERIFY MODE
V_{PP} = 0.0V, V_{CC} = 5.7V
READ All Addresses
FAILS
PASSES
SET VERIFY MODE
V_{PP} = 0.0V, V_{CC} = 4.2V
READ All Addresses
FAILS
DEVICE FAILED
PASSES
DEVICE PASSED

TL/D/10433–4

National Semiconductor

PRELIMINARY

NM100E149
256 x 4-Bit ECL EPROM

General Description

The NM100E149 is a fully decoded high-speed 1024-bit ultraviolet Erasable and electrically Programmable Read Only Memory (EPROM) device, organized 256 words by four bits. This device is well suited for ECL logic replacement applications such as programmable decoders and arbitrary function elements. It is also very useful as high speed fixed control store memory for microcoded machines. The NM100E149 is voltage and temperature compensated and compatible with the 100K family. This device is enabled when $\overline{CS}$ is LOW. Prior to programming, all outputs are active HIGH in the enabled state. Programmed bits will furnish LOW levels at corresponding outputs. When the device is disabled ($\overline{CS}$ is HIGH) all outputs are LOW.

The NM100E149 has easy TTL compatible programming and verify modes. Programming occurs when V_{PP} is at 12.5V and $\overline{CS}$ is at a TTL LOW. Verify occurs when V_{PP} and $\overline{CS}$ are at a TTL LOW.

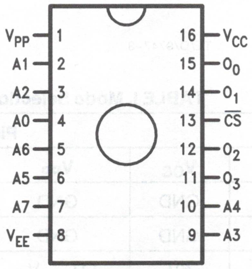
The enhanced testability provided by the erasable technology of the NM100E149 ensures that only the highest quality product leaves the factory. Users, as a result, save significantly in cost and time relative to currently available bipolar fuse link PROM alternatives. These conventional one-time-programmable devices must rely on special test bits outside the main memory array to verify programmability and adherence to parametric specifications. Consequently, users must bear the burden of yield loss at programming due to untested bad bits and then must employ expensive and time consuming parametric tests (and again suffer yield loss) after programming. Instead, with the NM100E149, the entire memory array is tested at the factory for programmability, followed by complete DC and AC parametric tests performed using data stored in the actual memory array, which is especially critical for these speed sensitive ECL devices. This way, users are assured optimum programming yield and can minimize post-programming parametric tests. The NM100E149's advanced technology and innovative design present a clear choice for high performance with low cost of ownership.

Features

- BiCMOS III process
- Fast address access time 5 ns, 7 ns, 10 ns max
- Operating power: 730 mW max, 500 mW typ
- Compatible with 100K ECL
- U.V. erasable
- Eraseable cell technology allows complete testing—ensuring superior quality
- Open-emitter outputs for memory expansion
- Standard 16-pin dual-in-line package
- Full address decoding on chip
- CMOS EPROM compatible programming
- NM100E149 power supply = −4.2V to −4.8V

Connection Diagram

Dual-In-Line Package

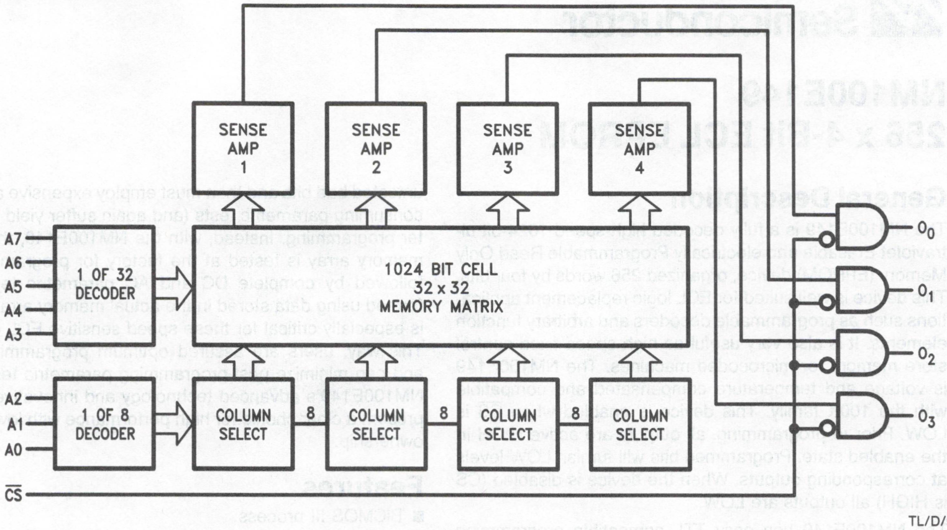


TL/D/9747-1

Pin Names

$\overline{CS}$	Chip Select Input
A_0–A_7	Address Inputs
O_0–O_3	Data Outputs

Logic Diagram


SENSE AMP 1
SENSE AMP 2
SENSE AMP 3
SENSE AMP 4
A7
A6
A5
A4
A3
1 OF 32 DECODER
1024 BIT CELL 32 x 32 MEMORY MATRIX
A2
A1
A0
1 OF 8 DECODER
COLUMN SELECT
8
COLUMN SELECT
8
COLUMN SELECT
8
COLUMN SELECT
$\overline{CS}$
O_0
O_1
O_2
O_3

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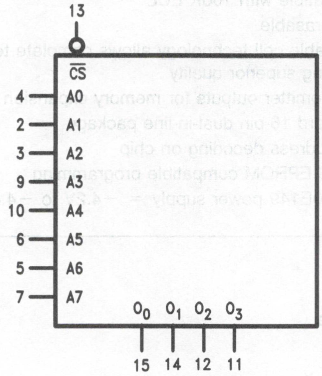
Logic Symbol


13
$\overline{CS}$
4
A0
2
A1
3
A2
9
A3
10
A4
6
A5
5
A6
7
A7
O_0
O_1
O_2
O_3
15
14
12
11

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Functional Description

The NM100E149 is a fully decoded BiCMOS erasable programmable read only memory organized 256 words by four bits per word. Word selection is achieved by means of an 8-bit address, A0 through A7. As in conventional ROM operation, the chip is selected, a binary address is applied to A0 through A7, and data is valid at the outputs after TAVQV.

DEVICE OPERATION

The six modes of operation of the NM100E149 are listed in Table I. For the read mode with 100K ECL levels, V_{CC} and V_{PP} are grounded and V_{EE} is supplied at a nominal −4.5V. In the programming and verify modes with TTL I/O levels, V_{EE} is tied to ground, V_{CC} is supplied at 6.0V, and V_{PP} swings from a TTL LOW to 12.5V.

TABLE I. Mode Selection

Mode	Pin				
	V_{EE}	V_{CC}	V_{PP}	$\overline{CS}$	Outputs
ECL Read	−4.5V	GND	GND	ECL − V_{IL}	ECL Data Out
ECL Deselect	−4.5V	GND	GND	ECL − V_{IH}	ECL − V_{OL}
TTL Verify	GND	6V	TTL − V_{IL}	TTL − V_{IL}	TTL Data Out
TTL Deselect	GND	6V	TTL − V_{IL}	TTL − V_{IH}	TRI-STATE
Program	GND	6V	12.5V	TTL − V_{IL}	TTL Data In
Program Inhibit	GND	6V	12.5V	TTL − V_{IH}	TRI-STATE

Functional Description (Continued)

ECL Read Mode

In the ECL read mode, the device's outputs are enabled when $\overline{CS}$ is LOW. When disabled ($\overline{CS}$ HIGH), all outputs are forced LOW.

An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications, such as memory expansion, the outputs of many NM100E149 devices can be tied together in a wired-OR. For large memories using this arrangement, the fast chip select access time permits the decoding of $\overline{CS}$ from the address without increasing address access time.

Regardless of the output configuration, an external 50Ω termination resistor to −2V, or an equivalent network, must be used to provide a LOW at the output.

TTL PROGRAMMING

CAUTION: Exceeding 13V on pin 1 (V_{PP}) will damage the NM10E149.

Initially and after each erasure, all bits of the NM10E149 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NM100E149 is in the programming mode when the V_{PP} power supply is at 12.5V. To prevent damage to the device, V_{CC} should be stable at 6V before applying the 12.5V, and V_{PP} should have a maximum of 0.25V of overshoot when switching. Before V_{PP} is supplied with the high voltage, the data output bus must be in a high impedance mode. This requirement prevents bus driver conflicts when, during V_{PP}'s ramp to 12.5V, the device momentarily passes through the ECL read mode with outputs enabled. After V_{PP} has reached 12.5V and is stable, the data to be programmed is applied four bits in parallel to the data output pins.

When the address and data are at stable TTL levels, an active LOW TTL program pulse is applied to the $\overline{CS}$ input. A program pulse must be applied to each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NM100E149 is designed to be programmed interactively, where each address programs with a series of 1.0 ms pulses until it verifies. The NM100E149 must not be programmed with a DC signal applied to the $\overline{CS}$ input.

Programming multiple NM100E149's in parallel with the same data can easily be accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NM10E149's may be connected together when they are programmed with the same data. A LOW level TTL pulse applied to the $\overline{CS}$ inputs programs the paralleled devices.

TTL Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify mode is attained when V_{PP} is at a TTL low and the outputs are enabled by $\overline{CS}$ being at a TTL low level.

ERASURE CHARACTERISTICS

The erasure characteristics of the NM100E149 are such that erasure begins to occur when the device is exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the (3000Å–4000Å) range.

After programming, opaque labels should be placed over the NM100E149 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NM100E149 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intenisty × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NM100E149 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NM100E149 erasure time for various light intensities.

TABLE II. Minimum NM100E149 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated supply transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between supply and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between supply and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +125°C
Maximum Junction Temperature	+125°C Max
Case Temperature under Bias	0°C to +95°C
Supply Voltage Range (V_{CC}–V_{EE})	−0.5V to +7V
V_{PP} w.r.t. V_{EE} ($4.2V \leq V_{CC} \leq 6.25V$)	−0.5V to +13.0V
Input Voltage	V_{EE} − 0.5V to V_{CC} + 0.5V
Output Current (ECL Mode)	−50 mA Max
Output Current (TTL Mode)	±60 mA

Operating Conditions

ECL Operating Range	V_{EE} = −4.8V to −4.2V
ECL Temperature Range	T_C = 0°C to +85°C
TTL Operating Range	V_{CC} = 4.2V to 6.25V
TTL Temperature Range	T_C = 20°C to 30°C

ECL Read Operation

DC Electrical Characteristics: V_{EE} = −4.8V to −4.2V, V_{CC} = V_{PP} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Parameter	Min	Typ	Max	Unit	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (max)}$ or $V_{IL\ (min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605	mV		
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$	
V_{OLC}	Output LOW Voltage			−1595	mV		
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	−50		170	µA	V_{IN} = $V_{IL\ (min)}$	
I_{IH}	Input HIGH Current All Inputs			220	µA	V_{IN} = $V_{IH\ (max)}$	
I_{EE}	Inputs and Outputs Open	−140			mA		

DC Characteristics: V_{EE} = −4.5V, V_{CC} = V_{PP} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Parameter	Min	Typ	Max	Unit	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025		−880	mV	V_{IN} = $V_{IH\ (max)}$ or $V_{IL\ (min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	50		170	µA	V_{IN} = $V_{IL\ (min)}$	
I_{IH}	Input HIGH Current All Inputs			220	µA	V_{IN} = $V_{IH\ (max)}$	
I_{EE}	Inputs and Outputs Open	−140			mA		

DC Characteristics: $V_{EE} = -4.8V$, $V_{CC} = V_{PP} = GND$, $T_C = 0°C$ to $+85°C$, Note 3

Symbol	Parameter	Min	Typ	Max	Unit	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	$V_{IN} = V_{IH\ (max)}$ or $V_{IL\ (min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620	mV		
V_{OHC}	Output HIGH Voltage	−1045			mV	$V_{IN} = V_{IH\ (min)}$ or $V_{IL\ (max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
I_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	−50		170	μA	$V_{IN} = V_{IL\ (min)}$	
I_{IH}	Input HIGH Current All Inputs			220	μA	$V_{IN} = V_{IH\ (max)}$	
I_{EE}	Inputs and Outputs Open	−140			mA		

Note 1: Unless specified otherwise on individual data sheet.

Note 2: Parametric values specified at −4.2V to −4.8V

Note 3: The specified limits represent the "worst case" value for the parameter since these "worst case" values normally occur at the temperature extremes additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

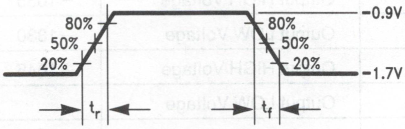
AC Electrical Characteristics $V_{EE} = -4.8V$ to $-4.2V$, $V_{CC} = V_{PP} = GND$, $T_C = 0°C$ to $+85°C$

Symbol	Parameter	−5		−7		−10		Units
		Min	Max	Min	Max	Min	Max	
TAVQV	Address Access Time		5		7		10	ns
TAXQX	Address Change to Output Change	1.0		1.0		1.0		ns
TSLQV	Chip Select Access		4		5		6	ns
TSHQL	$\overline{CS}$ to Output Disable		3		4		5	ns
TSHQX	$\overline{CS}$ High to Output Change	0		0		0		ns

ECL Read Operation (Continued)

AC Test Conditions

Input Pulse Levels	*Figure 1*
Input Rise and Fall Times	0.7 ns
Output Timing Reference Levels	50% of Input
AC Test Circuit	*Figure 2*


80%
50%
20%
t_r
80%
50%
20%
t_f
−0.9V
−1.7V

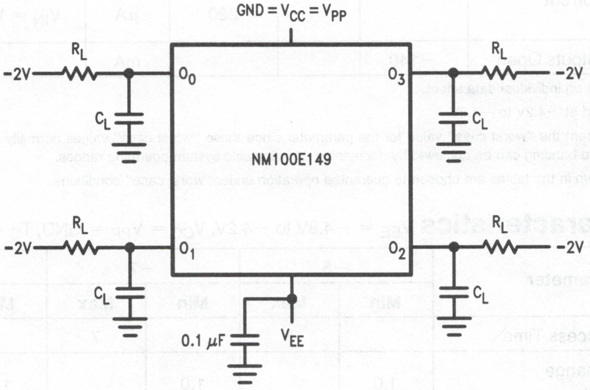
TL/D/9747–4

t_r = Rise Time

t_f = Fall Time

50% = Timing Reference Levels

FIGURE 1. Input Levels


GND = V_CC = V_PP
R_L
−2V
O_0
C_L
R_L
−2V
O_3
C_L
NM100E149
R_L
−2V
O_1
C_L
R_L
−2V
O_2
C_L
0.1 μF
V_EE

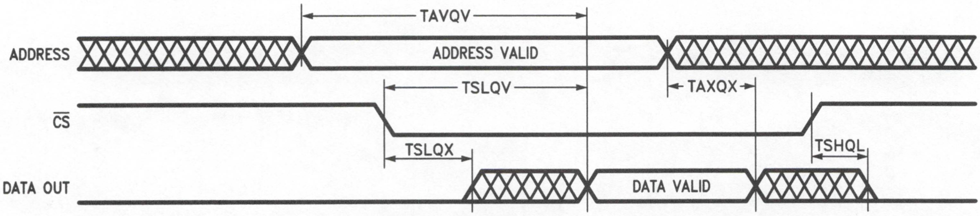
TL/D/9747–5

Notes:

$C_L \leq 5$ pF including Fixture and Stray Capacitance

$R_L = 50\Omega$ to $-2.0V$

FIGURE 2. AC Test Circuit


TAVQV
ADDRESS
ADDRESS VALID
TSLQV
TAXQX
CS
TSLQX
TSHQL
DATA OUT
DATA VALID

TL/D/9747–6

FIGURE 3. ECL Read Cycle

TTL Programming/Verify Operation (Notes 1, 2, and 3)

DC Characteristics $T_A = +25°C$, $V_{CC} = 4.2V–6.25V$, $V_{EE} = GND$

Symbol	Parameter	Conditions	Min	Max	Units
I_{LI}	Input Leakage	$V_{EE} \le V_{IN} \le V_{CC}$		±100	μA
I_{LO}	Output Leakage	$CS = V_{IH}, V_{EE} \le V_{IN} \le V_{CC}$		±100	μA
I_{CC}	V_{CC} Supply Current	Outputs Open		140	mA
I_{PP}	V_{PP} Supply Current			30	mA
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA (Note 4)		0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA (Note 4)	2.4		V
V_{IL}	Input Low Level	(Note 4)	−0.1	0.8	V
V_{IH}	Input High Level	(Note 4)	2.0	V_{CC}	V
V_{PP}	Programming Supply Voltage	Program Mode	12.25	12.75	V
		TTL Verify Mode	−0.1	0.8	
V_{PPOS}	V_{PP} Overshoot	*Figure 6*		0.25	V
V_{CC}	Power Supply Voltage	Program Mode	5.75	6.25	V
		TTL Verify Mode	4.2	6.25	

AC Electrical Characteristics $T_A = +25°C$, $V_{CC} = 4.2V–6.25V$, $V_{EE} = GND$ (Notes 1, 2, 3, and 4)

Symbol	Parameter	Min	Max	Units
TAVSL	Address Setup	2		μs
TPHSL	V_{PP} Setup	4		μs
TPHDV	TRI-STATE® Hold	2		μs
TDVSL	Data Setup	2		μs
TSHAX	Address Hold	0		μs
TSHPL	V_{PP} Hold	4		μs
TSHDX	Data Hold	2		μs
TSLSH	$\overline{CS}$ Pulse Width	0.8	1.05	ms
TDZPL	TRI-STATE Setup	2		μs
TPLSL	V_{PP} Recovery	2		μs
TAVQV	Address Access		1	μs
TSLQV	$\overline{CS}$ Access		1	μs
TSHQZ	$\overline{CS}$ to TRI-STATE		1	μs

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied before V_{PP} and removed after V_{PP}. The device must not be inserted into or removed from a socket with voltage applied to V_{PP} or V_{CC}.

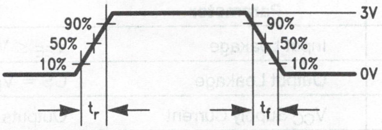
Note 3: The absolute maximum voltage which may be applied to the V_{PP} pin during programming is 13V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding the 13V maximum specification. At least a 0.1 μF capacitor is required to decouple V_{PP} and V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: These parameters are sampled only, and are not 100% tested.

TTL Programming/Verify Operation (Continued)

AC Test Conditions

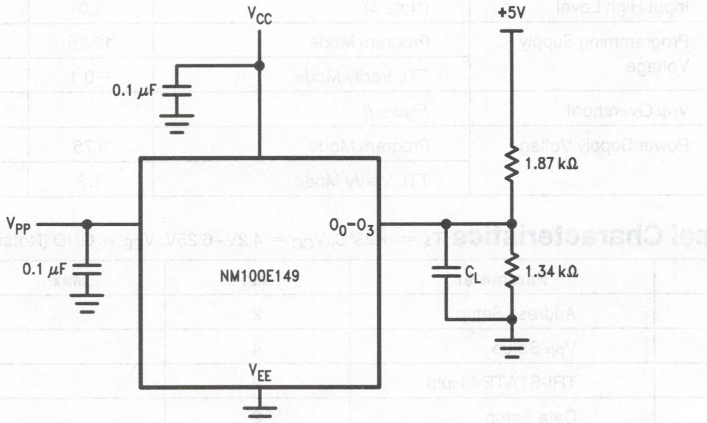
Input Pulse Levels	*Figure 4*
Input Rise and Fall Times	3 ns
Output Timing Reference Levels	50% of Input
AC Test Circuit	*Figure 5*


90%
50%
10%
3V
90%
50%
10%
0V
t_r
t_f

TL/D/9747-7

t_r = Rise Time
t_f = Fall Time
50% = Timing Reference Levels

FIGURE 4. Input Levels


V_{CC}
0.1 µF
+5V
1.87 kΩ
V_{PP}
0.1 µF
O_0–O_3
NM100E149
C_L
1.34 kΩ
V_{EE}

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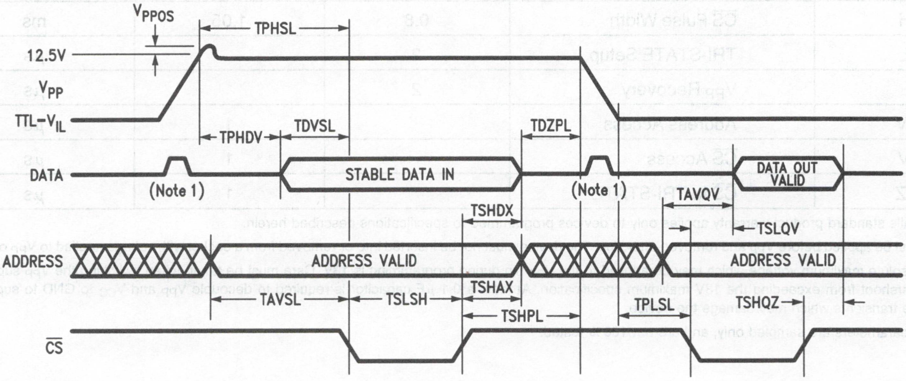
Notes: C_L = 30 pF including fixture and stray capacitance

FIGURE 5. AC Test Circuit


V_{PPOS}
TPHSL
12.5V
V_{PP}
TTL-V_{IL}
TPHDV
TDVSL
TDZPL
DATA
(Note 1)
STABLE DATA IN
(Note 1)
DATA OUT VALID
TSHDX
TAVQV
TSLQV
ADDRESS
ADDRESS VALID
ADDRESS VALID
TAVSL
TSLSH
TSHAX
TPLSL
TSHQZ
TSHPL
$\overline{CS}$

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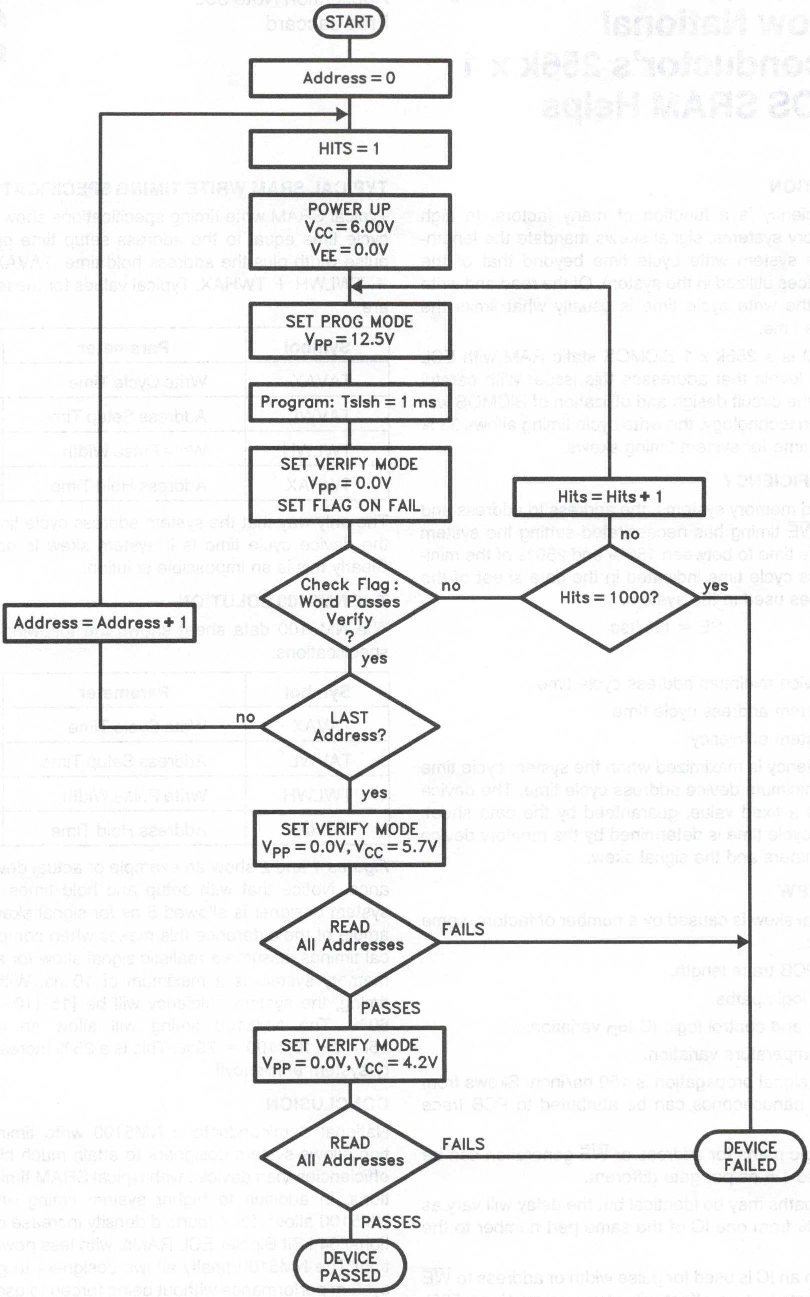
Note 1: When V_{PP} is transitioning between its low and high voltage, the device passes through the ECL read mode, with the ECL outputs enabled and driving the equivalent of a TTL HIGH.

FIGURE 6. TTL Programming/Verify Cycle

Programming/Verify Algorithm


START
Address = 0
HITS = 1
POWER UP
$V_{CC} = 6.00V$
$V_{EE} = 0.0V$
SET PROG MODE
$V_{PP} = 12.5V$
Program: Tslsh = 1 ms
SET VERIFY MODE
$V_{PP} = 0.0V$
SET FLAG ON FAIL
Check Flag: Word Passes Verify ?
no
Hits = 1000?
no
Hits = Hits + 1
yes
yes
Address = Address + 1
LAST Address?
no
yes
SET VERIFY MODE
$V_{PP} = 0.0V, V_{CC} = 5.7V$
READ All Addresses
FAILS
PASSES
SET VERIFY MODE
$V_{PP} = 0.0V, V_{CC} = 4.2V$
READ All Addresses
FAILS
PASSES
DEVICE FAILED
DEVICE PASSED

TL/D/9747-10

Memory System Efficiency and How National Semiconductor's 256k x 1 BiCMOS SRAM Helps

National Semiconductor
Application Note 565
Fred Jaccard

INTRODUCTION

System efficiency is a function of many factors. In high speed memory systems, signal skews mandate the lengthening of the system write cycle time beyond that of the memory devices utilized in the system. Of the read and write cycle time, the write cycle time is usually what limits the system cycle time.

The NM5100 is a 256k x 1 BiCMOS static RAM with ECL input/output levels that addresses this issue. With careful attention to the circuit design and utilization of BiCMOS wafer fabrication technology, the write cycle timing allows 33% of the cycle time for system timing skews.

SYSTEM EFFICIENCY

In high speed memory systems, the address to address and address to $\overline{WE}$ timing has necessitated setting the system address cycle time to between 150% and 250% of the minimum address cycle time indicated in the data sheet of the SRAM devices used in the system.

$$SE = tdc/tsc$$

Where

tdc = device minimum address cycle time
tsc = system address cycle time
SE = system efficiency

System efficiency is maximized when the system cycle time equals the minimum device address cycle time. The device cycle time is a fixed value, guaranteed by the data sheet. The system cycle time is determined by the memory device timing parameters and the signal skew.

SYSTEM SKEW

System signal skew is caused by a number of factors, some of which are:

1. Unequal PCB trace length.
2. Dissimilar logic paths.
3. Bus driver and control logic IC t_{PD} variation.
4. System temperature variation.

Typical PCB signal propagation is 150 ps/inch. Skews from 0 to several nanoseconds can be attributed to PCB trace length.

Dissimilar logic paths for address or $\overline{WE}$ generation can be from 0.5 ns to 1.5 ns per gate different.

Signal logic paths may be identical but the delay will vary as much as 50% from one IC of the same part number to the next.

If t_{PD} through an IC is used for pulse width or address to $\overline{WE}$ timing, the temperature effect will cause as much as 50% variation in t_{PD}.

For high speed memory system design, careful attention must be given to these factors to minimize the signal skew seen at each memory device in the system.

TYPICAL SRAM WRITE TIMING SPECIFICATIONS

Typical SRAM write timing specifications show the address cycle time equal to the address setup time plus the write pulse width plus the address hold time. TAVAX = TAVWL + TWLWH + TWHAX. Typical values for these parameters are:

Symbol	Parameter	Min
TAVAX	Write Cycle Time	15
TAVWL	Address Setup Time	3
TWLWH	Write Pulse Width	10
TWHAX	Address Hold Time	2

The only way that the system address cycle time can equal the device cycle time is if system skew is equal to zero. Clearly this is an impossible solution.

THE NM5100 SOLUTION

The NM5100 data sheet shows the following write timing specifications:

Symbol	Parameter	Min
TAVAX	Write Cycle Time	15
TAVWL	Address Setup Time	0
TWLWH	Write Pulse Width	10
TWHAX	Address Hold Time	0

Figures 1 and *2* show an example of actual device performance. Notice that with setup and hold times of 0 ns, the system designer is allowed 5 ns for signal skew. As an example of the difference this makes when compared to typical timings, assume a realistic signal skew for a high speed memory system is a maximum of 10 ns. With the typical timing, the system efficiency will be [15/(10+15)]*10) = 60%. The NM5100 timing will allow an efficiency of 15/(10+10)*100 = 75%. This is a 25% increase in memory system efficiency!!

CONCLUSION

National Semiconductor's NM5100 write timing specification allows system designers to attain much higher system efficiencies than devices with typical SRAM timing specifications. In addition to higher system timing efficiency, the NM5100 allows for a fourfold density increase over conventional 64 kBit Bipolar ECL RAMs, with less power consumption! The NM5100 finally allows designers to go all out for system performance without being forced to use low-density SRAMs.

V_{EE} (V)

```
-7.000 V|............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-6.800 V|.............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-6.600 V|.............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-6.400 V|.............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-6.200 V|.............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-6.000 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-5.800 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-5.600 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-5.400 V|...............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-5.200 V|...............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-5.000 V|................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-4.800 V|................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-4.600 V|.................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-4.400 V|..................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-4.200 V|...................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-4.000 V|.....................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-3.800 V|...................................................
-3.600 V|...................................................
-3.400 V|...................................................
-3.200 V|...................................................
-3.000 V|...................................................
        ||||||||||||||||||||||||||||||||||||||||||||||||||||
       -5.0ns    -3.0ns    -1.0ns     1.0ns     3.0ns     5.0ns
                        (TWHAX1)
```

FIGURE 1. Address Hold Time vs Operating Supply Voltage

V_{EE} (V)

```
-7.000 V|.............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-6.800 V|.............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-6.600 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-6.400 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-6.200 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-6.000 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-5.800 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-5.600 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-5.400 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-5.200 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-5.000 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-4.800 V|..............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-4.600 V|...............PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-4.400 V|................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-4.200 V|..................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-4.000 V|......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP
-3.800 V|............................PPPPPPP................
-3.600 V|...................................................
-3.400 V|...................................................
-3.200 V|...................................................
-3.000 V|...................................................
        ||||||||||||||||||||||||||||||||||||||||||||||||||||
       -5.0ns    -3.0ns    -1.0ns     1.0ns     3.0ns     5.0ns
                        (TAVWL1)
```

FIGURE 2. Address Setup Time vs Operating Supply Voltage

National Semiconductor's BiCMOS III Process Is Latch-Up Immune

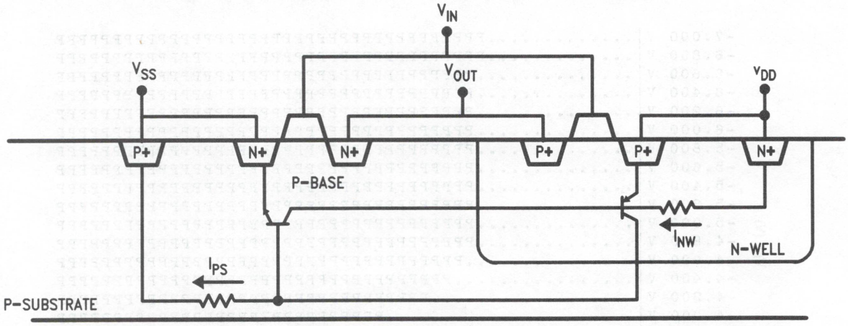
National Semiconductor
Application Note 566
Dave DiMarco

LATCH-UP AND CMOS

Latch-up is a well known and documented phenomena in CMOS technology.[1] It occurs when parasitic pnpn (or SCR) devices inherent in CMOS processes are turned on, and results in a high current, low impedance path between V_{DD} and V_{SS}. This can lead to permanent device damage or temporary nonfunctionality until the device is powered down.

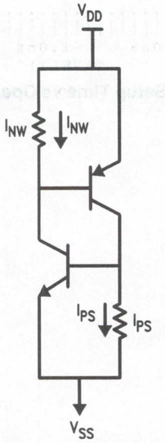
In N-well CMOS the pnpn path is the result of a parasitic lateral npn and a parasitic pnp transistor as shown in *Figures 1* and *2*. This structure has two stable states. In the first or the "blocking state" the emitter/base junctions are reverse biased and a high impedance path is maintained between V_{DD} and V_{SS}. In the second state, both emitter base junctions are forward biased, and a high current path between V_{DD} and V_{SS} is turned on.

In normal CMOS operation, this pnpn path is in its "blocking" state. It can, however, be switched into its "on" state if the lateral current I_{PS} and I_{NW} become large enough to forward bias the parasitic emitter base junctions. This can occur from: radiation currents, c dv/dt current resulting from voltage spikes across the n-well/substrate junction, avalanche multiplication currents at the n-well/substrate junction, or input over voltage conditions.[2]



TL/D/10091-1

FIGURE 1. Standard CMOS Process



TL/D/10091-2

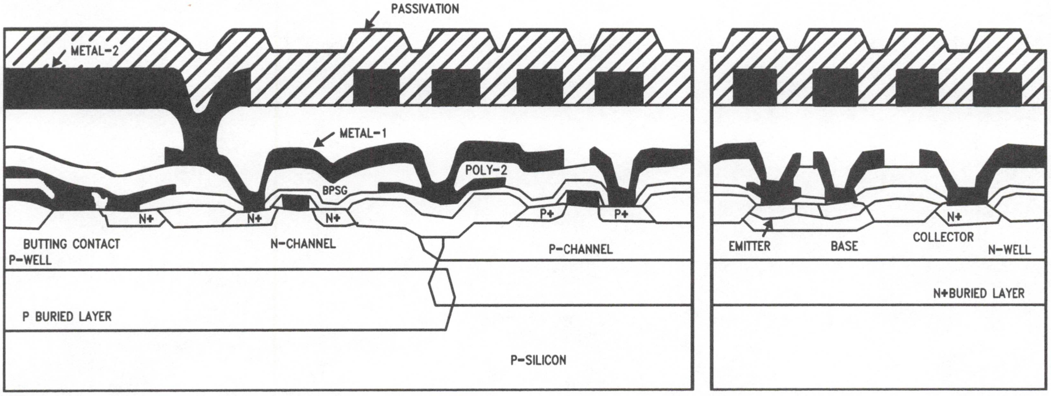
FIGURE 2. Parasitic Bipolar Schematic

In order for latch-up to occur, three conditions must be met.[1] First, there must be high enough lateral substrate current to forward bias both emitter/base junctions. Second, the current gain product of the parasitic pnp and npn must be > 1. And third, the power supply must be capable of supplying the "holding current" required to sustain latch-up. In order to minimize the effects of latch-up, these conditions must be controlled through intelligent process and design.

LATCH-UP AND BiCMOS

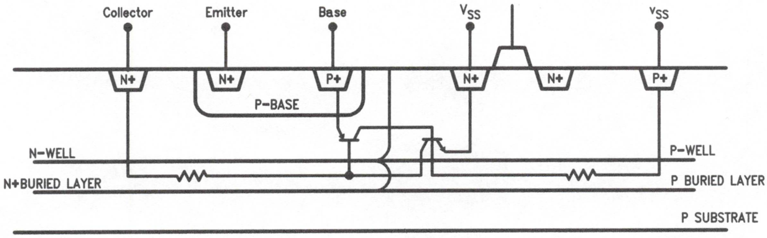
National's BiCMOS III process has inherent advantages over standard CMOS processes. These advantages eliminate latch-up problems and design/layout dependence. As part of BiCMOS III, N+ and P buried layers are present under all n-well and p-well areas respectively. A representative cross section is shown in *Figure 3*. As a result, the lateral n-well and p-well resistance are reduced to ohms from k-ohms. Hence, higher lateral currents can be tolerated without forward biasing the parasitic npn and pnp transistors. Additionally, inclusion of a buried layer results in a significantly lower current gain for the parasitic devices. The use of buried layers for latch-up control has previously been described by Estreich et al.[2]

Unique to BiCMOS processes is a latch-up condition created by the standard npn transistors in combination with the parasitic npn and parasitic pnp as shown in *Figure 4*. If the standard npn is allowed to saturate, forward biasing the base-collector junction, majority carrier holes are injected into the substrate. These carriers then form the base current for the parasitic npn transistors, and potentially, could trip the pnpn latch from its blocking state, to its on state.[3] Again, the N+ and P+ buried layers used in the BiCMOS III process reduce the lateral resistances to the point where this will not forward bias the parasitic transistors and latch-up is avoided.


PASSIVATION
METAL-2
METAL-1
POLY-2
BPSG
N+
N+
N+
P+
P+
BUTTING CONTACT
P-WELL
N-CHANNEL
P-CHANNEL
P BURIED LAYER
P-SILICON
EMITTER
BASE
COLLECTOR
N+
N-WELL
N+BURIED LAYER

TL/D/10091-3

FIGURE 3. BiCMOS III Process Cross Section


Collector
Emitter
Base
V_{SS}
V_{SS}
N+
N+
P+
P-BASE
N+
N+
P+
N-WELL
N+BURIED LAYER
P-WELL
P BURIED LAYER
P SUBSTRATE

TL/D/10091-4

FIGURE 4. BiCMOS Latch-Up Circuit

TEST RESULTS

Latch-up testing has been performed at temperature extremes for National's 256k x 1 ECL BiCMOS SRAM (NM5100) and no latch-up was observed. In all cases, latch-up could not be induced. Testing was performed under the following conditions:

Temp. = −60°C and 130°C

$V_{EE} = -5.0V$; $V_{CC} = 0V$

Each device pin ramped from 0 mA to 500 mA.
(Only one pin tested at a time.)

The following cases were tested:

1. Float all pins except supply pins and pin under test.
2. Pins adjacent to pin under test = V_{CC}, all other pins floating except supply and pin under test.
3. Same as #2 except adjacent pins = $-1.9V$ (V_{IL}).

CONCLUSION

National's BiCMOS III process has proven to be immune to latch-up in extensive characterization and testing. It has inherent process advantages over standard CMOS processes with respect to latch-up. Today, these advantages insure latch-up immunity in the NM5100. In the future, they will also insure latch-up immunity in all of National's BiCMOS static RAMs.

REFERENCES

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2. D.B. Estreich, "An Analysis of Latch-Up Prevention in CMOS IC's Using an Epitaxial-Buried Layer Process" *IEDM Digest,* pp. 230–234, 1978.
3. A.R. Alvarez, "BiCMOS Technology," *IEDM Short Course,* Dec. 1987.

Hot Carrier and Gate Oxide Reliability Characterization of National Semiconductor's BiCMOS III Technology

National Semiconductor
Application Note 567
Eric Hall
Marshall Davis

INTRODUCTION

Gate oxide quality and the susceptibility of MOSFETs to hot carrier degradation are two concerns which are of prime importance in the reliability of a MOS process. Detection of weak devices that can lead to field reliability failures is critical. Thus, major emphasis has been placed on end of line monitors and identifying processing steps which have improved the reliability of the BiCMOS III process.

HOT CARRIER DEGRADATION

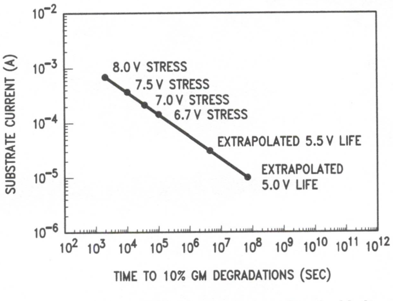
With decreasing MOSFET channel lengths, such as with National's BiCMOS III one micron technology and 256k SRAM, localized fields at the drain region continue to increase. This results in highly accelerated electrons which may collide with the silicon lattice and create electron hole pairs (impact ionization). Some of the "hot" carriers may be trapped in the gate oxide or at the oxide interface. Trapped carriers, or charge generation as a result of carrier injection, result in parametric shifts, which can lead to decreased performance and system non-functionality.

Device degradation is often measured in terms of percent shift in transconductance, Gm, which is the change in drain current with respect to the change in gate voltage at a constant drain voltage. In the BiCMOS III technology, Gm degradation has been characterized by accelerated DC and AC testing of N-channel MOSFETs. In DC stressing, the drain is held above 5.5V with the gate voltage set to achieve maximum impact ionization current, which is measured using substrate hole current. The time for 10% Gm degradation is used as a standard benchmark to show process stability and to study process effects on degradation. For AC stressing, several test modes are used to simulate different circuit conditions. Inverter and SRAM pass gate circuits are the two most used stress conditions. AC frequencies have been used up to 10 MHz, with rise and fall times from 100 ns down to 4.5 ns. AC testing shows degradation mechanisms not seen in DC stressing, and is, therefore, a better indicator of circuit lifetime(1). For both AC and DC stressing, the lifetime data is extrapolated back to a drain voltage of 5.0V and 5.5V to give the life under normal operating conditions as seen in *Figure 1* below.

From CMOS ring oscillator simulations on BiCMOS III, the time required for the gate to pass through the region which creates the highest impact ionization current was found to be about 1% of the total switching period. Taking into account that the CMOS circuitry constitutes approximately 50% of the total access time for the 256k SRAM, a 4E+6 second time to 10% Gm degradation, obtained from *Figure 1*, would equate to 8E+8 seconds [4E+6/(0.01 × 0.5)], or about 25 years at worst case operating conditions. AC stress data for inverter operation also shows much longer lifetimes than DC stress data. For pass gate circuits, Gm degradation is not important, but rather the drain current in the saturation region. This has been studied using AC stressing and has also shown very satisfactory lifetimes. Actual circuit degradation will be additionally determined by the switching frequency in the application of the MOSFET. System level failure will be determined by the application of the SRAM in terms of timing tolerances or power levels.

An additional processing concern is that the introduction of hydrogen during the Silicon Nitride plasma deposition for the second passivation, plasma bond pad etching, and the final forming gas anneal, also contribute to hot carrier injection. Introduced hydrogen ions form weak Si-H bonds at the oxide interface, and can be easily broken by hot carrier injection. Plasma radiation may enhance this process. Research is ongoing to optimize a final passivation process with minimal degradation effect. A final phosphorous doped silicon glass (PSG) passivation for devices in hermetic packages is also being considered.

To better understand total circuit effects, access time degradation is being characterized on 256k devices through both static and dynamic burn-in at −55°C and $V_{EE} = -6V$. In a static burn-in, no parametric shifts were seen through 1000 hours. Dynamic burn-in is currently underway. To date, the DC stressing results and the static burn-in results show that BiCMOS III has good tolerance against hot carrier degradation.



TL/D/10092-1

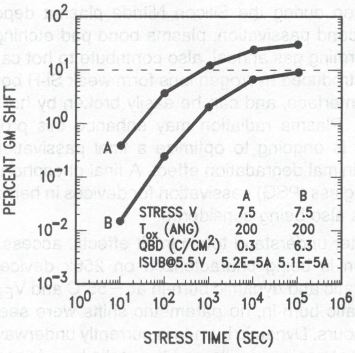
FIGURE 1. Accelerated AC and DC Stressing of Drain Voltage to Determine 10% GM Degradation under Normal Operating Conditions

GATE OXIDE INTEGRITY

Wafer Level Reliability (WLR) monitors in the BiCMOS III process are used to identify possibly unreliable lots. Two such measurements that are used for monitoring gate oxide integrity and possible hot carrier degradation are the Charge-to-Breakdown (Q_{bd}) and Fowler-Nordheim tunneling calculations to determine minimum oxide thickness. These measurements are taken on test structures that lie in the scribe line in between the 256k die. The test structures used are poly edge intensive capacitors, with N+ junction regions, which best simulate actual transistor gates. The WLR gate oxide monitors have been very successful in detecting processing problems which result in both yield failures and decreased reliability.

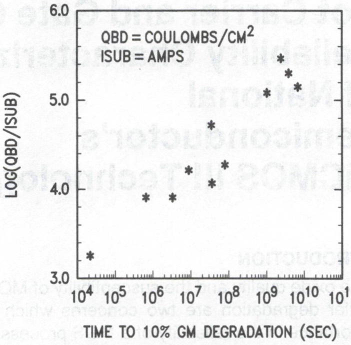
The Fowler-Nordheim minimum oxide thickness is determined from current measurements taken during V-ramp testing. This test shows the oxide thickness at the thinnest, or weakest, point in the structure, unlike capacitance measurements which give an average thickness of the gate oxide. This measurement is particularly useful in detecting point defects or oxide thinning at the field edges, which create localized high field regions.

In the Charge-to-Breakdown measurement, a constant current density is forced ($J = 0.1\ A/cm^2$) while the gate voltage is monitored. This is done until avalanche breakdown occurs, which is defined as a 50% reduction in the gate voltage in a one second interval. Q_{bd} is calculated as being J × time to fail, in units of Coulombs/cm^2. Q_{bd}, and not just substrate current alone, has also been found to correlate well with hot electron degradation in the BiCMOS III process *(Figures 2* and *3)* (2).



TL/D/10092–2

FIGURE 2. G_m Degradation over Time for Devices with the Same Substate Current and Stress Voltage, but Different Q_{bd}



TL/D/10092–3

FIGURE 3. Relationship between Q_{bd}/I_{sub} and the Time to 10-Percent G_m Degradation during Hot-Electron Stressing

SUMMARY

With reliability monitors and continued development, the effects of hot carrier and gate oxide degradation can be minimized and controlled. BiCMOS III also has incorporated in-line and end-of-line WLR monitors to ensure high reliability. Fowler-Nordheim thickness and Q_{bd} measurements are good indicators of weak or thin gate oxides with susceptibility to hot carrier degradation. All of these enhancements and WLR monitors help to provide for excellent process stability.

REFERENCES

1. H. Wang, M. Davis, R. Lahri, *"Transient Substate Current on N-Channel MOSFET Device Lifetime"*, (to be presented at IEDM 1988).
2. M. Davis and R. Lahri, *"Gate Oxide Charge-to-Breakdown Correlation to MOSFET Hot-Electron Degradation"*, *IEEE Elect. Dev. Let.*, vol. EDL-9, No. 4, pp. 183–185, April 1988.

The Reliability of National Semiconductor's 256k x 1 BiCMOS SRAM (NM5100/NM100500)

National Semiconductor
Application Note 568
Eric Hall

INTRODUCTION

Since the beginning of the development of National Semiconductor's one micron BiCMOS III process one third of the BiCMOS process development team has been dedicated to reliability assurance. Long before first silicon of the 256k SRAM arrived, many test structures which contained devices similar to those on the 256k were available for characterization and enhancement of the reliability of the process. Once 256k die were available, extensive dynamic high temperature operational life (HTOL) testing began in a real-time monitored burn-in system.

PROCESS RELIABILITY TESTING AND RESULTS

Before the 256k die arrived in silicon, test vehicles allowed BiCMOS process engineers to characterize the process for such reliability concerns as gate oxide quality, electromigration in metals and the integrity of passivation layers.

With the thin gate oxide (200Å) in the BiCMOS III process, the high quality of the oxide is critical. Such tests as breakdown voltage measurements, thickness measurements and current stressing were performed. Normal breakdown voltages of the dielectric in excess of 24V were measured, where target values are 20V–22V for this thickness. Thickness measurements were developed to give a thickness at the thinnest point in the oxide and not just an overall average. Constant current stressing allowed for a method of monitoring hot carrier degradation. These three tests allowed for detecting weak points in the oxide and correcting them with process enhancements.

As well, electromigration was tested in the BiCMOS TiW/Al-CuSi/Ti metal sandwich, contacts and vias. From the results, all structures have expected lifetimes in excess of 100 years with small variance. This is independent of whether the failure mode was an open circuit, intralayer short or interlayer short.

Another reliability monitor which was performed on unlidded, packaged test structures was a high temperature (85°C) and high humidity (85% RH) stress test. Two groups of units were tested; one group having just a single layer of phosphorous doped silicon glass (PSG) passivation and the other with an additional layer of silicon nitride passivation (normal BiCMOS process). After 2000 hours, only two parts from sixteen with PSG alone showed any signs of corrosion. Later BiCMOS SRAMs were subjected to HAST (highly accelerated stress testing; 145°C, 85% RH). Through 48 hours, equivalent to over 2500 hours of 85°C/85% RH, five of 26 parts had corroded bond wires. However, no sign of metal corrosion of the die was observed, even under SEM analysis. Again these parts were tested in unlidded packages with full passivation.

These monitors and testing of the BiCMOS III process are just a sample of the total number that have been performed. Furthermore, the areas of reliability concern, such as breakdown energy of metal and gate oxide quality are continually monitored on each 256k fab lot with wafer level end of line testing.

NM5100 DIE RELIABILITY TESTING AND RESULTS

HTOL testing is used to accelerate failure mechanisms that may occur during the lifetime of the device. This is achieved by stressing the devices at elevated temperatures and voltage. Some of the typical failure modes stressed by HTOL are ionic contamination, electromigration and oxide time dependent dielectric breakdown (TDDB). The first two failure modes are accelerated by temperature when a bias voltage is applied. The temperature increase will allow contaminating ions enough energy to become mobile and getter at the device surface causing threshold shifts. Electromigration occurs in high current density areas of metal. Aluminum atoms are transported along the grain boundaries of the metal in the direction of the electron flow. This creates voids in the metal at one end and a build up of aluminum atoms (hillocks) at the other. Often the failure mode results in an open circuit.

TDDB is also accelerated by voltage stressing. Over time when a constant voltage is applied across the gate of a MOS transistor, trapped charge will accumulate in the gate oxide. This will continue until the effective potential across the gate oxide equals the breakdown voltage of the dielectric (hence the name TDDB), at which time failure occurs.

The activation energies for these three failure mechanisms are given in Table I below where a higher energy corresponds to a larger acceleration factor from operating temperature to stress temperature. The temperature acceleration factor is given by equation 1 where Ea is the activation energy.

$$\mathrm{AF\ (Temp)} = \exp[\mathrm{Ea}/k(1/\mathrm{Tst} - 1/\mathrm{Top})] \qquad \text{Eq. 1}$$

The voltage acceleration factor for TDDB is

$$\mathrm{AF\ (Vtg)} = \exp[\mathrm{B}(1/\mathrm{Eop} - 1/\mathrm{Est})] \qquad \text{Eq. 2}$$

where Eop is the operating voltage divided by the gate oxide thickness (200Å), Est is the stress energy and B is an empirical constant of the process. B has been measured to be 112 MV/cm for BiCMOS III.

BiCMOS 256k and 16k SRAMs (the 16k is identical in its periphery circuitry to the 256k but has a smaller memory) have been stressed in a monitored dynamic burn-in system at a voltage supply of −6.25V and a temperature of 150°C. The acceleration factors and stressed hour to operational year equivalents for the 256k are summarized in Table I. The monitored burn-in system allows for functionally exercising each part to test patterns such as march and checkerboard. The burn-in tester will log the time and board location of any failure. In addition all devices were individually serialized and tested for parametric shifts at 0, 24, 48, 72, 144, 288, 576, and 1152 hour readpoints. In all, 24 parameters were monitored across the commercial temperature range of 0°C to 85°C. Excellent results were attained; none of the parameters shifted significantly from 0 to 1152 hours. A sample of these parameters is summarized in Table II below.

4

TABLE I
NM5100 BiCMOS 256k x 1 SRAM Acceleration Factors

Fail Mechanism	Ea	Temp AF	VTG AF	TOT AF	10 YR	1152 HR
Electromigration	0.7 eV	160	N/A	160	547 HR	21 YR
Oxide TDDB	0.3 eV	8.8	133	1174	74 HR	156 YR
Ionic Contamination	1.0 eV	1412	N/A	1412	62 HR	186 YR

$V_{OP} = -5.5V$, $V_{ST} = -6.25V$, $T_{OP} = 75°C$, $T_{ST} = 172°C$

TABLE II
NM5100 BiCMOS 256k x 1 SRAM HTOL Parametric Data

Parameter	0°C 0 HR	0°C 1152 HR	85°C 0 HR	85°C 1152 HR	Units
I_{EE}	−143.58	−144.36	−137.31	−138.49	mA
V_{OH}	−0.97	−0.97	−0.98	−0.98	V
V_{OL}	−1.70	−1.71	−1.72	−1.73	V
T_{AA} (TAVQV)	11.50	11.36	13.24	13.10	ns
T_{W} (TWLWH)	8.22	7.99	10.01	10.01	ns
T_{WSA} (TAVWL)	−5.96	−5.96	−6.64	−6.87	ns
T_{WHA} (TWHAX)	−4.51	−4.41	−5.62	−5.82	ns

Parametric Shifts in AC values < 200 ps are not significant due to tester resolution.

TABLE III
BiCMOS SRAM Burn-in Results

Lot #	Device	Test	# IN	# HRS	# Fails	Shift	Comment
1	16k	Static HTOL	30	3456	0	No	
2	16k	Static HTOL	28	1728	0	No	
3	16k	Dynamic HTOL	33	1152	0	No	
4	16k	Dynamic HTOL	58	1152	0	No	
5	256k	Dynamic HTOL	40	1728	1 @ 96 Hrs	No	Single Bit
6	256k	Dynamic HTOL	114	1152	0	No	
7	256k	Dynamic HTOL	125	1152	0	No	
8	256k	Dynamic HTOL	75	1152	1 @ 24 Hrs	No	Minirow
9	256k	Dynamic HTOL	12	1152	0	No	PtSi/As+ EVAL
10	16k	Static LTOL	29	1000	0	No	HOT e− EVAL

Oven Temp = 150°C for HTOL, −55°C for LTOL.
Supply V_{EE} = −6.25V for dynamic, −6.0V for static burn-in.

Out of all the 16k and 256k devices, only two units failed functionally during the burn-in stress testing (Table III). One unit failed at the 96 hour readpoint with a "stuck" single bit. The second failed at the 24 hour readpoint with a minirow fail. These failures are currently being analyzed. For 256k devices alone, this would equate to 32 FIT (1 Failure In Time equals 1E+9 device hours). Since a production burn-in equal to 48 hours is performed on all devices, this implies that the 24 hour failure would have been screened out as a failing unit. This brings the FIT rate down to 16 FIT. For example, with 1000 units, it would be over 7 years of operation at constant worst case operating conditions before 1 device fails. One other remarkable point to note is that all of the 16k SRAMs used for HTOL and also Lot 5 of the 256k devices were from only the second BiCMOS SRAM lot ever produced in the fab.

As part of the functional testing that each device receives, a gate oxide stress is applied with a −6.5V supply. This stress will screen devices with very weak oxides for TDDB failures.

Further evaluations include a low temperature op life study for hot carrier degradation and a HTOL look ahead for possible process enchancements. At low temperatures the silicon lattice is more stable and an electron has a greater probability of colliding with it and creating an electron hole pair (impact ionization). The "hot" carriers may then become trapped in the gate oxide causing threshold shifts. A static burn-in at a supply of −6.0V and stress temperature of −55°C was performed on 29 units for 1000 hours. In this study no fails or parametric shifts were observed. A dynamic test under the same conditions is under way.

Upcoming process changes involve conversion from phosphorus to arsenic doped emitters for speed enhancement and adding a platinum silicide layer under first metal to reduce P+ contact resistance. Twelve units have been burned in to 1152 hours, once again with no fails or parametric shifts.

SUMMARY

As indicated by the "upfront" commitment from the BiCMOS process development group to their wafer level testing and end of line monitors, followed by the burn-in studies with actual 256k SRAMs, the reliability of the BiCMOS III process has been fully characterized and enhanced. To further insure the reliability, each fab wafer lot will continue to be monitored and samples will be periodically placed on HTOL. Additionally, each device receives, and will continue to receive, a 48 hour burn-in and gate oxide stress test in order to eliminate infant mortality failures before they are shipped to the customer. Reliability was designed into the process and will continue to be a major factor in manufacturing of BiCMOS III products.

REFERENCES

1. D.L. Crook, *"Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown," ibid.,* 17,1, 1979.

2. Technology Associates, *Accelerated Testing Handbook,* 1987.

256k x 1 BiCMOS ECL SRAM Memory Cell Characterization and Alpha Sensitivity Testing

National Semiconductor
Application Note 569
Paul Berndt
Dave DiMarco

INTRODUCTION

National Semiconductor's 256k x 1 BiCMOS ECL SRAM (NM5100) has undergone extensive characterization to ensure its reliable performance in a system. Part of the characterization entailed an extensive analysis of the stability and alpha sensitivity of the memory cell. The stability and alpha sensitivity are major attributes of the memory cell. These attributes will affect the reliability and performance of the memory in a system environment from a "soft error" stand point. A "soft error" is a fail which occurs when the memory cell looses data and flips state but can then successfully be rewritten with data.

CELL STABILITY

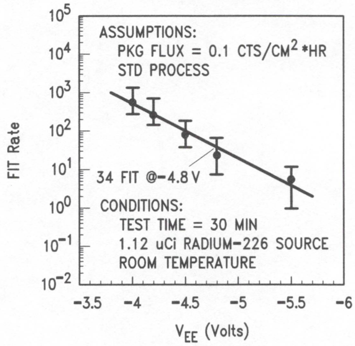
The stability of the memory cell will determine the memory's immunity to system level disturbances. One such disturbance of special interest is address skew. Address skew is a common phenomena in systems which can cause "soft error" problems. An unstable memory cell will be highly sensitive to this condition. When addresses are skewed on a static RAM, memory cells can be partially selected. This can degrade the internal voltage margin in the memory cell to the point where it may flip states, resulting in a "soft error". The NM5100 has been extensively characterized from both a DC and an AC point of view to verify immunity to this phenomena. Additionally, all die are tested to a simulated address skew condition at wafer level to insure device integrity.

ALPHA SENSITIVITY

The alpha sensitivity of the memory cell is a major factor in determining a memory's Soft Error Rate (SER). Alpha particle hits are a well documented cause of "soft errors" in semiconductor memories.(1) The package material used in semiconductor devices emits alpha particles due to contaminates which are present in the package material. These contaminates are present in plastic and ceramic packages. When an alpha particle strikes the internal node of a memory cell, it can cause the cell to change states. This results in a soft error. Even though low alpha flux package material is used, alpha induced soft errors can still cause system problems if proper memory design techniques are not followed.

In order to determine what the alpha SER of a memory will be, accelerated alpha testing must be conducted. Accelerated alpha testing is done with sources which have alpha fluxes that are orders of magnitude higher than that of packages. These high flux alpha sources make it possible to assess the alpha sensitivity of the device in a short period of time. Alpha performance is measured in FITs. One FIT equals one fail in 10E^9 device hours. The FIT Rate is calculated by taking the flux of the alpha source and the flux of the device package and calculating an acceleration factor.

For the NM5100, alpha sensitivity testing was done with Radium-226 sources. These sources match the energy distribution found in packaging materials. A Takeda 3331 Memory Tester was used to test devices and log errors. A checkerboard pattern was written into the memory and read in 5 minute intervals to check for errors for a total of 30 minutes. Alpha testing was conducted over the following supply voltages: −4.00V, −4.20V, −4.50V, −4.80V and −5.50V. *Figure 1* shows the NM5100's FIT rate vs supply voltage. FIT rates below 100 have been achieved for V_{EE} less than −4.50V!



Alpha

TL/D/10094-1

FIGURE 1

CONCLUSION

Cell stability and alpha immunity are two major components required for system reliability. These components have been thoroughly characterized to insure the NM5100's reliable performance in a system. Cell stability is tested on all devices and alpha induced soft error rates of less than 100 FIT have been demonstrated (without die coat)!

REFERENCES

1. Tim May, Murry Woods, "*A New Failure Mechanism for Soft Errors in Dynamic Memories*", Proceedings 1978, Reliability Physics Symposium, April 1978, pp. 33–40.

Understanding Advanced Self-Timed SRAMs

National Semiconductor
Application Note 572
Charlie Hochstedler

INTRODUCTION

The Advanced Self-Timed SRAM devices are designed to relieve several system design difficulties usually encountered when designing memory arrays associated with high speed ECL data processors. These unique and innovative devices are intended for applications demanding high memory bandwidth. The design of arrays for cycle times of 5 ns to 10 ns is much easier with these AST SRAMs than with generic ECL SRAMs. Speed critical applications such as caches, address translation buffers, writable control stores, and large register files all may greatly benefit from the use of these new memory devices.

This brief explains the differences between conventional SRAMs, self-timed SRAMs, and these new Advanced Self-Timed SRAMs. Particular emphasis is given to the timing differences, which profoundly influence the system design. This brief does not include a complete discussion of all the features and functions of an AST SRAM. Device data sheets contain additional and very important information, and should be reviewed along with this brief.

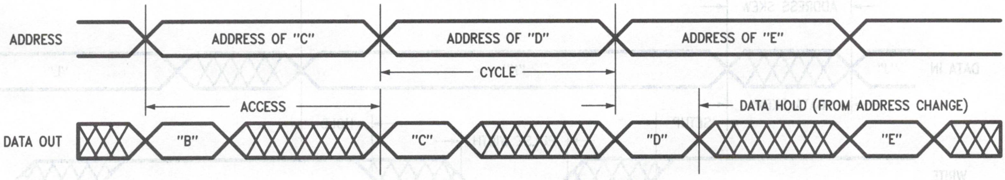
LIMITATIONS OF GENERIC SRAMs

High speed ECL SRAMs are certainly available. They offer fast read access. Careful system design can result in good access performance, but high bandwidth is very often a significant challenge or even an elusive goal. Memory bandwidth is commonly defined as the reciprocal of the cycle time. Access time is the delay you encounter while waiting for a memory response, and cycle time is the rate at which you can repetitively access memory. Generic SRAM data sheets would lead you to believe that cycle time is equal to access time. A more realistic view might be to consider access time the lower limit of cycle time; seldom achieved in practice. The reason for this difference between access time and cycle time will become clear through a quick review of the timing of a generic ECL high speed SRAM.

Read cycle timing is shown in *Figure 1,* first as it is found in the typical data sheet, and then again with a few practical system level constraints included. Notice that there is only a very short window of time where data outputs are valid if the cycle time is set equal to the access time. This time is usually specified as output hold or data hold from address change; and is often only a few nanoseconds for fast ECL SRAMs. One system design problem is how to use a very brief data output valid interval. The normal solution is to latch or register the data into the next logic element. The design must allow enough time for the data register or latch setup and hold time. Also added to the setup and hold times is some allowance for the variations expected in the signal which clocks the data register or latch. These factors will invariably sum to a value greater than the SRAM specification for output hold from address change; resulting in the necessity of increasing the cycle time beyond the data sheet minimum.

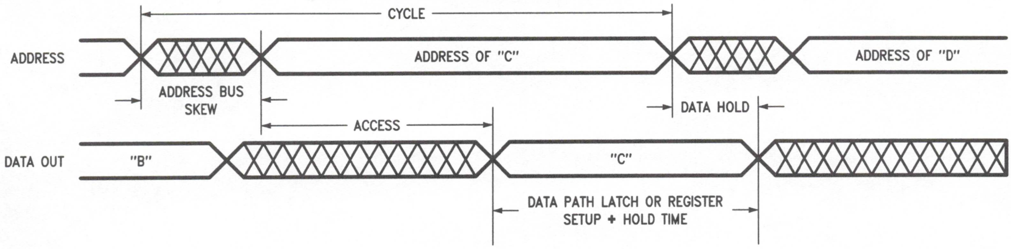
Address bus skew is another speed robbing effect which must be accounted for. In a practical system, addresses can not be guaranteed to change from the previous state to the

Data Sheet Read Cycle



TL/D/10097-1

System Read Cycle



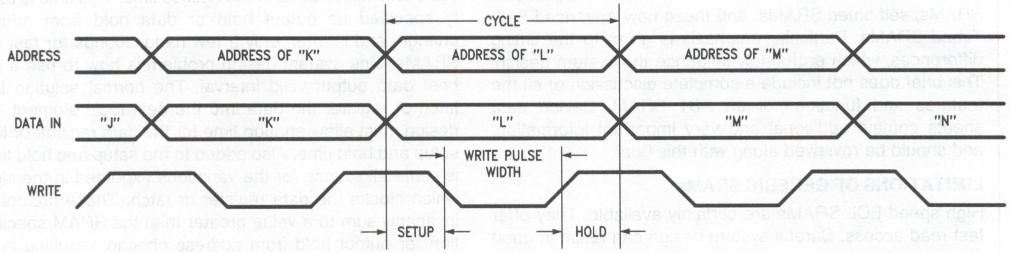
TL/D/10097-2

FIGURE 1. Generic SRAM Read Timing

new state all at exactly the same time. There is, in reality, a window of time during which the addresses may be changing. Address bus skew, defined for the purposes of this brief, is from the instant that the quickest address may begin its transition until the slowest address can be guaranteed to have completed its transition. Address bus skew and data path setup and hold times are normally the most significant factors which cause read cycle time to be slower than read access time.

The write cycle is almost always the bandwidth limiting factor in systems designed with generic ECL SRAMs. It is uncommon for a designer to design for different read and write cycle times because most systems must accommodate reads and writes at random. Writable control stores are a notable exception; caches are a good example of memories usually requiring random reads and writes. *Figure 2* illustrates the differences between a data sheet write cycle and the timing a system designer contends with. For most ECL high speed SRAMs the sum of write pulse width, data setup, and data hold times equals the data sheet write cycle time specification. The write pulse skew (the soonest it may fall, until the time is guaranteed to have risen) adds directly to the write cycle time. Also the effects of address and data bus skew need to be considered to determine which is actually the design limitation. These skews often sum to large values relative to the data sheet speed. It is common for system design constraints to result in practical cycle times of 15 ns to 20 ns for 7 ns SRAMs. If fast access is all that is required, then these effects are not deleterious. In many applications cycle time is as critical as access time, creating a strong desire for relief from these speed degrading effects.

Data Sheet Write Cycle


CYCLE
ADDRESS
ADDRESS OF "K"
ADDRESS OF "L"
ADDRESS OF "M"
DATA IN
"J"
"K"
"L"
"M"
"N"
WRITE PULSE WIDTH
WRITE
SETUP
HOLD

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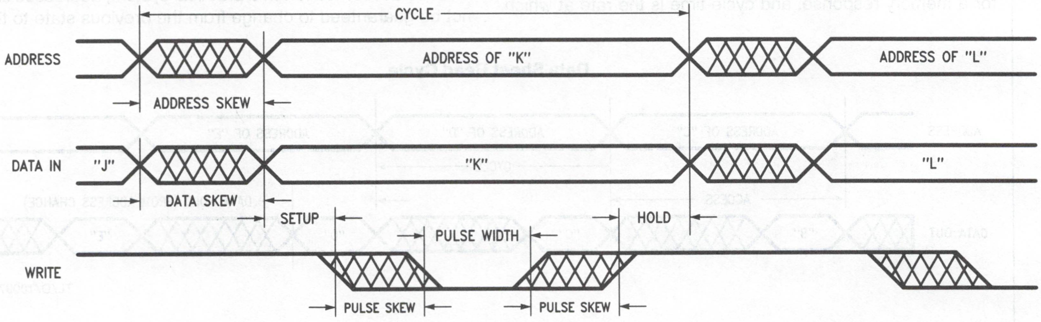
System Write Cycle


CYCLE
ADDRESS
ADDRESS OF "K"
ADDRESS OF "L"
ADDRESS SKEW
DATA IN
"J"
"K"
"L"
DATA SKEW
SETUP
HOLD
PULSE WIDTH
WRITE
PULSE SKEW
PULSE SKEW

TL/D/10097-4

FIGURE 2. Generic SRAM Write Timing

To maximize throughput system designers have often used latches or registers to hold all the inputs going into, and the outputs coming from the memory array. Most ECL processors designed today utilize ECL gate array or standard cell ASICs for the logic elements in the design. This approach makes the inclusion of memory support registers or latches relatively easy and practical. A write pulse generator is generally implemented locally, very near the SRAMs to minimize the write pulse skews. The write pulse generator can be a straightforward monostable utilizing gate delays to set the pulse width; triggered by a write command generated elsewhere in the system logic. As timing demands tighten, the need to time the write pulse from a system clock increases, so more exacting design alternatives are used. *Figure 3* illustrates these functions usually found supporting common ECL fast SRAMs.

Self-Timed SRAMs include on chip registers and/or latches for inputs and outputs, and also include an on chip write pulse timing generator. A basic self-timed SRAM block diagram is given in *Figure 4.* Several variations are appearing today, offering a choice of latches or registers, and a few different types of clock and control functions. These differences are relatively minor and not significant in the understanding of the operation of this new class of memory.

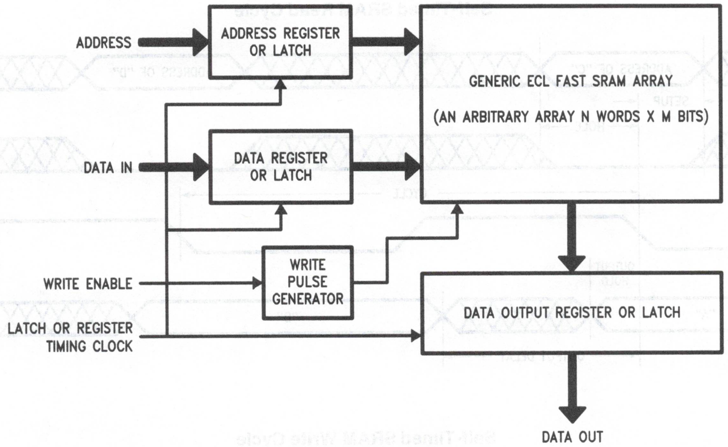

ADDRESS
ADDRESS REGISTER OR LATCH
GENERIC ECL FAST SRAM ARRAY
(AN ARBITRARY ARRAY N WORDS X M BITS)
DATA IN
DATA REGISTER OR LATCH
WRITE ENABLE
WRITE PULSE GENERATOR
DATA OUTPUT REGISTER OR LATCH
LATCH OR REGISTER TIMING CLOCK
DATA OUT
TL/D/10097-5

FIGURE 3. A Typical ECL SRAM Implementation

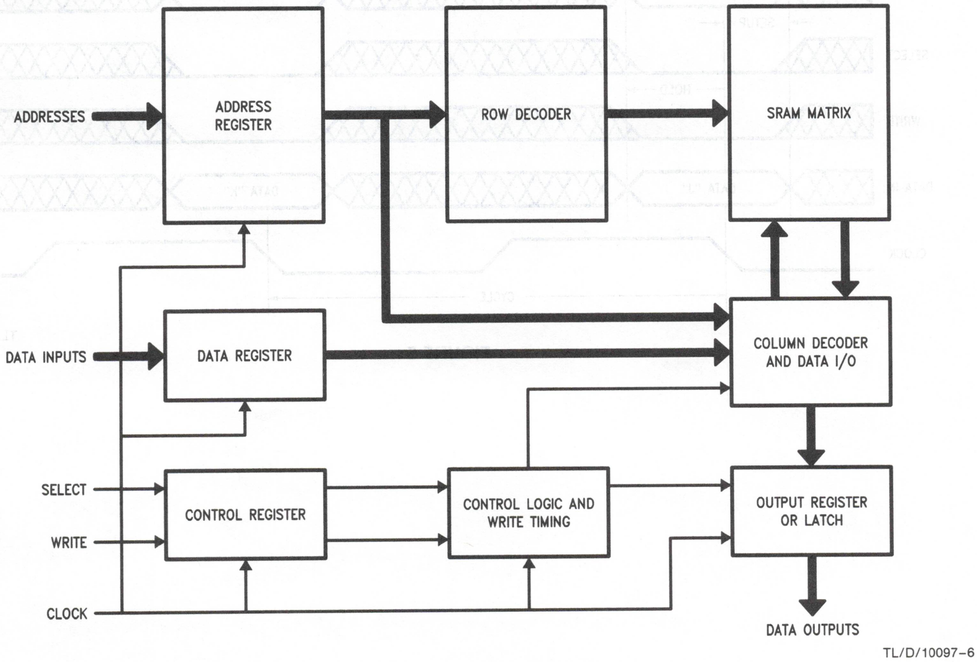
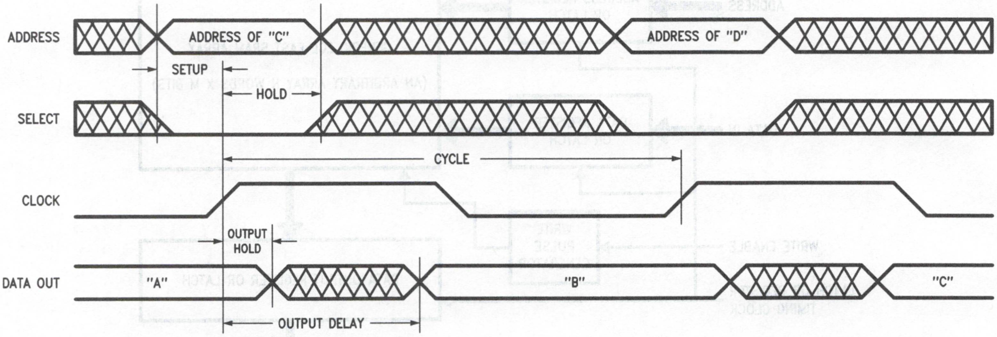

ADDRESSES
ADDRESS REGISTER
ROW DECODER
SRAM MATRIX
DATA INPUTS
DATA REGISTER
COLUMN DECODER AND DATA I/O
SELECT
WRITE
CONTROL REGISTER
CONTROL LOGIC AND WRITE TIMING
OUTPUT REGISTER OR LATCH
CLOCK
DATA OUTPUTS
TL/D/10097-6

FIGURE 4. Basic Self-Timed SRAM Block Diagram

The key to understanding the self-timed SRAM is the timing waveforms of *Figure 5.* Notice that all inputs are registered (or latched in some devices) by the clock edge, in both the read cycle and in the write cycle. Also notice that in a read cycle the data output is registered (or latched in some devices) by the same clock edge. The device now contains the functions which were often included in the memory support logic ASICs. But something more than just different partitioning is happening. Now the registered data output is held for much of a cycle, alleviating the data path setup and hold constraints even with cycle times similar to access time. Also, the data input and address busses are registered, trading off bus skew problems for setup and hold times on the inputs. The control line registers result in the most important difference. With write and select registered, the write timing is all completed internally. This eliminates the need for the system designer to be concerned with the tricky write pulse width, setup and hold time constraints. Control signals are often specified with the same characteristics as the address and data input signals. The ability to easily design for cycle time about the same as access time, especially for write cycles, is the fundamental benefit of self-timed devices.

Self-Timed SRAM Read Cycle


ADDRESS
ADDRESS OF "C"
ADDRESS OF "D"
SETUP
HOLD
SELECT
CYCLE
CLOCK
OUTPUT HOLD
DATA OUT
"A"
"B"
"C"
OUTPUT DELAY

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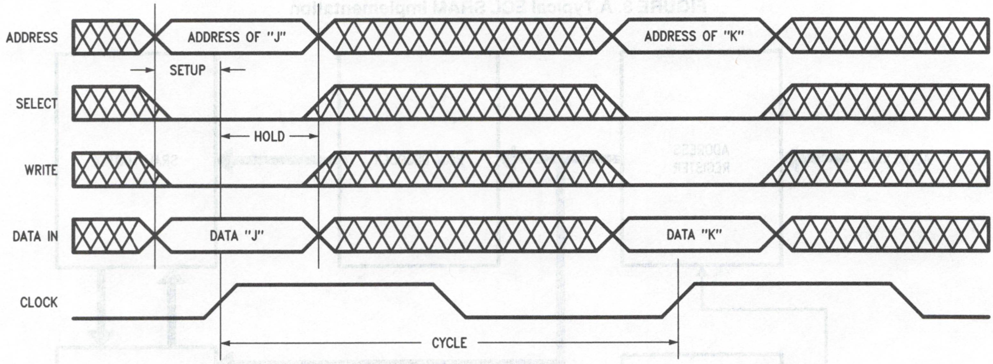
Self-Timed SRAM Write Cycle


ADDRESS
ADDRESS OF "J"
ADDRESS OF "K"
SETUP
SELECT
HOLD
WRITE
DATA IN
DATA "J"
DATA "K"
CLOCK
CYCLE

TL/D/10097-8

FIGURE 5

Different styles of self-timed SRAMs bring slightly different issues to light. The devices with registered inputs and registered outputs are usually defined in such a way as to force the system designer to treat them as a "1 deep" pipeline stage. The data output is always clocked out at the same time as the next set of inputs are clocked in, giving rise to the notion of 1 clock period latency. For many system architectures this may not be a detriment, and the advantages of a shorter cycle time usually outweigh the negatives.

In devices with latched inputs and outputs the data output is available a little sooner (at least theoretically) but the clock usually requires much more critical timing. Now one level of the clock is used to latch the outputs. This places demands on the clock generation and distribution which complicate it more than edge triggered registered style devices.

For complete timing flexibility, separate clocks (i.e., an input clock separate from an output clock) are possible. Generally, the flexibility and performance advantages this can provide are overshadowed by the additional complexity of generating and distributing two carefully controlled clocks instead of one.

ADVANCED SELF-TIMED SRAMs

Advanced Self-Timed SRAMs (AST SRAMs) expand on the concepts of the basic self-timed devices (ST SRAMs) already reviewed. The most important difference is that the AST devices are register based and include an on chip timing generator for the output register. A simplified block diagram for the AST SRAM is given in *Figure 6*.

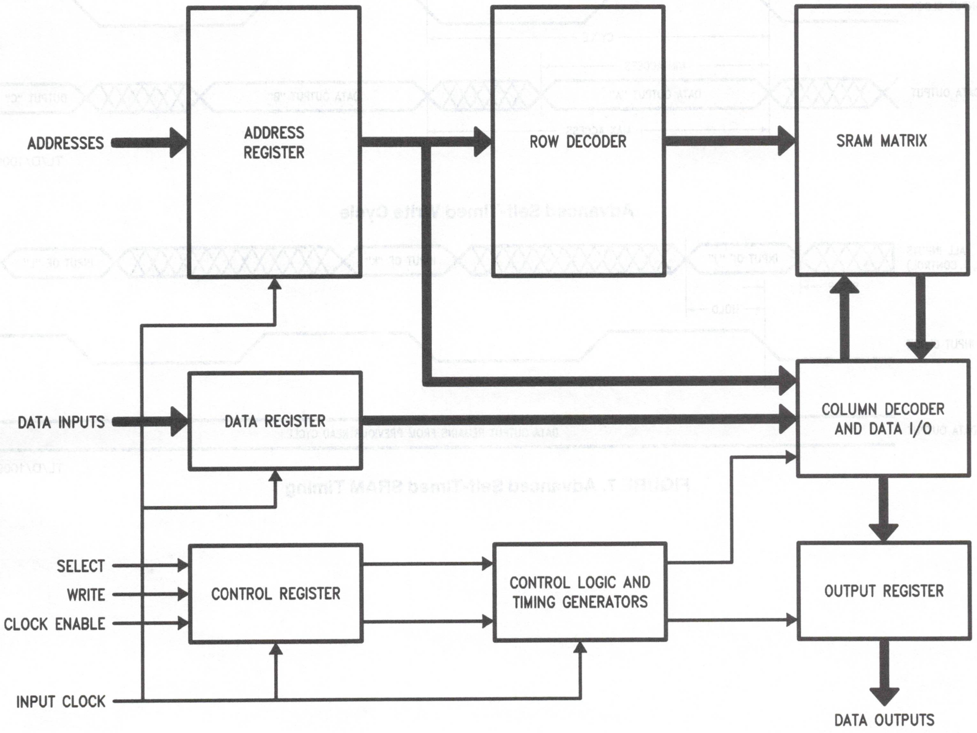

ADDRESSES
ADDRESS REGISTER
ROW DECODER
SRAM MATRIX
DATA INPUTS
DATA REGISTER
COLUMN DECODER AND DATA I/O
SELECT
WRITE
CLOCK ENABLE
CONTROL REGISTER
CONTROL LOGIC AND TIMING GENERATORS
OUTPUT REGISTER
INPUT CLOCK
DATA OUTPUTS

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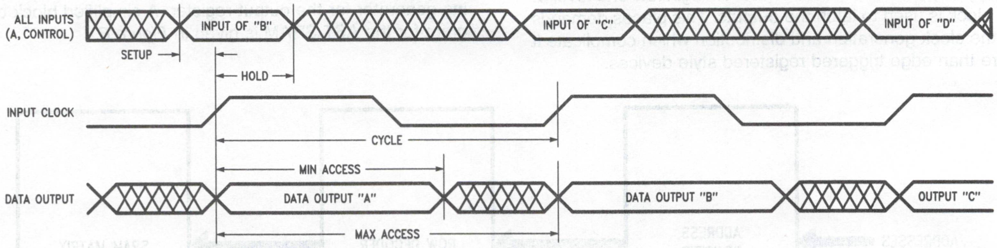
FIGURE 6. Advanced Self-Timed SRAM Simplified Block Diagram

Fundamentally, what is achieved is similar to a registered ST SRAM with separate clocks, with the output clock adjusted for minimum access time. All the other benefits of the basic ST SRAM are retained, but some interesting additional benefits of timing flexibility also are found in the AST SRAM. *Figure 7* illustrates both read and write cycles of the AST SRAM, drawn for the case where the cycle time is set equal to the access time. The key differences to notice are that there is an input clock, and that access occurs a fixed time delay later. Also note that both minimum and maximum access times are given, allowing the designer to properly design to preclude either short path or long path problems. If a system is designed with cycle time longer than access time, the AST SRAM is still quite useful. In this case the device will still internally self-time the read data output register clock (at access time), simply providing earlier access or longer setup for the logic block downstream from the device.

Advanced Self-Timed Read Cycle


ALL INPUTS
(A, CONTROL)
INPUT OF "B"
INPUT OF "C"
INPUT OF "D"
SETUP
HOLD
INPUT CLOCK
CYCLE
MIN ACCESS
DATA OUTPUT
DATA OUTPUT "A"
DATA OUTPUT "B"
OUTPUT "C"
MAX ACCESS

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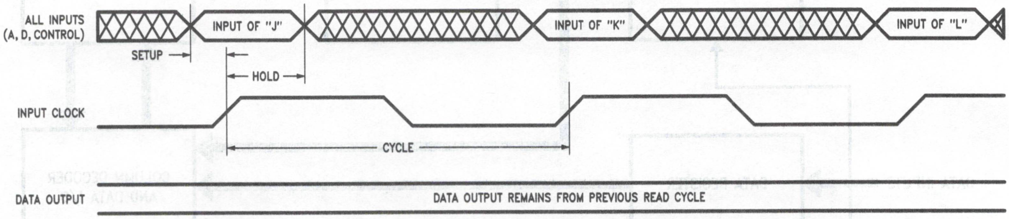
Advanced Self-Timed Write Cycle


ALL INPUTS
(A, D, CONTROL)
INPUT OF "J"
INPUT OF "K"
INPUT OF "L"
SETUP
HOLD
INPUT CLOCK
CYCLE
DATA OUTPUT
DATA OUTPUT REMAINS FROM PREVIOUS READ CYCLE

TL/D/10097-11

FIGURE 7. Advanced Self-Timed SRAM Timing

Another important difference is that the write cycle has no effect on the state of the data outputs. This allows the benefit of a "hidden write cycle" mode which is described in some detail in the device data sheet. The idea behind the hidden write mode is the following: First, since the output register is unaffected by write cycles, and second, since whatever logic needing the read output data will require it for some finite and significant time interval, then it could be an advantage to improve bandwidth by allowing write cycles to occur during the time that the downstream logic needs the read data.

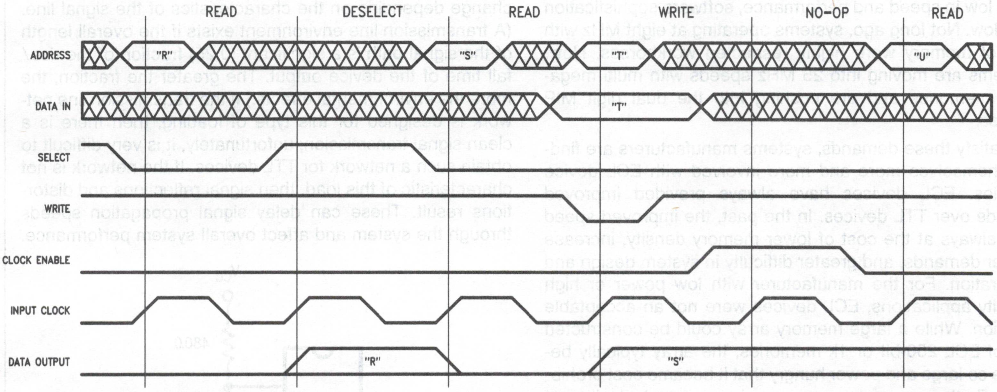
There are several other features and functions provided on the AST SRAM which are not found on ST SRAMs. One particularly worth mention is the benefit of the on chip clock gating control input. Since many of these types of devices are being designed into high speed ECL processors, and since most such systems are pipelined architectures, the designer must contend with the subtle timing nuances which can occur when starting and stopping the pipeline. The on chip clock gating input provides very convenient control without concern over clock "slivers" (i.e., narrow partial clock pulses which can cause unpredictable responses).

To best illustrate the operation of an AST SRAM, *Figure 8* shows an arbitrary sequence of memory cycles. Also shown is the functionality of the clock enable input, which causes the AST device to do nothing for the cycle(s) where it is asserted. Because the device outputs are designed to remain valid with the last read data, there is a deselect cycle which can be executed whenever desired. This does not mean that a wasted dummy cycle is needed to disable the device. In the case where, for example, there are two (or more) AST SRAMs deep in an array with the outputs bussed together, the higher order address decode logic will select the proper device using the select lines; only one of which can be active at the start of each cycle. For the one that is inactive a deselect cycle occurs. For the active one, the result is a read cycle. If, however, the next cycle where a write to any address in the array, the outputs would not disable because that would preclude the benefit of the hidden write mode for arrays more than one device deep. The data sheet provides significant detail on the subtleties of the control functions of an AST device.

Other benefits of the AST SRAM include on chip parity checking, and scan path diagnostics features, all designed in such a way that the designer can ignore them if that particular function is not desired in a given application.

CONCLUSION

Timing skews encountered in practical system designs degrade cycle time significantly from the ideal case for generic ECL high speed SRAMs. Recently a new style of device, the self-timed SRAM, has begun to emerge. These ST SRAMs alleviate several timing constraints and make it easier to design high speed systems, especially when bandwidth is the issue (not just access time). The Advanced Self-Timed SRAM goes a step further in several areas. The AST SRAM offers more flexibility in timing modes, more flexibility in control input functions, and just more speed, too. It makes it rather easy to design for cycle times as short as access time, which is something that no previous SRAM could do nearly as well. For applications in high speed pipelined ECL processors this new style of device is certainly worth serious consideration.



TL/D/10097-12

FIGURE 8. A Sequence of AST SRAM Cycles

Design Considerations for High Speed Architectures

National Semiconductor
Application Note 573
Mike Arden

INTRODUCTION

Users and software developers are placing increasing demands on the systems manufacturer to improve the performance of his products. Quite often, these demands can be reduced to two fundamental characteristics of the system, memory array size and system speed. Larger and larger memory arrays are required to support the memory intensive demands of new software applications. Furthermore, as software complexity increases, the system is burdened with more and more software overhead. Greater operating speeds are demanded out of a system in order to support the enlarged software demands without burdening the user with a less responsive system.

Historically, memory array sizes could be improved with the implementation of larger TTL memory devices. The improved density and availability of semiconductor memory devices over the past twenty years is well known. Memory density has improved at roughly a geometric growth rate. To some extent, the memory device could be treated as an ever increasing, self contained black box. The techniques used to integrate a 256k DRAM are virtually identically to those required of a 1k DRAM. It was up to the semiconductor manufacturer (and in his best interest) to maintain a logical progression from one device generation to the next. During this same period of time, small to mid-level systems (personal computers, workstations, graphic display stations, etc.) were in their infancy. Eventhough, processors were fairly low in speed and performance, software sophistication was low. Not long ago, systems operating at eight MHz with 32k of memory were highly respected workhorses. Now, systems are moving into 25 MHz speeds with multi megabyte memories and are pushing into the dual digit MIP ranges.

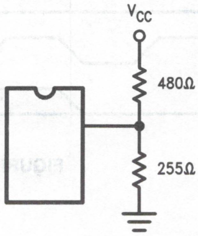
To satisfy these demands, systems manufacturers are finding themselves more and more involved with ECL device families. ECL devices have always provided improved speeds over TTL devices. In the past, the improved speed was always at the cost of lower memory density, increase power demands, and greater difficulty in system design and integration. For the manufacturer with low power or high density applications, ECL devices were not an acceptable solution. While a large memory array could be constructed out of ECL 256-bit or 1k memories, the array typically became so large and power hungry that it became cost prohibitive. Furthermore, processor engines were typically not available to make use of this high speed memory.

With the advent of the National Semiconductor's BiCMOS ECL memory products, the traditional shortcomings related to density and power consumption have been eliminated. ECL memories rival their TTL counterparts in density and power consumption. In addition, these memories retain the traditional ECL speed advantage over their TTL cousins. Furthermore, ECL system environments offer distinct advantages over TTL environments which can enhance system performance.

System Environments (ECL vs TTL)

As mentioned previously, for low speed/performance systems, ECL devices are more difficult to integrate into a system than TTL devices. This is due to the particular electrical requirements for ECL devices. Correctly implementing an ECL device is more than simply connecting an output of one device to an input of another. The system environment that an ECL device is placed in is defined (loading, network terminations, line impedances, etc.) and the device is designed specifically for this environment. A TTL device on the other hand is not designed for any particular system environment. While this aids the TTL device in fitting into general use applications, it is a major stumbling block for high speed applications.

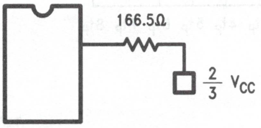
For example, TTL device outputs are designed for load conditions related to TTL input conditions. *Figure 1a* shows a common (databook) TTL test load configuration. This load is an approximation of multiple TTL input loads. When the output is in the HIGH state (≥ 2.4V), the load will sink a minimum of 4.0 mA. Conversely, when the output is in the LOW state (≤ 0.4V), the load will source a minimum of 8.0 mA. These are common V_{OH}/I_{OH} and V_{OL}/I_{OL} DC conditions. The device is designed and tested to this set of conditions. As long as the device is placed in an environment such that signal paths are relatively short, the TTL output will behave as expected. However, if the device is placed into a transmission line environment the output characteristics will change depending on the characteristics of the signal line. (A transmission line environment exists if the overall length of the signal path is a significant (0.25) fraction of the rise/fall time of the device output. The greater the fraction, the more the environmental effects.) If the transmission line network is designed for this type of loading, then there is a clean signal transmission; unfortunately, it is very difficult to obtain such a network for TTL devices. If the network is not characteristic of this load, then signal reflections and distortions result. These can delay signal propagation speeds through the system and affect overall system performance.



TL/D/10098-1

FIGURE 1a. Databook

Theoretically, a transmission line network can be designed for a TTL load. *Figure 1b* shows the Thevenin equivalent of the TTL load. This equivalent load has the same loading properties as the original load. From this Thevenin load, a transmission line matching load can be derived (see *Figure 1c*). The transmission line load is equivalent to the databook load with the exception of the physical propagation delay of the transmission line. A device output will behave exactly the same with this load as it would with the databook load. The signal itself would be delayed by the transmission line, but not distorted. A device input at the other end of the line would see an undistorted TTL output waveform.



TL/D/10098-2

FIGURE 1b. Equivalent Loading

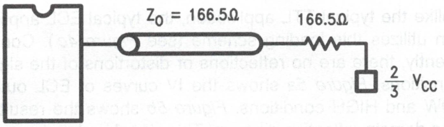


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FIGURE 1c. Transmission Line Match

Unfortunately, TTL systems are not designed with this type of loading scheme. *Figure 2* shows a more commonly found environment. Note that the signal line impedances are lower than the ideal. High impedances in printed circuit boards are difficult to manufacture and are not commonly found. Quite often 75Ω–100Ω is an upper limit. Also, the transmission line is unterminated. The ideal transmission line load used a 166.5Ω resistor terminated to 3.33V. Terminated lines would require an additional power supply and many discrete resistors to implement. These differences equate to reflections on the signal paths. These reflections can result in delays in data transmission.

Figure 3a shows IV curves of TTL inputs and outputs in the HIGH state. These curves can be equated to time domain reflection diagrams illustrating the signal integrity. For the example of a 100Ω environment, *Figure 3b* shows the resulting waveforms. For this example, any input at the far end of the line will receive a relatively clean signal. The signal is above the V_{IH} level at t = T and data can be properly identified. The slight bump at t = 3T only cleans up the signal futher. The problem arises if another input is placed near the device output. Due to the reflection from the far end of the line, the input at A (device 2) has to wait until t = 2T before it receives clear identifiable data! Furthermore, any input placed somewhere between the output and the end of the transmission line will see some distorted signal which may not provide a valid data transition until t = 1.5T. This example is relatively simple; even still, such a reflected delay can amount to a significant percentage of the overall cycle rate and can cause a marked degradation in system speed. Depending on the type of routing scheme used, and the actual impedances of the PCB, even greater delays can occur.

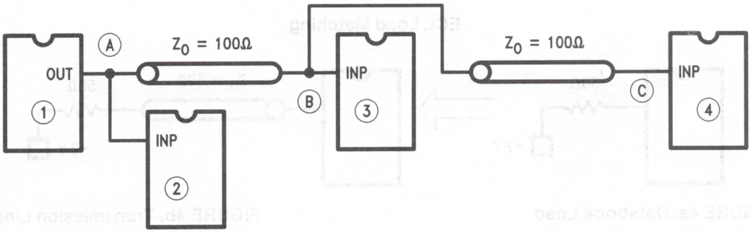

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FIGURE 2. "Typical" Application

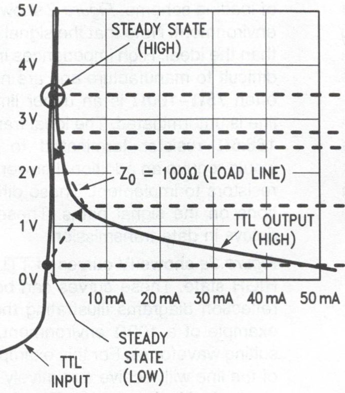

FIGURE 3a. TTL Transition to High State

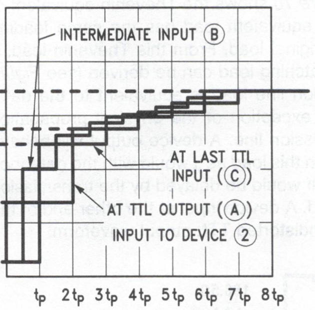

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FIGURE 3b. Reflection Diagram for Transition to High State

For ECL devices placed into their specified environment, reflections are not a concern. ECL devices are designed specifically for (50Ω) transmission line networks. *Figure 4a* shows the databook load for ECL devices. This load is not only the test load for the device, it is also the specified load for the system environment. This load is a Thevenin equivalent and can be easily translated into an equivalent transmission line load (see *Figure 4b*). As was the case with the idealized TTL transmission line load *(Figure 1c)*, this load will transmit data cleanly with only the physical delay of the transmission line being a factor in propagation speeds.

Unlike the typical TTL application, the typical ECL application utilizes this loading scheme (see *Figure 4c*). Consequently, there are no reflections or distortions of the signal transitions. *Figure 5a* shows the IV curves of ECL output LOW and HIGH conditions. *Figure 5b* shows the resulting time domain reflection diagram. This signal is cleanly propagated along the network until it arrives at the end of the line. Due to the fact that it is a properly terminated transmission line, there is no reflection. Any input placed along the line wil see a clean signal transition delayed by the propagation delay of the line to that point! The worst case delay for the signal is t = T!

ECL Load Matching

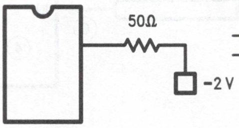

FIGURE 4a. Databook Load

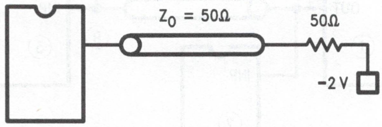

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FIGURE 4b. Transmission Line Match

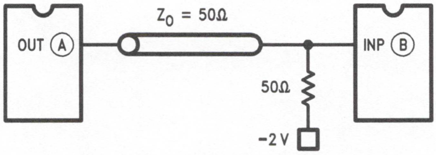

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FIGURE 4c. "Typical" Application

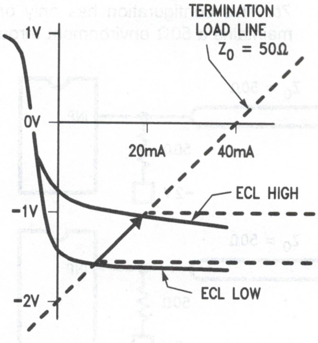
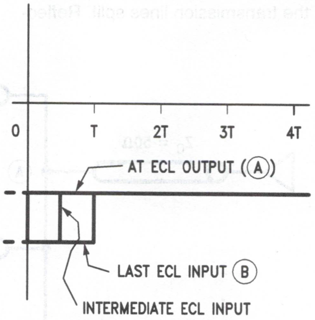


FIGURE 5a. ECL Transition to High State



TL/D/10098–8

FIGURE 5b. Reflection Diagram for Transition to High State

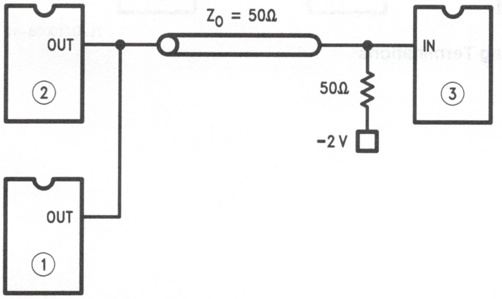
ECL System Design Considerations

Due to the terminated impedance environment required by ECL devices, there are a few basic routing rules which must be followed. Before designing an ECL system, an understanding of these basic routing conditions should be understood. Some of the basic considerations are discussed here; a more comprehensive discussion can be found in the National F100K ECL User's Handbook.

The most straight forward connection method was shown in *Figure 4c*. This method simply places a 50Ω resistor at the input to the next device to provide a series terminated load.

In some cases, it is desirable to connect several outputs to a common bus. This is particularly desirable for ECL devices since they have open emitter outputs and are specifically designed to be used in wired-or bus configurations. *Figure 6a* shows a typical "party line" connection. In this case, care must be taken to minimize the physical distance between the two outputs. If the distance is large enough, the signal line between the two outputs will act as a transmission line *(Figure 6b)*. For the output in device 1 this doesn't cause a problem, because it is at one end of the transmission line. However, device 2 is in the middle of the transmission line. The output in device 2 sees two transmission lines in parallel. The result is that the output sees the equivalent of a 25Ω transmission line for some length of time. This causes impedance mismatches at the terminated load and results in signal reflections.

Party Lines



TL/D/10098–9

FIGURE 6a

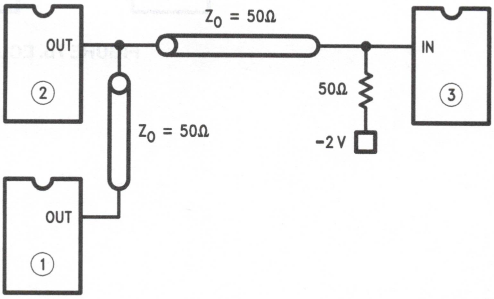


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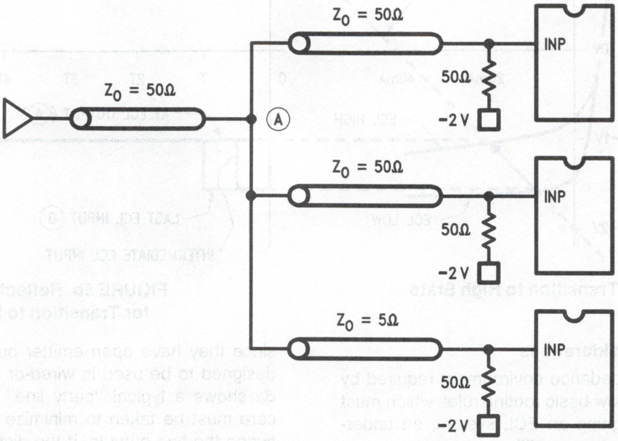
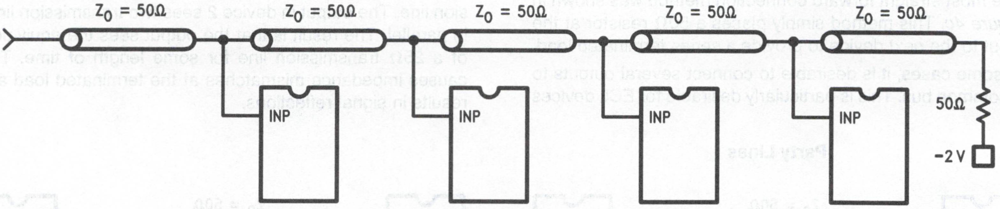
FIGURE 6b

Figure 7a shows an incorrect signal termination method. The parallel terminations cause the impedance that the device output sees to drop to 16.7Ω. An impedance mismatch occurs at node A where the transmission lines split. Reflections and disturbed signal integrity can result. A correct termination method for bus configurations is shown in *Figure 7b*. This configuration has only one terminated load and maintains a 50Ω environment throughout.


Z_0 = 50Ω
Ⓐ
Z_0 = 50Ω
INP
50Ω
-2 V
Z_0 = 50Ω
INP
50Ω
-2 V
Z_0 = 5Ω
INP
50Ω
-2 V

TL/D/10098–11

FIGURE 7a. Incorrect (For High Speed Applications)


Z_0 = 50Ω
Z_0 = 50Ω
Z_0 = 50Ω
Z_0 = 50Ω
Z_0 = 50Ω
INP
INP
INP
INP
50Ω
-2 V

TL/D/10098–12

FIGURE 7b. ECL Bussing Terminations

ECL PCB Design Considerations

In order to design a printed circuit board for an ECL system, many factors have to be considered. The ultimate goal is to develop a PCB with transmission line impedances as close to 50Ω as possible. In order to accomplish this, the geometry of the board itself and the properties of the ECL device must be considered.

Figure 8 shows a PCB cross-section of several μstrip transmission lines. The factors affecting the overall impedance of the board are the metal thicknesses, widths, heights, and spacings; and the dielectric constants and thicknesses of the dielectric materials. For example, the impedance of a microstrip line can be found from:

$$Z_O = [87/\sqrt{(e_r + 1.41)}]^* \ln [4.98h/(0.8w + t)]$$

where h = dielectric thickness, w = trace width, t = trace thickness, e_r = dielectric constant of board material relative to air.

This formula can be used to calculate the undisturbed or "unloaded" impedance of the PCB. Packaged devices have inherent capacitive and inductive characteristics which can load a PCB transmission line. What is desired from the system point of view is that the final or "loaded" impedance of the board is equal to 50Ω. The capacitance of the device affects the final impedance of the PCB. *Figure 9* shows a discrete RLCM model of the transmission line network shown in *Figure 8* and *Figure 10* shows the effect of adding a device to this network. Capacitors CD1, CD2 are the capacitances of two device inputs. These capacitors are parallel to the capacitors of the transmission line and thus increase the overall capacitance of the transmission line. The inductors (LD1, LD2) are the inductances of two device inputs. Though these inductors are parallel to the transmission line, they do not affect the overall characteristics of the transmission line because they lead into an open circuit (they device itself). Consequently, the dominant effect of adding devices to a PCB is the increased capacitance of the PCB.

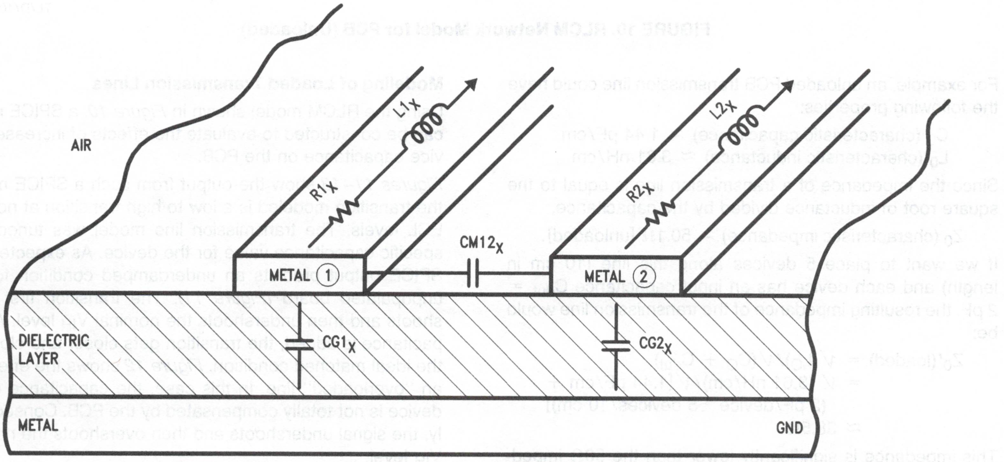


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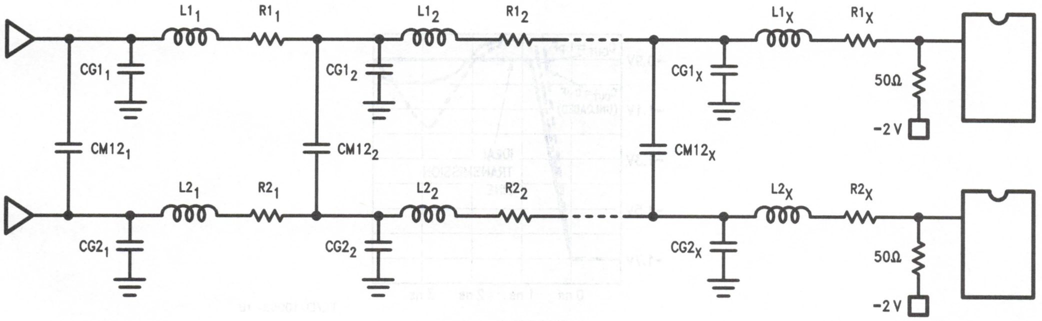
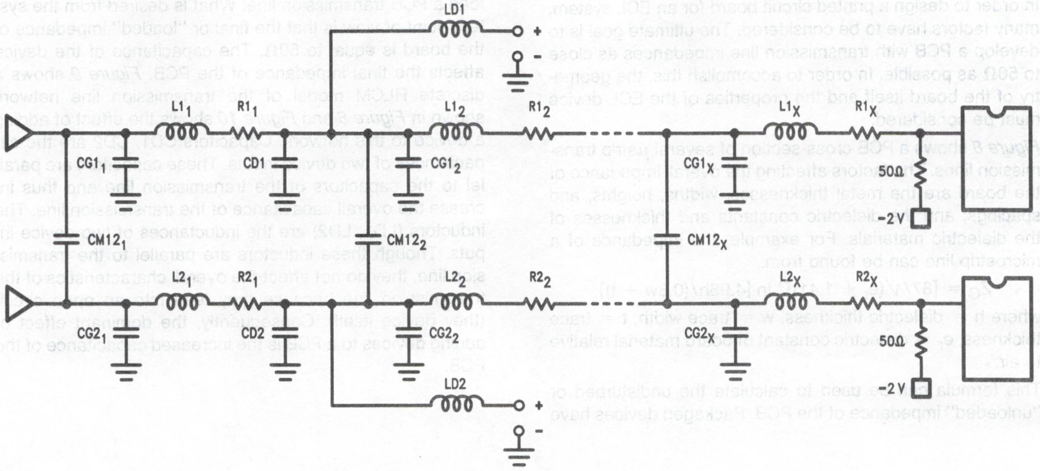
FIGURE 8. Geometric Model of PCB



TL/D/10098-14

FIGURE 9. RLCM Network Model for PCB (Unloaded)



TL/D/10098-15

FIGURE 10. RLCM Network Model for PCB (Unloaded)

For example, an unloaded PCB transmission line could have the following properties:

C_0 (characteristic capacitance) $\approx$ 1.44 pF/cm
L_0 (characteristic inductance) $\approx$ 3.61 nH/cm

Since the impedance of a transmission line is equal to the square root of inductance divided by the capacitance,

Z_0 (characteristic impedance) $\approx$ 50.1Ω [unloaded].

If we want to place 5 devices along this line (10 cm in length) and each device has an input capacitance C_{dut} = 2 pF, the resulting impedance of the transmission line would be:

$$\begin{aligned} Z_0'(\text{loaded}) &= \sqrt{}(L_O)/\sqrt{}(C_O + C_{dut}) \\ &= \sqrt{}(3.61\ \text{nH/cm})/\sqrt{}[1.44\ \text{pF/cm} + (2\ \text{pF/device} * 5\ \text{devices}/10\ \text{cm})] \\ &\approx 38.5\Omega \end{aligned}$$

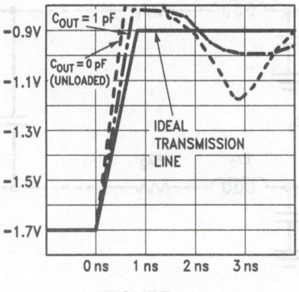
This impedance is significantly lower than the 50Ω impedance which is needed. Consequently, the designer must design his unloaded board to a sufficiently high impedance so that after the board is populated it will measure 50Ω.

Modeling of Loaded Transmission Lines

Using the RLCM model shown in *Figure 10*, a SPICE model can be constructed to evaluate the effects of increased device capacitance on the PCB.

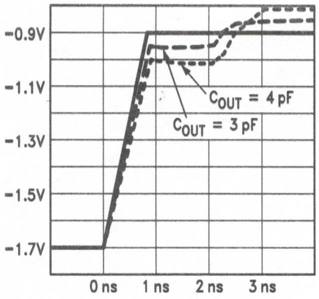
Figures 11–13 show the output from such a SPICE model; the transition modeled is a low to high transition at nominal ECL levels. The transmission line model was tuned to a specific capacitance value for the device. As expected, the SPICE output predicts an underdamped condition for the unpopulated board *(Figure 11)*. The transition first overshoots and then undershoots the nominal V_{IH} level. As capacitance is added, the transition gets closer and closer to the ideal matched condition. *Figure 12* shows the effects of an "overloaded" line. In this case, the capacitance of the device is not totally compensated by the PCB. Consequently, the signal undershoots and then overshoots the nominal V_{IH} level.

Figure 13 shows the resulting signal of a tuned "loaded" transmission line. Due to the design of the transmission line, the added capacitance of the device is compensated by the intentional addition of increased line inductance.



TL/D/10098-16

FIGURE 11



TL/D/10098-17

FIGURE 12

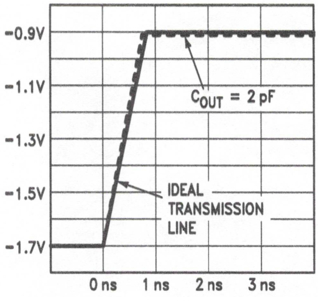


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FIGURE 13

Summary

For maximum performance, layout and construction requirements on printed circuit boards for next generation systems must become more demanding. While at first glance, designing with ECL devices poses more difficulties for a system designer than TTL devices, if the goal is to obtain high system performance then ECL devices offer significant advantages. Because of the fact that they are designed specifically for high speed environments, the ECL device is easier to integrate into a high speed system. With the geometries and characteristics of the printed circuit board and the device considered as a unit, a network can be designed to produce a clean controlled impedance environment for an ECL device much easier than for a comparable TTL device.

Section 5

TTL I/O Static RAMs

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National Semiconductor

TTL I/O-MOS Static RAM Selection Guide

Part Number	Organization	Outputs	Pins	Access Time	Temperature Range
TTL I/O STATIC RAMS					
DM54S189	16 x 4	TS	16	50	−55°C to +125°C
DM54S189A	16 x 4	TS	16	30	−55°C to +125°C
DM74S189	16 x 4	TS	16	35	0°C to +70°C
DM74S189A	16 x 4	TS	16	25	0°C to +70°C
DM74S289	16 x 4	OC	16	35	0°C to +70°C
93L415A	1k x 1	OC	16	25 ns	0°C to +70°C
93L422A	256 x 4	TS	22	25 ns	0°C to +70°C
93L425A	1k x 1	TS	16	25 ns	0°C to +70°C
93479	256 x 9	TS	22	25 ns	0°C to +70°C
MOS STATIC RAMS					
NMC2147H	4k x 1	TS	18	70	0°C to +70°C
NMC2147H-3	4k x 1	TS	18	55	0°C to +70°C
NMC2147H-2	4k x 1	TS	18	45	0°C to +70°C
NMC2147H-1	4k x 1	TS	18	35	0°C to +70°C
NMC2147H-3L	4k x 1	TS	18	55	0°C to +70°C
NMC2148H	1k x 4	TS	18	70	0°C to +70°C
NMC2148H-3	1k x 4	TS	18	55	0°C to +70°C
NMC2148H-2	1k x 4	TS	18	45	0°C to +70°C
NMC2148H-1	1k x 4	TS	18	70	0°C to +70°C
NMC2148H-3L	1k x 4	TS	18	55	0°C to +70°C
EDGE-TRIGGERED REGISTERS					
DM75S68	16k x 4	TS	16	55	−55°C to +125°C
DM75S68A	16k x 4	TS	16	45	−55°C to +125°C
DM85S68	16k x 4	TS	16	40	0°C to +70°C
DM85S68A	16k x 4	TS	16	24	0°C to +70°C

National Semiconductor

DM54S189/DM74S189 64-Bit (16 x 4) TRI-STATE® RAM DM54S189A/DM74S189A High Speed 64-Bit TRI-STATE RAM

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs; yet it retains the fast rise time characteristics of the TTL totem-pole output. Systems utilizing data bus lines with a defined pull-up impedance can employ the open-collector DM74S289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM74S189 outputs are bus connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable is high, the outputs will be in the high-impedance state.

The fast access time of the DM74S189A makes it particularly attractive for implementing high-performance memory functions requiring access times less than 25 ns. The high capacitive drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM74S189A outputs being at a high-impedance during writing, combined with the data inputs being inhibited during reading, means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Features

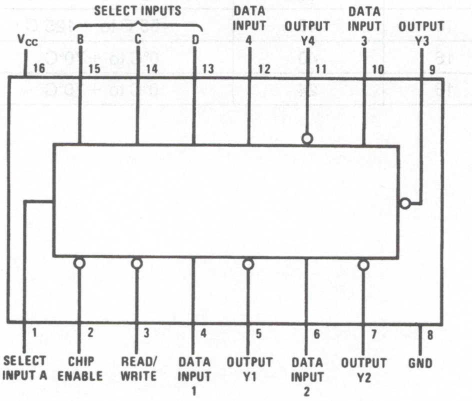
- Schottky-clamped for high speed applications (S189A)

Access from chip-enable input	17 ns max
Access from address inputs	25 ns max

- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads (S189, S189A)
- DM74S289 are functionally equivalent and have open-collector outputs
- DM54SXXX is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL circuits
- Chip-enable input simplifies system decoding

Connection Diagram

Dual-In-Line Package



TL/D/9232–1

Top View

Truth Table

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write (Store Complement of Data)	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level, L = Low Level, X = Don't Care

Order Number DM54S189J, DM54S189AJ, DM74S189J, DM74S189AJ, DM74S189N or DM74S189AN See NS Package Number J16A or N16E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM54S189	4.5	5.5	V
DM74S189	4.75	5.25	V
Temperature (T_A)			
DM54S189	−55	+125	°C
DM74S189	0	+70	°C

DM54S189, DM74S189 Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM54S189	2.4	3.4		V
			I_{OH} = −6.5 mA, DM74S189	2.4	3.2		V
I_{CEX}	High Level Output Current Open Collector Only	V_{CC} = Min	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM54S189			0.5	V
			DM74S189			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V	DM54S189, DM74S189	−30		−100	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	110	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V	DM54S189, DM74S189			50	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.45V	DM54S189, DM74S189	−50			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "Off"			6.0		pF

DM74S189 Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S189			DM74S189			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{AA}	Access Times from Address		C_L = 30 pF, R_L = 280Ω (*Figure 4*)		25	50		25	35	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	C_L = 5 pF, R_L = 280Ω (*Figure 4*)		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time (*Figure 1*)	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time (*Figure 1*)	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM54S189(A)	4.5	5.5	V
DM74S189(A)	4.75	5.25	V
Temperature (T_A)			
DM54S189(A)	−55	+125	°C
DM74S189(A)	0	+70	°C

DM54S189A, DM74S189A Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM54S189A	2.4	3.4		V
			I_{OH} = −6.5 mA, DM74S189A	2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 16 mA			0.45	V
			I_{OL} = 20 mA			0.5	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.40V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V		−20		−90	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V				40	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.4V		−40			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "Off"			6.0		pF

DM54S189A, DM74S189A Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S189A			DM74S189A			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{AA}	Access Time from Address		C_L = 30 pF, R_L = 280Ω *(Figure 4)*		20	30		20	25	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			11	25		11	17	ns
t_{CZL}	Output Enable Time to Low Level				11	25		11	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	C_L = 5 pF, R_L = 280Ω *(Figure 4)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			20			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			20			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time *(Figure 1)*	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189(A) and across the 0°C to +70°C range for the DM74S189(A). All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

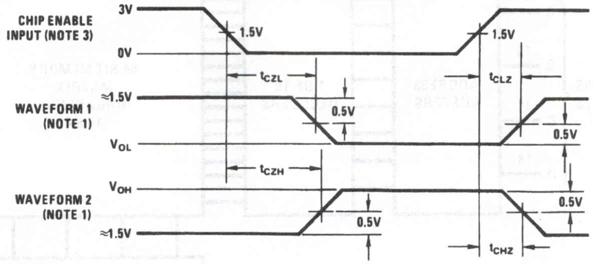
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded; and the outputs open.

DM54S189(A), DM74S189(A) Switching Time Waveforms

Enable and Disable Time from Chip-Enable


CHIP ENABLE INPUT (NOTE 3)
3V
0V
1.5V
1.5V
t_{CZL}
t_{CLZ}
WAVEFORM 1 (NOTE 1)
≈1.5V
V_{OL}
0.5V
0.5V
t_{CZH}
WAVEFORM 2 (NOTE 1)
V_{OH}
≈1.5V
0.5V
0.5V
t_{CHZ}

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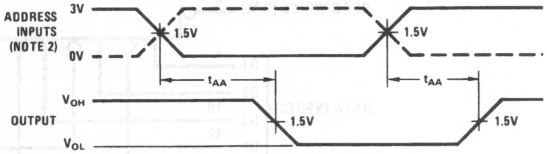
Access Time from Address Inputs


ADDRESS INPUTS (NOTE 2)
3V
0V
1.5V
1.5V
t_{AA}
t_{AA}
OUTPUT
V_{OH}
V_{OL}
1.5V
1.5V

TL/D/9232-3

Write Cycle

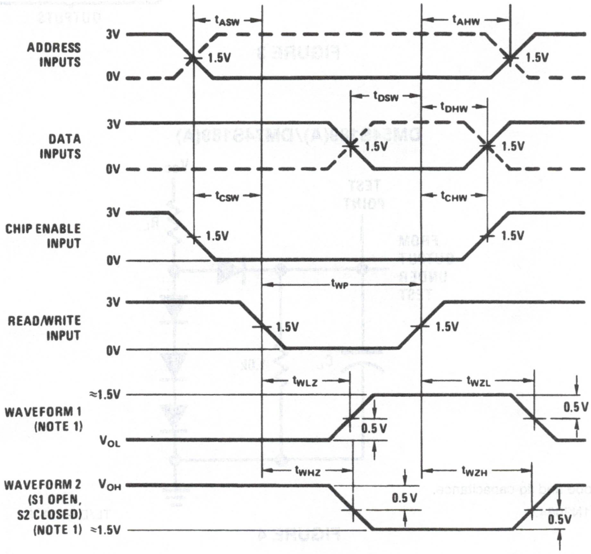

t_{ASW}
t_{AHW}
ADDRESS INPUTS
3V
0V
1.5V
1.5V
t_{DSW}
t_{DHW}
DATA INPUTS
3V
0V
1.5V
1.5V
t_{CSW}
t_{CHW}
CHIP ENABLE INPUT
3V
0V
1.5V
1.5V
t_{WP}
READ/WRITE INPUT
3V
0V
1.5V
1.5V
t_{WLZ}
t_{WZL}
WAVEFORM 1 (NOTE 1)
≈1.5V
V_{OL}
0.5V
0.5V
t_{WHZ}
t_{WZH}
WAVEFORM 2 (S1 OPEN, S2 CLOSED) (NOTE 1)
V_{OH}
≈1.5V
0.5V
0.5V

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FIGURE 1

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

Note 2: When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} = \approx 50\Omega$.

Block Diagram

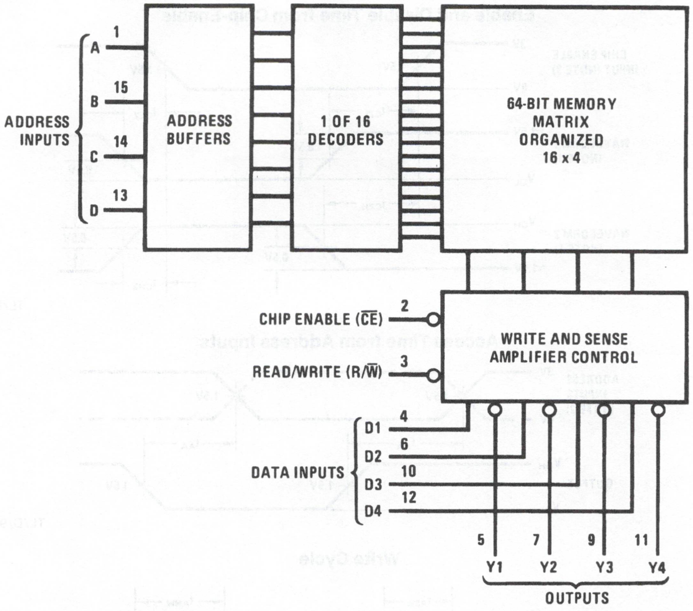
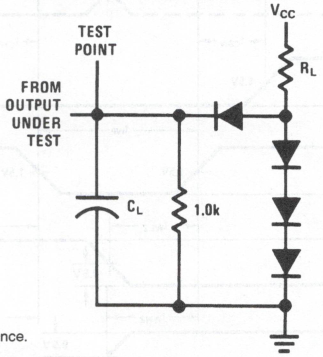

ADDRESS INPUTS
A
1
B
15
C
14
D
13
ADDRESS BUFFERS
1 OF 16 DECODERS
64-BIT MEMORY MATRIX ORGANIZED 16 x 4
CHIP ENABLE ($\overline{CE}$)
2
READ/WRITE (R/$\overline{W}$)
3
WRITE AND SENSE AMPLIFIER CONTROL
DATA INPUTS
D1
4
D2
6
D3
10
D4
12
5
7
9
11
Y1
Y2
Y3
Y4
OUTPUTS
TL/D/9232-5

FIGURE 3

AC Test Circuits

DM54S189(A)/DM74S189(A)


V_{CC}
TEST POINT
R_L
FROM OUTPUT UNDER TEST
C_L
1.0k

C_L includes probe and jig capacitance.

All diodes are 1N3064.

TL/D/9232-6

FIGURE 4

National Semiconductor

DM74S289
64-Bit (16 x 4) Open-Collector RAM TRI-STATE® RAM

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −25 mA, only one-eighth that of a DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM74S289 outputs are bus connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

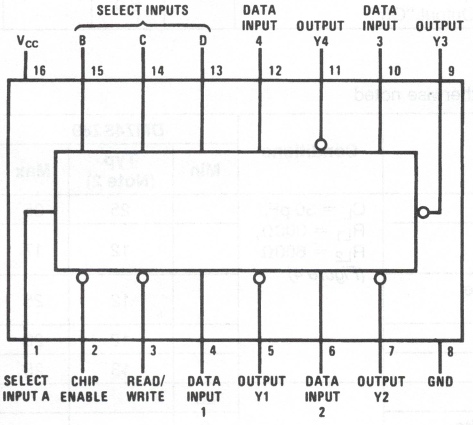
Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable is high, the outputs will be in the high-impedance state.

Features

- Commercial address access time 25 ns
- Features open-collector output
- Compatible with most TTL circuits
- Chip-enable input simplifies system decoding

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DM74S289J or DM74S289N
See NS Package Number J16A or N16E

Truth Table

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write (Store Complement of Data)	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 Sec.)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM74S289	4.75	5.25	V
Temperature (T_A)			
DM74S289	0	+70	°C

DM74S289 Electrical Characteristics

Over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −6.5 mA	2.4	3.2		V
I_{CEX}	High Level Output Current	V_{CC} = Min	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA				0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{CC}	Supply Current (Note 4)	V_{CC} = Max			75	110	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "Off"			6.0		pF

DM74S289 Switching Characteristics

Over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM74S289			Units
				Min	Typ (Note 2)	Max	
t_{AA}	Access Time from Address		C_L = 30 pF, R_{L1} = 300Ω, R_{L2} = 600Ω *(Figure 4)*		25	35	ns
t_{CHL}	Enable Time from Chip-Enable				12	17	ns
t_{WHL}	Enable Time from Read/Write	Sense Recovery Time from Read/Write			12	25	ns
t_{CLH}	Disable Time from Chip-Enable				12	20	ns
t_{WLH}	Disable Time from Read/Write				13	25	ns
t_{WP}	Width of Enable Pulse (Read/Write Low)			25			ns
t_{ASW}	Setup Time *(Figure 2)*	Address to Read/Write		0			ns
t_{DSW}		Data to Read/Write		25			ns
t_{CSW}		Chip-Enable to Read/Write		0			ns
t_{AHW}	Hold Time *(Figure 2)*	Address from Read/Write		0			ns
t_{DHW}		Data from Read/Write		0			ns
t_{CHW}		Chip-Enable from Read/Write		0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics provides conditions for actual device operation.

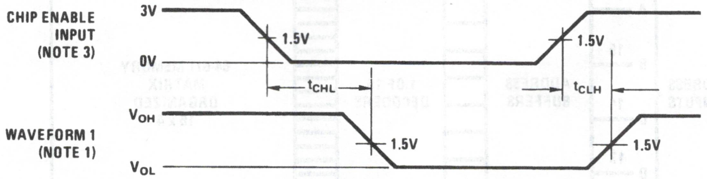
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189 and across the 0°C to −70°C range for the DM74S189/289. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: I_{CC} is measured with all inputs grounded, and the outputs open.

DM74S289 Switching Time Waveforms

Enable and Disable Time from Chip-Enable


CHIP ENABLE
INPUT
(NOTE 3)
3V
0V
1.5V
1.5V
t_{CHL}
t_{CLH}
WAVEFORM 1
(NOTE 1)
V_{OH}
V_{OL}
1.5V
1.5V

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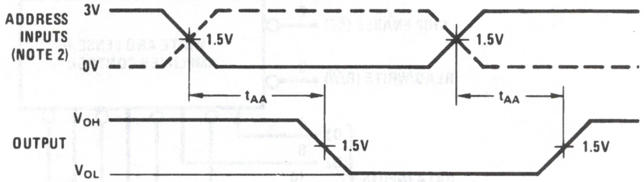
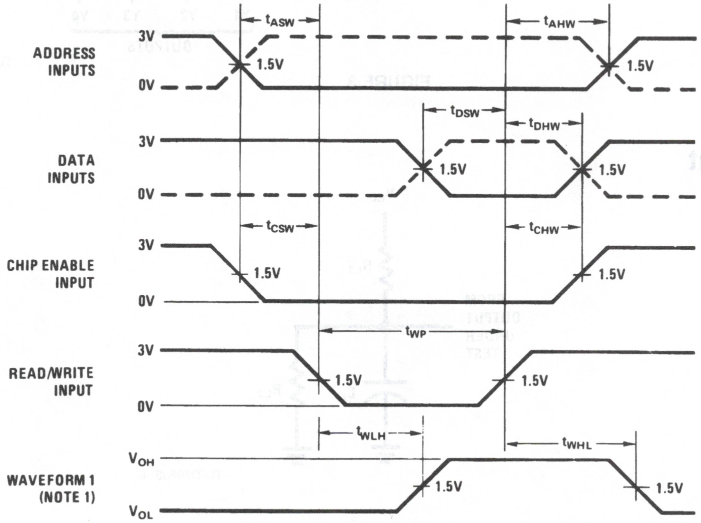
Access Time from Address Inputs


ADDRESS
INPUTS
(NOTE 2)
3V
0V
1.5V
1.5V
t_{AA}
t_{AA}
OUTPUT
V_{OH}
V_{OL}
1.5V
1.5V

TL/D/9693–3

Write Cycle


t_{ASW}
t_{AHW}
ADDRESS
INPUTS
3V
0V
1.5V
1.5V
t_{DSW}
t_{DHW}
DATA
INPUTS
3V
0V
1.5V
1.5V
t_{CSW}
t_{CHW}
CHIP ENABLE
INPUT
3V
0V
1.5V
1.5V
t_{WP}
READ/WRITE
INPUT
3V
0V
1.5V
1.5V
t_{WLH}
t_{WHL}
WAVEFORM 1
(NOTE 1)
V_{OH}
V_{OL}
1.5V
1.5V

TL/D/9693–4

FIGURE 2

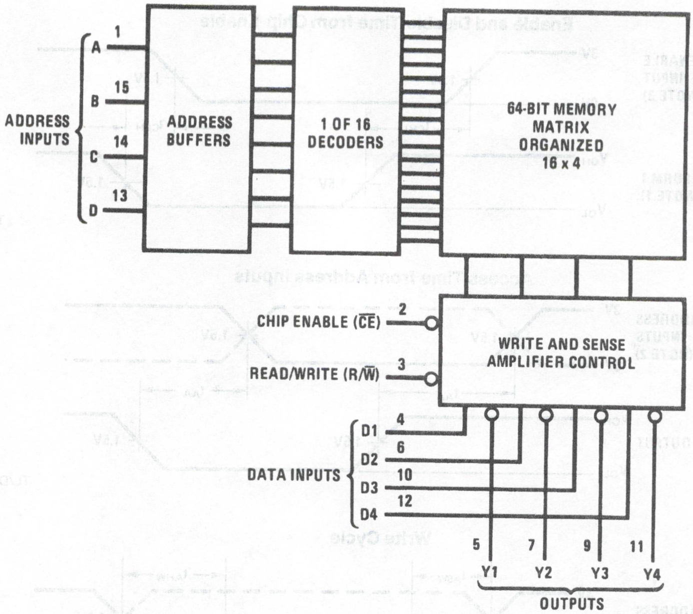
Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled.

Note 2: When measuring delay times from address inputs, the chip-enable is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. PRR $\leq$ 1 MHz and $Z_{OUT} = 50\Omega$.

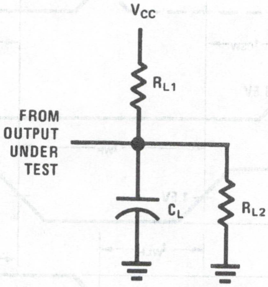
Block Diagram


ADDRESS INPUTS
A
1
B
15
C
14
D
13
ADDRESS BUFFERS
1 OF 16 DECODERS
64-BIT MEMORY MATRIX ORGANIZED 16 x 4
CHIP ENABLE ($\overline{CE}$)
2
READ/WRITE (R/$\overline{W}$)
3
WRITE AND SENSE AMPLIFIER CONTROL
DATA INPUTS
D1
4
D2
6
D3
10
D4
12
5
7
9
11
Y1
Y2
Y3
Y4
OUTPUTS

TL/D/9693-5

FIGURE 3

AC Test Circuit


V_{CC}
R_{L1}
FROM OUTPUT UNDER TEST
C_L
R_{L2}

TL/D/9693-6

National Semiconductor

93L415A 1024 x 1-Bit Static Random Access Memory

General Description

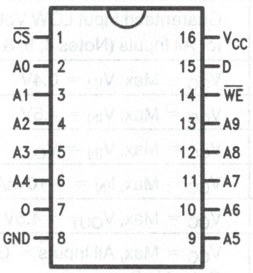
The 93L415A is a 1024-bit read write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

Features

- New design to replace old 93415/93L415
- Improved ESD thresholds
- Alpha hard without die coat
- Commercial address access time
  93L415A 25 ns max
- Features open collector output
- Power dissipation decreases with increasing temperature

Connection Diagram

16-Pin DIP



$\overline{CS}$ 1
A0 2
A1 3
A2 4
A3 5
A4 6
O 7
GND 8
16 V_{CC}
15 D
14 $\overline{WE}$
13 A9
12 A8
11 A7
10 A6
9 A5

TL/D/10003–1

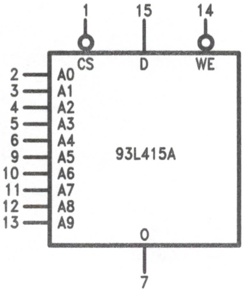
Top View

Order Number 93L415ADC or 93L415APC
See NS Package Number J16A* and N16E*

Optional Processing QR = Burn-In

*For most current package information, contact product marketing.

Logic Symbol



1
15
14
$\overline{CS}$
D
$\overline{WE}$
2 A0
3 A1
4 A2
5 A3
6 A4
9 A5
10 A6
11 A7
12 A8
13 A9
93L415A
O
7

TL/D/10003–3

V_{CC} = Pin 16
GND = Pin 8

Pin Names

$\overline{CS}$	Chip Select Input Active LOW
A0–A9	Address Inputs
$\overline{WE}$	Write Enable Input Active LOW
D	Data Input
O	Data Output

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Note 1)	−0.5V to V_{CC}
Input Current (DC)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Note 2)	−0.5V to 5.5V
Lead Temperature (Soldering, 10 sec.)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	
Commercial	5.0V ±5%
Case Temperature (T_C)	
Commercial	0°C to +75°C

DC Characteristics over operating temperature ranges (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 16 mA			0.45	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5, & 6)	2.1			
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5, & 6)			0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V		−180	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 4.5V		1.0	40	μA
I_{IHB}	Input Breakdown Current	V_{CC} = Max, V_{IN} = V_{CC}			1.0	mA
V_{IC}	Input Diode Clamp Voltage	V_{CC} = Max, I_{IN} = −10 mA		−1.0	−1.5	V
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{OUT} = 4.5V		1.0	100	μA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs = GND Output is Open			65	mA

AC Electrical Characteristics (Note 6) $V_{CC} = 5.0 \pm 5\%$, GND = 0V, $T_C = 0°C$ to $+75°C$

Symbol	Parameter	Conditions	Min	Max	Units
READ TIMING					
t_{ACS}	Chip Select Access Time	*Figures 3a, 3b*		15	ns
t_{RCS}	Chip Select Recovery Time			15	ns
t_{AA}	Address Access Time (Note 7)			25	ns
WRITE TIMING					
t_W	Write Pulse Width to Guarantee Writing (Note 8)	*Figure 4*	20		ns
t_{WSD}	Data Setup Time Prior to Write		5		ns
t_{WHD}	Data Hold Time after Write		5		ns
t_{WSA}	Address Setup Time Prior to Write (Note 8)		5		ns
t_{WHA}	Address Hold Time after Write		5		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		ns
t_{WS}	Write Enable to Output Disable			15	ns
t_{WR}	Write Recovery Time			15	ns

Note 1: Either input voltage limit or input current limit sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at $V_{CC} = 5.0V$, $T_C = +25°C$ and maximum loading.

Note 4: Tested under static condition only.

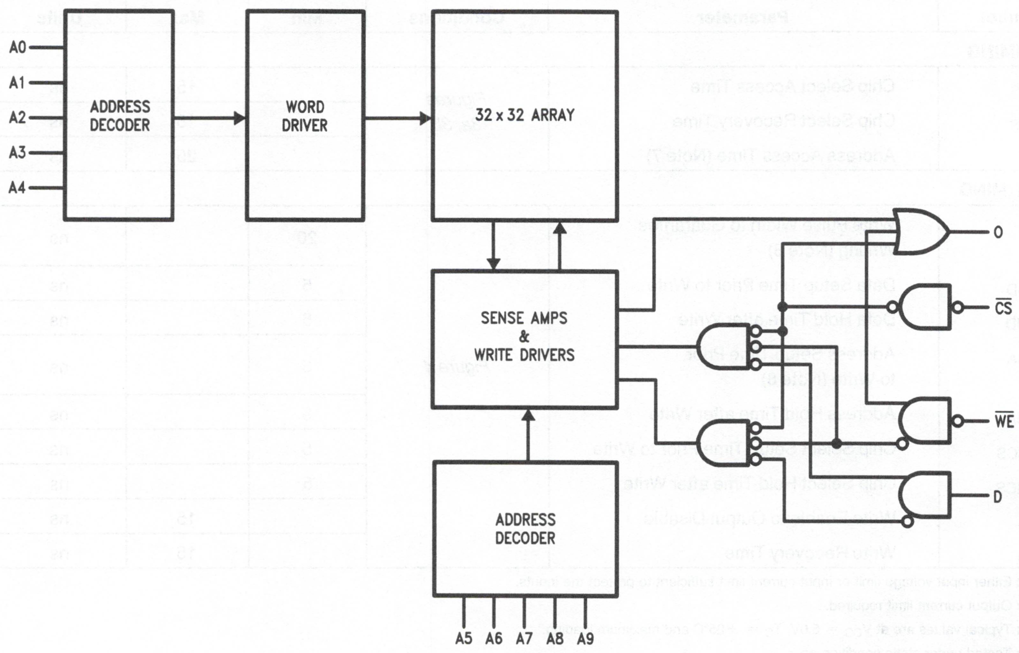
Note 5: Functional testing done at input levels $V_{IL} = 0.45V$ (V_{OL} Max) and $V_{IH} = 2.4V$ (V_{OH} Min).

Note 6: AC testing done at input levels $V_{IH} = 3V$, $V_{IL} = 0V$.

Note 7: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 8: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

Logic Diagram



TL/D/10003-2

Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level: 2.4V
L = LOW Voltage Level: 0.45V
X = Don't Care (HIGH or LOW)

Functional Description

The 93L415A is a fully decoded 1024-bit read/write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address A0 through A9.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories, the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93L415A are controlled by the state of the active low chip select ($\overline{CS}$) input. The write function is controlled by the active low write enable ($\overline{WE}$) input. With $\overline{CS}$ held low and $\overline{WE}$ held low, the data (D) is written into the memory location specified by addresses (A0 through A9). To assure a valid write, data setup (t_{WSD}), address setup (t_{WSA}), data hold (t_{WHD}), and address hold (t_{WHA}) times must be met. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output O.

An open collector output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93L415As can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output when the chip is deselected. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}\,(\text{Max})}{I_{OL} - \text{FO}\,(1.6)} \leq R_L \leq \frac{V_{CC}\,(\text{Min}) - V_{OH}}{n\,(I_{CEX}) + \text{FO}\,(0.04)}$$

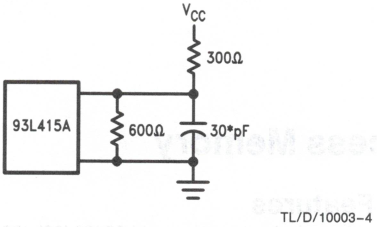
R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by the output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

One Unit Load = 40 μA HIGH/1.6 mA LOW.

FO_{MAX} = 5 UL.

Functional Description (Continued)


V_CC
300Ω
93L415A
600Ω
30*pF
TL/D/10003-4

*Includes jig and probe capacitance

FIGURE 1. AC Test Circuit

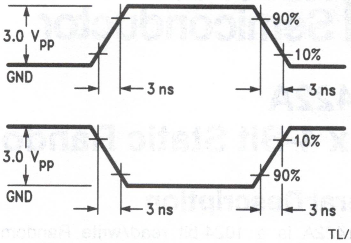
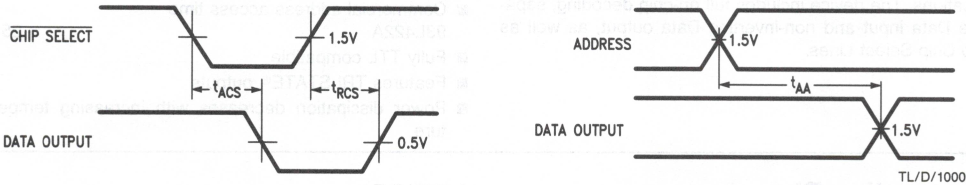

3.0 V_PP
GND
90%
10%
3 ns
3 ns
3.0 V_PP
GND
10%
90%
3 ns
3 ns
TL/D/10003-5

FIGURE 2. AC Test Input Levels


CHIP SELECT
1.5V
t_ACS
t_RCS
DATA OUTPUT
0.5V
TL/D/10003-6
ADDRESS
1.5V
t_AA
DATA OUTPUT
1.5V
TL/D/10003-7

a. Read Mode Propagation Delay from Chip Select

b. Read Mode Propagation Delay from Address Valid

FIGURE 3. Read Mode Timing

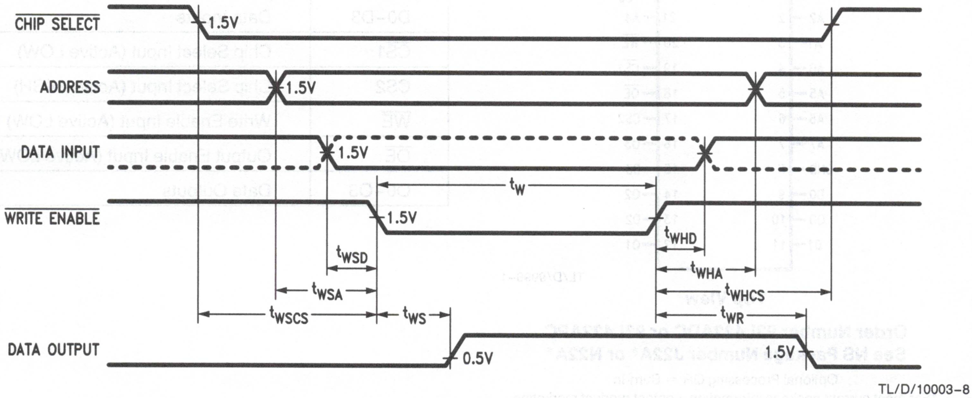

CHIP SELECT
1.5V
ADDRESS
1.5V
DATA INPUT
1.5V
WRITE ENABLE
1.5V
t_W
t_WSD
t_WSA
t_WSCS
t_WS
t_WHD
t_WHA
t_WHCS
t_WR
DATA OUTPUT
0.5V
1.5V
TL/D/10003-8

FIGURE 4. Write Mode Timing

Note 1: Timing Diagram represents one solution which results in an optimium cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0V/0V.

National Semiconductor

93L422A
256 x 4-Bit Static Random Access Memory

General Description

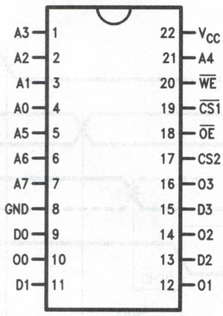
The 93L422A is a 1024-bit read/write Random Access Memory (RAM) organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as two Chip Select Lines.

Features

- New design to replace old 93422/93L422
- Improved ESD thresholds
- Alpha hard without die coat
- Commercial address access time
  93L422A 25 ns
- Fully TTL compatible
- Features TRI-STATE® outputs
- Power dissipation decreases with increasing temperature

Connection Diagram

22-Pin DIP



A3 1
A2 2
A1 3
A0 4
A5 5
A6 6
A7 7
GND 8
D0 9
O0 10
D1 11
22 V$_{CC}$
21 A4
20 $\overline{WE}$
19 $\overline{CS1}$
18 $\overline{OE}$
17 CS2
16 O3
15 D3
14 O2
13 D2
12 O1

TL/D/9996-1

Top View

Order Number 93L422ADC or 93L422APC
See NS Package Number J22A* or N22A*

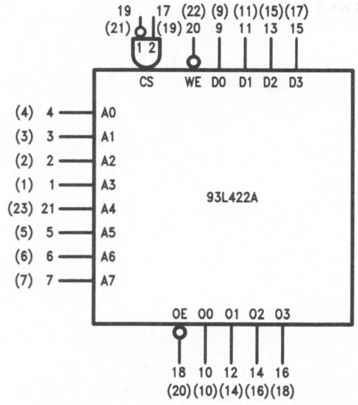
Optional Processing QR = Burn-In

*For most current package information, contact product marketing

Pin Names

A0–A7	Address Inputs
D0–D3	Data Inputs
$\overline{CS1}$	Chip Select Input (Active LOW)
CS2	Chip Select Input (Active HIGH)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
O0–O3	Data Outputs

Logic Symbol



19 (21)
17 (19)
(22) 20
(9) 9
(11) 11
(15) 13
(17) 15
1 2
CS
WE
D0
D1
D2
D3
(4) 4 A0
(3) 3 A1
(2) 2 A2
(1) 1 A3
(23) 21 A4
(5) 5 A5
(6) 6 A6
(7) 7 A7
93L422A
OE O0 O1 O2 O3
18 10 12 14 16
(20) (10) (14) (16) (18)

TL/D/9996-3

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Note 1)	−0.5V to V_{CC}
Input Current (DC)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Note 2)	−0.5V to +5.5V
Lead Temperature (Soldering, 10 sec.)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	5.0V ±5%
Case Temperature (T_C)	0°C to +75°C

DC Characteristics over operating temperature ranges (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8 mA		0.3	0.45	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5 & 6)	2.1			
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5 & 6)			0.8	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −5.2V	2.4			V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V		−150	−300	µA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 4.5V		1.0	40	µA
I_{IHB}	Input Breakdown Current	V_{CC} = Max, V_{IN} = V_{CC}			1.0	mA
V_{IC}	Input Diode Clamp Voltage	V_{CC} = Max, I_{IN} = −10 mA		−1.0	−1.5	V
I_{OZH}	Output Current (HIGH Z)	V_{CC} = Max, V_{OUT} = 2.4V			50	µA
I_{OZL}		V_{CC} = Max, V_{OUT} = 0.5V			−50	µA
I_{OS}	Output Current Short Circuit to Ground	V_{CC} = Max (Note 7)	−10		−70	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All Outputs Open, All Inputs = GND			80	mA

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C

Symbol	Parameter	Conditions	Min	Max	Units
READ TIMING					
t_{ACS}	Chip Select Access Time	*Figures 3a, 3b, 3c*		20	ns
t_{ZRCS}	Chip Select to High Z			20	ns
t_{AOS}	Output Enable Access Time			20	ns
t_{ZROS}	Output Enable to HIGH Z			20	ns
t_{AA}	Address Access Time (Note 8)			25	ns
WRITE TIMING					
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*Figure 4*	20		ns
t_{WSD}	Data Setup Time prior to Write		5		ns
t_{WHD}	Data Hold Time after Write		5		ns
t_{WSA}	Address Setup Time prior to Write (Note 9)		5		ns
t_{WHA}	Address Hold Time after Write		5		ns
t_{WSCS}	Chip Select Setup Time prior to Write		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		ns
t_{ZWS}	Write Enable to Output Disable			20	ns
t_{WR}	Write Recovery Time			20	ns

Note 1: Either input voltage limit or input current limit sufficient to protecting inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V, t_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels V_{IL} = 0.45V (V_{OL} Max) and V_{IH} = 2.4V (V_{OH} Min).

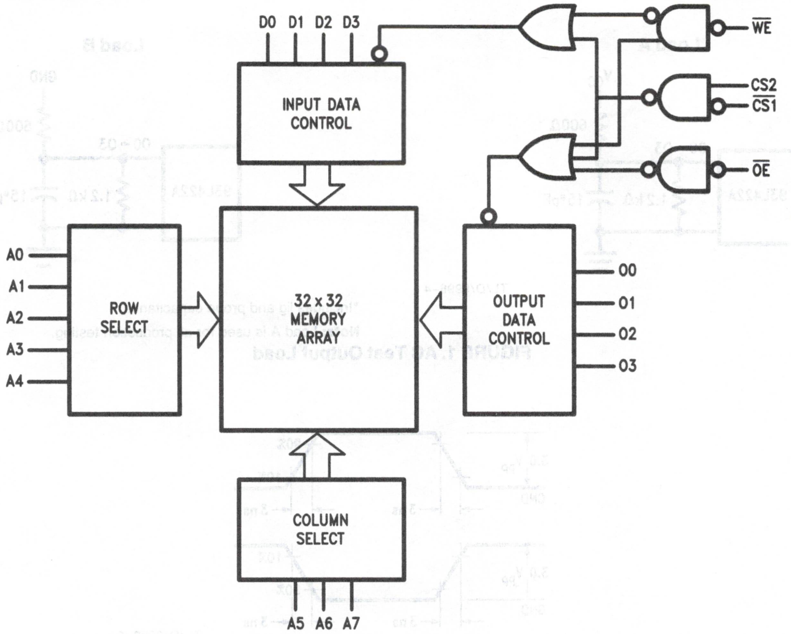
Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second; ground only one output at a time.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

Logic Diagram



TL/D/9996-2

Truth Table

Inputs				Outputs	
OE	**CS1**	**CS2**	**WE**	**TRI-STATE**	**Mode**
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D_{OUT}	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level 2.4V
L = LOW Voltage Level 0.45V
X = Don't Care HIGH or LOW
HIGH Z = High-Impedance

Functional Description

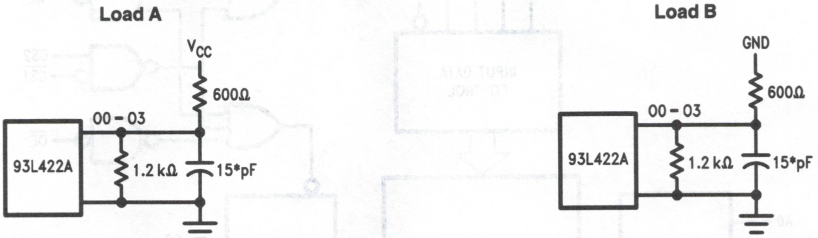
The 93L422A is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address A0–A7.

Two Chip Select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of the chip selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable WE input. When WE is held LOW and the chip is selected, the data at D0–D3 is written into the address location. Since the write function is level-triggered, data must be held stable for at least $t_{WSD\ (Min)}$ plus $t_{W\ (Min)}$ plus $t_{WHD\ (Min)}$ to insure a valid write. To read, WE is held high, the chip is selected, and the data is transferred to the outputs (O0–O3).

The 93L422A has TRI-STATE outputs which provide active pull-ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Functional Description (Continued)


Load A
VCC
600Ω
00-03
93L422A
1.2 kΩ
15*pF
Load B
GND
600Ω
00-03
93L422A
1.2 kΩ
15*pF

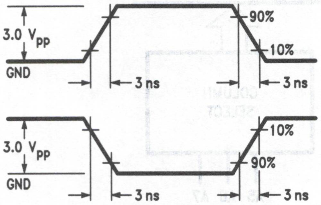
TL/D/9996-4

TL/D/9996-5

*Includes jig and probe capacitance

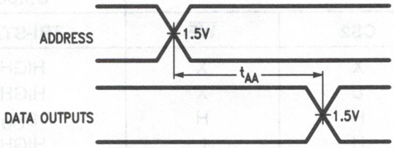
Note: Load A is used for all production testing.

FIGURE 1. AC Test Output Load


3.0 VPP
GND
90%
10%
3 ns
3 ns
3.0 VPP
GND
10%
90%
3 ns
3 ns

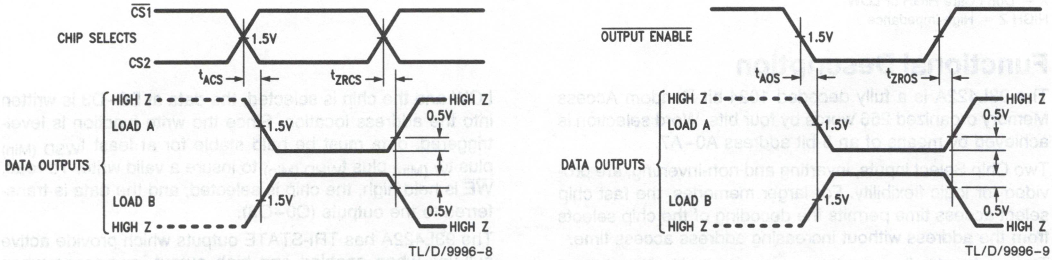
TL/D/9996-6

FIGURE 2. AC Test Input Levels


ADDRESS
1.5V
tAA
DATA OUTPUTS
1.5V

TL/D/9996-7

3a. Read Mode Propagation Delay from Address


CS1
CHIP SELECTS
CS2
1.5V
tACS
tZRCS
HIGH Z
LOAD A
1.5V
HIGH Z
0.5V
DATA OUTPUTS
LOAD B
1.5V
0.5V
HIGH Z
HIGH Z
OUTPUT ENABLE
1.5V
tAOS
tZROS
HIGH Z
LOAD A
1.5V
HIGH Z
0.5V
DATA OUTPUTS
LOAD B
1.5V
0.5V
HIGH Z
HIGH Z

TL/D/9996-8

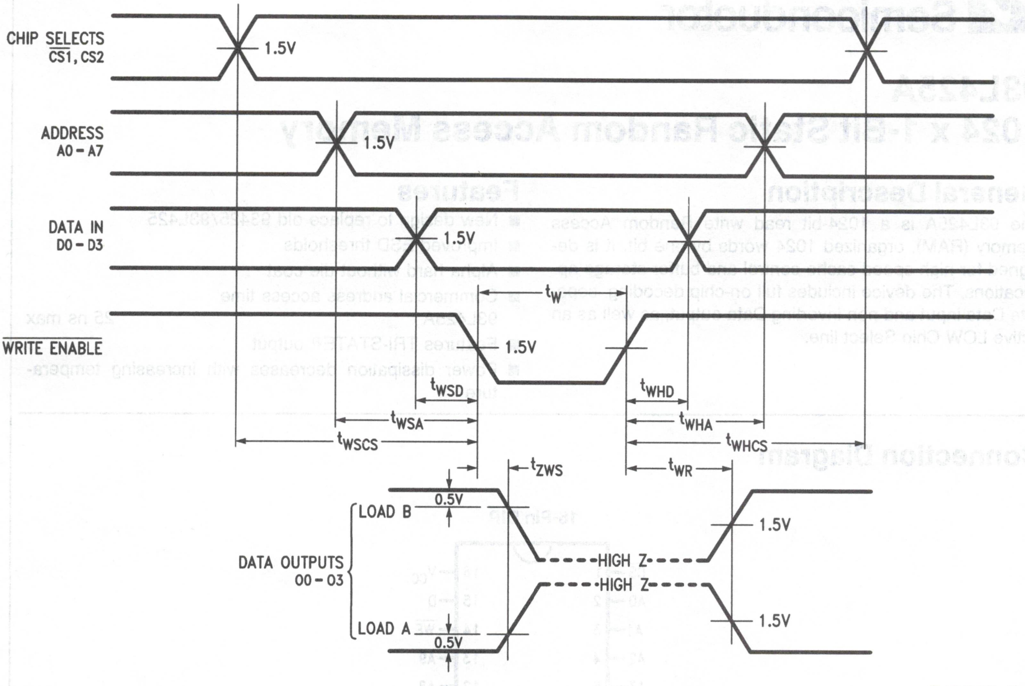
3b. Read Mode Propagation Delay from Chip Select

TL/D/9996-9

3c. Read Mode Propagation Delay from Output Enable

FIGURE 3. Read Mode Testing

Functional Description (Continued)


CHIP SELECTS
CS1, CS2
ADDRESS
A0 - A7
DATA IN
D0 - D3
WRITE ENABLE
1.5V
1.5V
1.5V
1.5V
t_W
t_{WSD}
t_{WHD}
t_{WSA}
t_{WHA}
t_{WSCS}
t_{WHCS}
t_{ZWS}
t_{WR}
LOAD B
0.5V
DATA OUTPUTS
O0 - O3
HIGH Z
HIGH Z
1.5V
1.5V
LOAD A
0.5V

TL/D/9996-10

FIGURE 4. Write Mode Timing

Note 1: Timing Diagram represents one solution which results in an optimium cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0V–0V.

National Semiconductor

93L425A
1024 x 1-Bit Static Random Access Memory

General Description

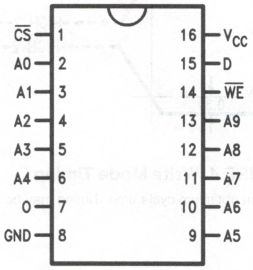
The 93L425A is a 1024-bit read write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

Features

- New design to replace old 93425/93L425
- Improved ESD thresholds
- Alpha hard without die coat
- Commercial address access time
  93L425A 25 ns max
- Features TRI-STATE® output
- Power dissipation decreases with increasing temperature

Connection Diagram

16-Pin DIP


$\overline{CS}$ 1
A0 2
A1 3
A2 4
A3 5
A4 6
O 7
GND 8
16 V_{CC}
15 D
14 $\overline{WE}$
13 A9
12 A8
11 A7
10 A6
9 A5

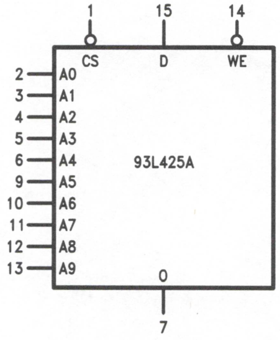
TL/D/10004–1

Top View

Order Number 93L425ADC or 93L425APC
See NS Package Number J16A* or N16E*

Optional Processing QR = Burn-In
*For most current package information, contact product marketing.

Logic Symbol


1
15
14
CS
D
WE
2 A0
3 A1
4 A2
5 A3
6 A4
9 A5
10 A6
11 A7
12 A8
13 A9
93L425A
O
7

V_{CC} = Pin 16
GND = Pin 8

TL/D/10004–3

Pin Names

$\overline{CS}$	Chip Select (Active LOW)
A0–A9	Address Inputs
$\overline{WE}$	Write Enable Input (Active LOW)
D	Data Input
O	Data Output

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Note 1)	−0.5V to V_{CC}
Input Current (DC)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Note 2)	−0.5V to 5.5V
Lead Temperature (Soldering, 10 sec.)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	
Commercial	5.0V ±5%
Case Temperature (T_C)	
Commercial	0°C to +75°C

DC Characteristics over operating temperature ranges (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −5.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 16 mA			0.45	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5, & 6)	2.1			V
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5, & 6)			0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V		−180	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 4.5V		1.0	40	μA
I_{IHB}	Input Breakdown Current	V_{CC} = Max, V_{IN} = V_{CC}			1.0	mA
V_{IC}	Input Diode Clamp Voltage	V_{CC} = Max, I_{IN} = −10 mA		−1.0	−1.5	V
I_{OZH}	Output Current (HIGH Z)	V_{CC} = Max, V_{OUT} = 2.4V			50	μA
I_{OZL}		V_{CC} = Max, V_{OUT} = 0.5V			−50	μA
I_{OS}	Output Current Short Circuit to Ground (Note 7)	V_{CC} = Max (Note 7)			−100	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs = GND, Output Open			65	mA

AC Electrical Characteristics (Note 6) V_{CC} = 5.0 ±5%, GND = 0V, T_C = 0°C to + 75°C

Symbol	Parameter	Conditions	Min	Max	Units
READ TIMING					
t_{ACS}	Chip Select Access Time	*Figures 3a, 3b*		15	ns
t_{ZRCS}	Chip Select to HIGH Z			15	ns
t_{AA}	Address Access Time (Note 8)			25	ns
WRITE TIMING					
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*Figure 4*	20		ns
t_{WSD}	Data Setup Time Prior to Write		5		ns
t_{WHD}	Data Hold Time after Write		5		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		5		ns
t_{WHA}	Address Hold Time after Write		5		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		ns
t_{ZWS}	Write Enable to Output Disable			15	ns
t_{WR}	Write Recovery Time			15	ns

Note 1: Either input voltage limit or input current limit is sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V, T_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels V_{IH} = 0.45V (V_{OL} Max) and V_{IH} = 2.4V (V_{OH} Min).

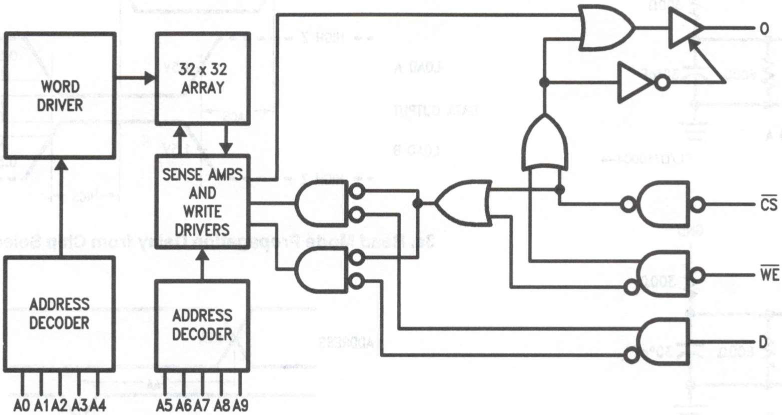
Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

Logic Diagram



TL/D/10004–2

Functional Description

The 93L425A is a fully decoded 1024-bit read write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address A0–A9.

One Chip Select ($\overline{CS}$) input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories the fast chip select access time permits direct address decoding without an increase in overall memory access time.

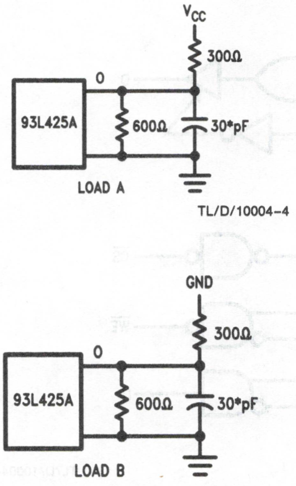
The read and write functions of the 93L425A are controlled by the state of the active LOW Write Enable $\overline{WE}$ input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at A0 through A9. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output O.

The 93L425A has a three-state output which provides an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-up provides drive capability for high capacitive loads while the high impedance state allows optimization of word expansion in bus organized systems.

Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	H	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write 0
L	L	H	HIGH Z	Write 1
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level: 2.4V
L = LOW Voltage Level: 0.45V
X = Don't Care HIGH or LOW
HIGH Z = High-Impedance


V_CC
300Ω
0
93L425A
600Ω
30*pF
LOAD A
TL/D/10004-4
GND
300Ω
0
93L425A
600Ω
30*pF
LOAD B
TL/D/10004-5

Note: Load A is used for all production testing.

*Includes jig and probe capacitance.

FIGURE 1. AC Test Output Load

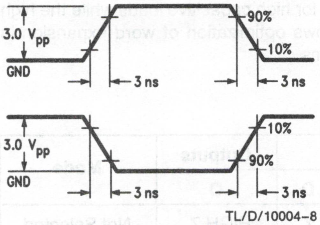
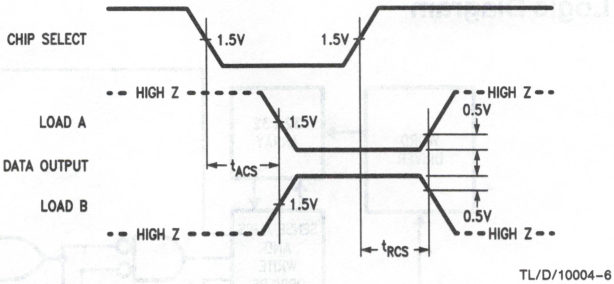
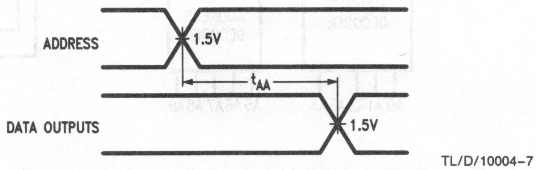

3.0 V_PP
GND
90%
10%
3 ns
3 ns
3.0 V_PP
GND
10%
90%
3 ns
3 ns
TL/D/10004-8

FIGURE 2. AC Test Input Levels

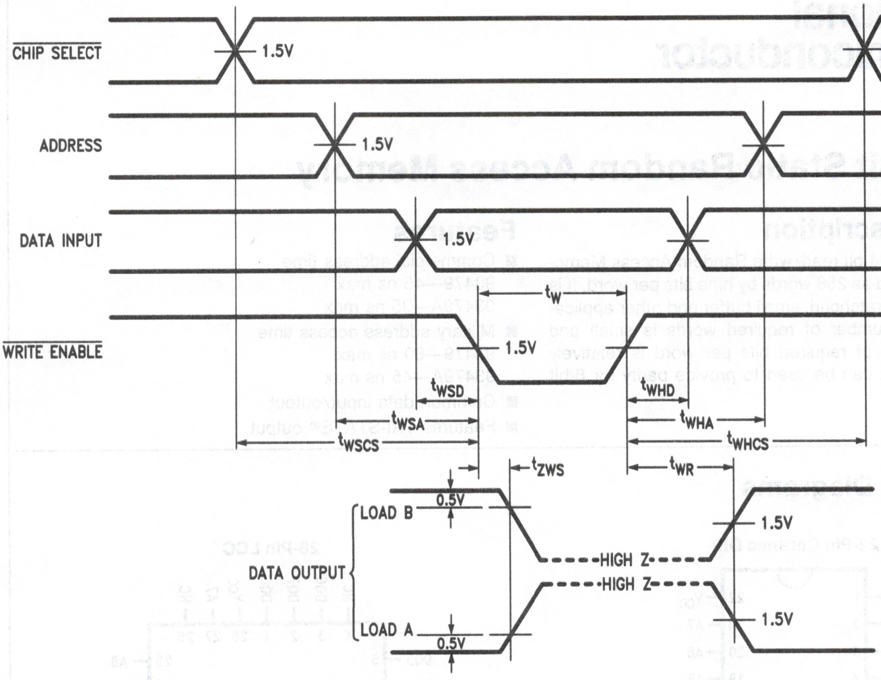

CHIP SELECT
1.5V
1.5V
HIGH Z
HIGH Z
LOAD A
1.5V
0.5V
DATA OUTPUT
t_ACS
LOAD B
1.5V
0.5V
HIGH Z
HIGH Z
t_RCS
TL/D/10004-6

3a. Read Mode Propagation Delay from Chip Select


ADDRESS
1.5V
t_AA
DATA OUTPUTS
1.5V
TL/D/10004-7

3b. Read Mode Propagation Delay from Address

FIGURE 3. Read Mode Timing


CHIP SELECT
1.5V
ADDRESS
1.5V
DATA INPUT
1.5V
WRITE ENABLE
1.5V
t_W
t_{WSD}
t_{WHD}
t_{WSA}
t_{WHA}
t_{WSCS}
t_{WHCS}
t_{ZWS}
t_{WR}
LOAD B
0.5V
DATA OUTPUT
HIGH Z
HIGH Z
1.5V
1.5V
LOAD A
0.5V

TL/D/10004–9

Note 1: Timing Diagram represents one solution which results in an optimum cycle time Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0V–0V.

FIGURE 4. Write Mode Timing

National Semiconductor

93479
256 x 9-Bit Static Random Access Memory

General Description

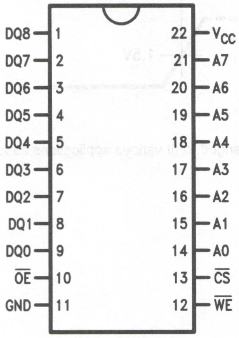
The 93479 is a 2304-bit read/write Random Access Memory (RAM), organized as 256 words by nine bits per word. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and where the number of required bits per word is relatively large. The ninth bit can be used to provide parity for 8-bit word systems.

Features

- Commercial address time
  93479—45 ns max
  93479A—35 ns max
- Military address access time
  93479—60 ns max
  93479A—45 ns max
- Common data input/output
- Features TRI-STATE® output

Connection Diagrams

22-Pin Ceramic DIP


DQ8 1
DQ7 2
DQ6 3
DQ5 4
DQ4 5
DQ3 6
DQ2 7
DQ1 8
DQ0 9
$\overline{OE}$ 10
GND 11
22 V_{CC}
21 A7
20 A6
19 A5
18 A4
17 A3
16 A2
15 A1
14 A0
13 $\overline{CS}$
12 $\overline{WE}$

TL/D/9675-1

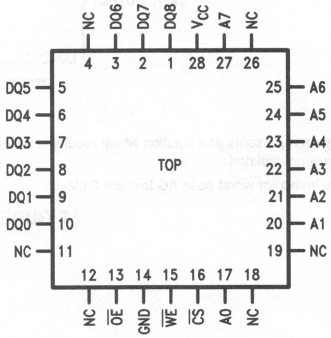
Top View

Order Number 93479DC, 93479ADC, 93479DMQB or 93479ADMQB
See NS Package Number J22A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn In

28-Pin LCC


NC 4
DQ6 3
DQ7 2
DQ8 1
V_{CC} 28
A7 27
NC 26
DQ5 5
DQ4 6
DQ3 7
DQ2 8
DQ1 9
DQ0 10
NC 11
TOP
25 A6
24 A5
23 A4
22 A3
21 A2
20 A1
19 NC
12 NC
13 $\overline{OE}$
14 GND
15 $\overline{WE}$
16 $\overline{CS}$
17 A0
18 NC

TL/D/9675-3

Top View

Order Number 93479LMQB or 93479ALMQB
See NS Package Number E28A*

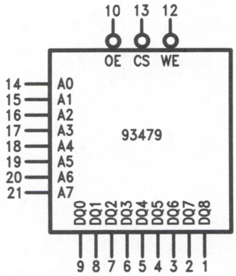
*For most current package information, contact product marketing.

Optional Processing QR = Burn In

Pin Names

A0–A7	Address Inputs
DQ0–DQ8	Data Input Outputs
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
NC	No Connect

Logic Symbol


10
13
12
OE
CS
WE
14 A0
15 A1
16 A2
17 A3
18 A4
19 A5
20 A6
21 A7
93479
DQ0 9
DQ1 8
DQ2 7
DQ3 6
DQ4 5
DQ5 4
DQ6 3
DQ7 2
DQ8 1

V_{CC} = Pin 22
GND = Pin 11

TL/D/9675-2

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Notes 1, 2)	−0.5V to V_{CC} (RAMs) −1.5V to V_{CC} (PROMs)
Voltage Applied to Outputs (Notes 2, 3) (Output HIGH)	−0.5V to +5.5V (RAMs) −1.5V to +5.5V (PROMs)
Lead Temperature (Soldering, 10 seconds)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA
Input Current (DC)	−12 mA to +5.0 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	
Commercial	5.0V ±5%
Military	5.0V ±10%
Case Temperature (T_C)	
Commercial	0°C to +75°C
Military	−55°C to +125°C

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V. T_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels $V_{IL} = V_{OL\ (Max)}$ (0.45V), $V_{IH} = V_{OH\ (Min)}$ (2.4V).

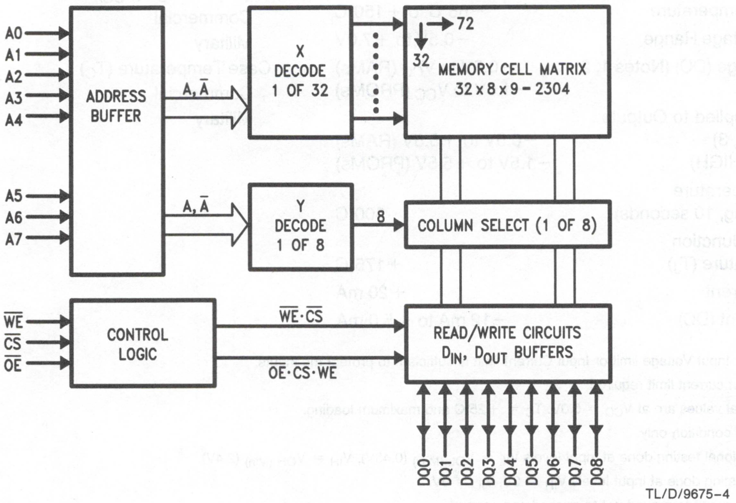
Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

Logic Diagram


A0
A1
A2
A3
A4
A5
A6
A7
ADDRESS BUFFER
A, Ā
X DECODE 1 OF 32
72
32
MEMORY CELL MATRIX 32 x 8 x 9 - 2304
A, Ā
Y DECODE 1 OF 8
8
COLUMN SELECT (1 OF 8)
WE
CS
OE
CONTROL LOGIC
WE·CS
OE·CS·WE
READ/WRITE CIRCUITS D_IN, D_OUT BUFFERS
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8

TL/D/9675-4

Functional Description

The 93479 is a fully decoded 2304-bit random access memory organized 256 words by nine bits. Word selection is achieved by means of an 8-bit address A0–A7.

The Chip Select input provides for memory array expansion. For larger memories the fast chip select access time permits decoding without an increase in overall memory access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW, the chip selected and the output disabled, the data at DQ0–DQ8 is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH, the chip selected and the output enabled. Non-inverted data is then presented at the outputs DQ0–DQ8.

The 93479 has TRI-STATE outputs which provide an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-ups provide drive capability for high capacitive loads while the high impedance state allows optimization of word expansion in bus organized systems.

Truth Table

Inputs			Data In/Out DQ0–DQ8	Mode
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$		
X	H	X	HIGH Z	Output Disabled
H	X	X	HIGH Z	R W Disabled
L	L	H	Data Out	Read
L	H	L	Data In	Write

H = HIGH Voltage Level 2.4V
L = LOW Voltage Level 0.5V
X = Don't Care HIGH or LOW
HIGH Z = High Impedance State

DC Electrical Characteristics Over operating temperature ranges (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA				0.5	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −5.2 mA		2.4			V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5 & 6)		2.1			V
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5 & 6)				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V			−250	−400	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 4.5V			1.0	40	μA
I_{IHB}	Input Breakdown Current	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{OZH} I_{OZL}	Output Current (HIGH Z)	V_{CC} = Max, V_{OUT} = 2.4V V_{CC} = Max, V_{OUT} = 0.5V			 −50	50 −400	μA μA
V_C	Input Diode Clamp Voltage	V_{CC} = Max, V_{IN} = −10 mA			−1.0	−1.5	V
I_{OS}	Output Current Short Circuit to Ground	V_{CC} = Max, (Note 7)				−70	mA
I_{CC}	Power Supply Current	Commercial Military	V_{CC} = Max All Inputs GND			185 200	mA

Commercial

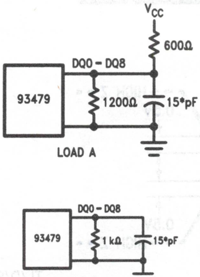
AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C

Symbol	Parameter	Conditions	A		Std		Units
			Min	Max	Min	Max	
READ TIMING							
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b, 3d)*		25		25	ns
t_{ZRCS}	Chip Select to HIGH Z			25		25	ns
t_{AOS}	Output Enable Access Time			25		25	ns
t_{ZROS}	Output Enable to HIGH Z			25		25	ns
t_{AA}	Address Access Time (Note 8)			35		45	ns
WRITE TIMING							
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figure 4)*	25		25		ns
t_{SO}	Output Enable Setup Time		5		5		ns
t_{HO}	Data Enable Hold Time		5		5		ns
t_{WSD}	Data Setup Time Prior to Write		25		25		ns
t_{WHD}	Data Hold Time after Write		5		5		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		5		5		ns
t_{WHA}	Address Hold Time after Write		5		5		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		5		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		ns

Military

AC Electrical Characteristics (Note 6)V_{CC} = 5.0V ±10%. GND = 0V. T_C = −55°C to +125°C

Symbol	Parameter	Conditions	A		Std		Units
			Min	Max	Min	Max	
READ TIMING							
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b, 3d)*		30		40	ns
t_{ZRCS}	Chip Select to HIGH Z			30		40	ns
t_{AOS}	Output Enable Access Time			30		40	ns
t_{ZROS}	Output Enable to HIGH Z			30		40	ns
t_{AA}	Address Access Time (Note 8)			45		60	ns
WRITE TIMING							
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figure 4)*	40		40		ns
t_{SO}	Output Enable Setup Time		5		5		ns
t_{HO}	Data Enable Hold Time		5		5		ns
t_{WSD}	Data Setup Time Prior to Write		50		50		ns
t_{WHD}	Data Hold Time after Write		10		10		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		10		10		ns
t_{WHA}	Address Hold Time after Write		10		10		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		10		10		ns
t_{WHCS}	Chip Select Hold Time after Write		10		10		ns


VCC
600Ω
DQ0 – DQ8
93479
1200Ω
15*pF
LOAD A
DQ0 – DQ8
93479
1 kΩ
15*pF
LOAD B

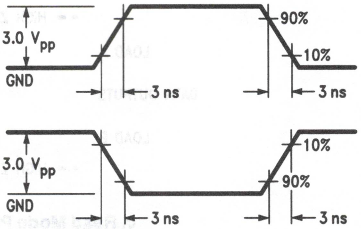
TL/D/9675-5

TL/D/9675-6

*Includes jig and probe capacitance

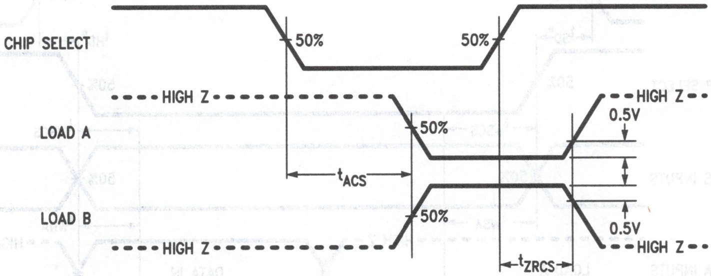
Note: Load A is used for all production testing.

FIGURE 1. AC Test Load Output Load


3.0 Vpp
GND
90%
10%
3 ns
3 ns
3.0 Vpp
GND
10%
90%
3 ns
3 ns

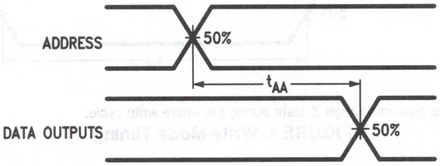
TL/D/9675-7

FIGURE 2. AC Test Input Levels


CHIP SELECT
50%
50%
HIGH Z
LOAD A
50%
tACS
HIGH Z
0.5V
LOAD B
50%
HIGH Z
0.5V
HIGH Z
tZRCS

TL/D/9675-8

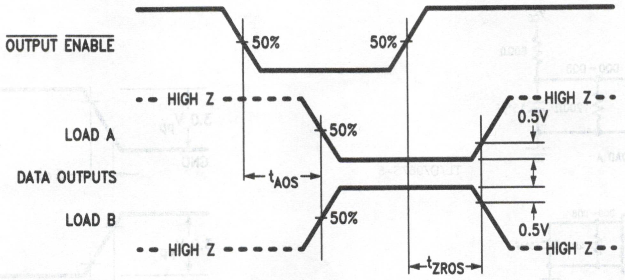
a. Read Mode Propagation Delay from Chip Select to Output


ADDRESS
50%
tAA
DATA OUTPUTS
50%

TL/D/9675-9

b. Read Mode Propagation Delay from Address to Output

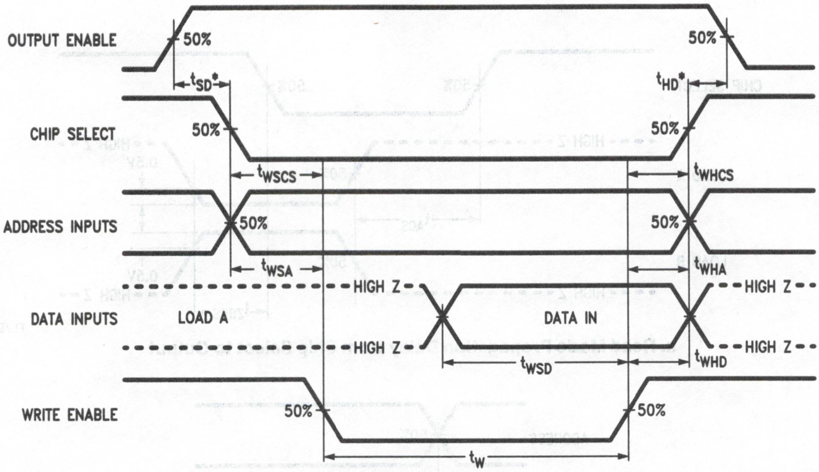
FIGURE 3. Read Mode Timing


OUTPUT ENABLE
50%
50%
HIGH Z
LOAD A
DATA OUTPUTS
LOAD B
HIGH Z
50%
50%
HIGH Z
0.5V
0.5V
HIGH Z
t_{AOS}
t_{ZROS}

TL/D/9675-10

c. Read Mode Propagation Delay from Output Enable

FIGURE 3. Read Mode Timing (Continued)


OUTPUT ENABLE
50%
50%
t_{SD}*
t_{HD}*
CHIP SELECT
50%
50%
t_{WSCS}
t_{WHCS}
ADDRESS INPUTS
50%
50%
t_{WSA}
t_{WHA}
DATA INPUTS
LOAD A
HIGH Z
HIGH Z
DATA IN
HIGH Z
HIGH Z
t_{WSD}
t_{WHD}
WRITE ENABLE
50%
50%
t_W

TL/D/9675-11

*These timing parameters are only necessary to guarantee High Z state during the entire write cycle.

FIGURE 4. Write Mode Timing

Note 1: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0/0.0V.

National Semiconductor

MM54C89/MM74C89 64-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a $\overline{\text{write enable}}$ line and a $\overline{\text{memory enable}}$ line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE data output lines working in conjunction with the memory enable input provide for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{\text{memory enable}}$. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of $\overline{\text{memory enable}}$).

Note: The timing is different than the DM7489 in that a positive to negative transition of the $\overline{\text{memory enable}}$ must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing $\overline{\text{write enable}}$ and $\overline{\text{memory enable}}$ low.

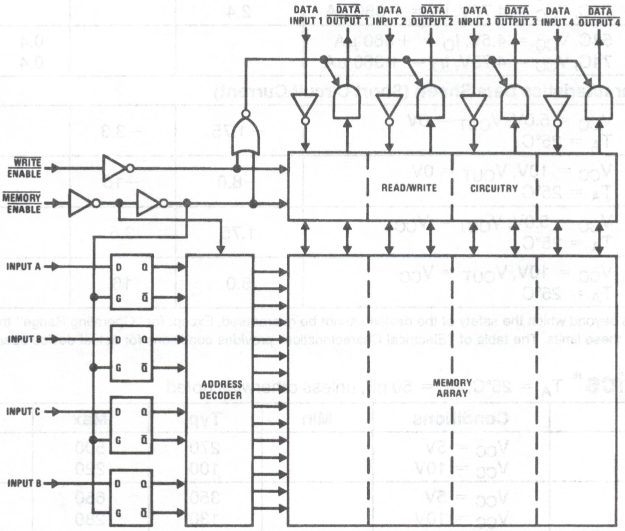
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing $\overline{\text{memory enable}}$ low and $\overline{\text{write enable}}$ high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

Features

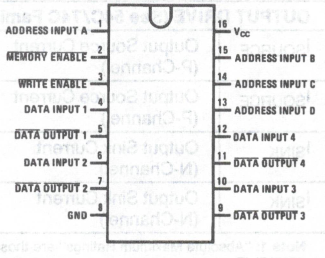
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low power consumption	100 nW/package (typ.)
■ Fast access time	130 ns (typ.) at V_{CC} = 10V
■ TRI-STATE output	

Logic and Connection Diagrams


DATA INPUT 1
DATA OUTPUT 1
DATA INPUT 2
DATA OUTPUT 2
DATA INPUT 3
DATA OUTPUT 3
DATA INPUT 4
DATA OUTPUT 4
WRITE ENABLE
MEMORY ENABLE
READ/WRITE
CIRCUITRY
INPUT A
INPUT B
INPUT C
INPUT D
D Q
G Q̄
ADDRESS DECODER
MEMORY ARRAY

TL/F/5888-1

Dual-In-Line Package


ADDRESS INPUT A 1
MEMORY ENABLE 2
WRITE ENABLE 3
DATA INPUT 1 4
DATA OUTPUT 1 5
DATA INPUT 2 6
DATA OUTPUT 2 7
GND 8
16 VCC
15 ADDRESS INPUT B
14 ADDRESS INPUT C
13 ADDRESS INPUT D
12 DATA INPUT 4
11 DATA OUTPUT 4
10 DATA INPUT 3
9 DATA OUTPUT 3

Top View TL/F/5888-2

Order Number MM54C89 or MM74C89

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C89	−55°C to +125°C
MM74C89	−40°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10 µA V_{CC} = 10V, I_O = −10 µA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10 µA V_{CC} = 10V, I_O = +10 µA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		µA
I_{OZ}	Output Current in High Impedance State	V_{CC} = 15V, V = 15V V_{CC} = 15V, V_O = 0V	 −1.0	0.005 −0.005	1.0	µA µA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	µA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360 µA 74C, V_{CC} = 4.75V, I_O = −360 µA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = +360 µA 74C, V_{CC} = 4.75V, I_O = +360 µA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay from Memory Enable	V_{CC} = 5V V_{CC} = 10V		270 100	500 220	ns ns
t_{ACC}	Access Time from Address Input	V_{CC} = 5V V_{CC} = 10V		350 130	650 280	ns ns
t_{SA}	Address Setup Time	V_{CC} = 5V V_{CC} = 10V	150 60			ns ns
t_{HA}	Address Hold Time	V_{CC} = 5V V_{CC} = 10V	60 40			ns ns
t_{ME}	Memory Enable Pulse Width	V_{CC} = 5V V_{CC} = 10V	400 150	250 90		ns ns

AC Electrical Characteristics* $T_A = 25°C, C_L = 50$ pF, unless otherwise noted (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{SR}	Write Enable Setup Time for a Read	$V_{CC} = 5V$ $V_{CC} = 10V$	0 0			ns ns
t_{WS}	Write Enable Setup Time for a Write	$V_{CC} = 5V$ $V_{CC} = 10V$			t_{ME} t_{ME}	ns ns
t_{WE}	Write Enable Pulse Width	$V_{CC} = 5V, t_{WS} = 0$ $V_{CC} = 10V, t_{WS} = 0$	300 100	160 60		ns ns
t_{HD}	Data Input Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$	50 25			ns ns
t_{SD}	Data Input Setup	$V_{CC} = 5V$ $V_{CC} = 10V$	50 25			ns ns
t_{1H}, t_{0H}	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Memory Enable	$V_{CC} = 5V, C_L = 5$ pF, $R_L = 10k$ $V_{CC} = 10V, C_L = 5$ pF, $R_L = 10k$		180 −85	300 120	ns ns
t_{1H}, t_{0H}	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Write Enable	$V_{CC} = 50V, C_L = 5$ pF, $R_L = 10k$ $V_{CC} = 10V, C_L = 5$ pF, $R_L = 10k$		180 85	300 120	ns ns
C_{IN}	Input Capacity	Any Input (Note 2)		5		pF
C_{OUT}	Output Capacity	Any Output (Note 2)		6.5		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		230		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

AC Electrical Characteristics* Guaranteed across the specified temperature range, $C_L = 50$ pF

Parameter	Conditions	MM54C89 $T_A = -55°C$ to $+125°C$		MM74C89 $T_A = -40°C$ to $+85°C$		Units
		Min	Max	Min	Max	
t_{PD}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$		700 310 250		600 265 210	ns ns ns
t_{ACC}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$		910 400 320		780 345 270	ns ns ns
t_{SA}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	210 90 70		180 80 60		ns ns ns
t_{HA}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	80 55 45		70 50 40		ns ns ns
t_{ME}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	560 210 170		480 180 150		ns ns ns
t_{WE}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	420 140 110		360 120 100		ns ns ns
t_{HD}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	70 35 30		60 30 25		ns ns ns

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics*

Guaranteed across the specified temperature range, C_L = 50 pF (Continued)

Parameter	Conditions	MM54C89 T_A = −55°C to +125°C		MM74C89 T_A = −40°C to +85°C		Units
		Min	Max	Min	Max	
t_{SD}	V_{CC} = 5V	70		60		ns
	V_{CC} = 10V	35		30		ns
	V_{CC} = 15V	30		25		ns
t_{1H}, t_{0H}	V_{CC} = 5V		420		360	ns
	V_{CC} = 10V, C_L = 5 pF		170		145	ns
	V_{CC} = 15V, R_L = 10 kΩ		135		115	ns

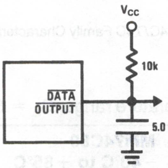
*AC Parameters are guaranteed by DC correlated testing.

Truth Table

ME	WE	Operation	Condition of Outputs
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

AC Test Circuits

t_{0H}


V_CC
10k
DATA OUTPUT
5.0 pF

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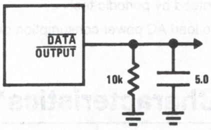
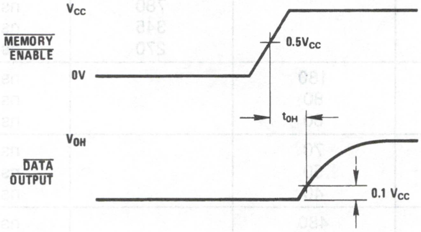
t_{1H}


DATA OUTPUT
10k
5.0 pF

TL/F/5888-3

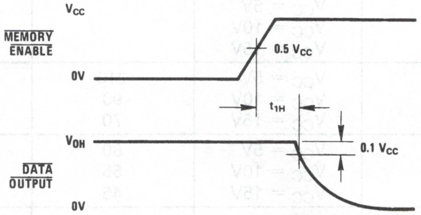
Switching Time Waveforms

t_{0H}


V_CC
MEMORY ENABLE
0V
0.5V_CC
t_0H
V_OH
DATA OUTPUT
0.1 V_CC

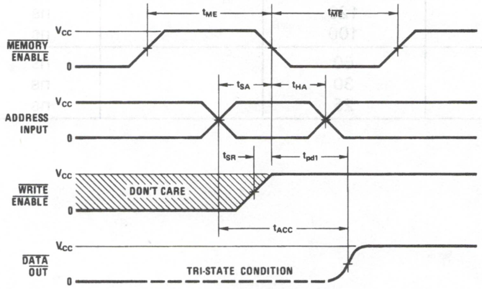
TL/F/5888-5

t_{1H}


V_CC
MEMORY ENABLE
0V
0.5 V_CC
t_1H
V_OH
DATA OUTPUT
0V
0.1 V_CC

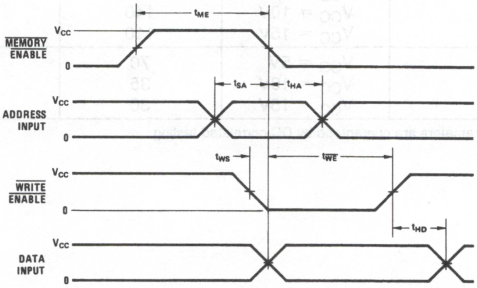
TL/F/5888-6

Read Cycle


t_ME
t_ME
V_CC
MEMORY ENABLE
0
t_SA
t_HA
V_CC
ADDRESS INPUT
0
t_SR
t_pd1
V_CC
WRITE ENABLE
0
DON'T CARE
t_ACC
V_CC
DATA OUT
0
TRI-STATE CONDITION

TL/F/5888-7

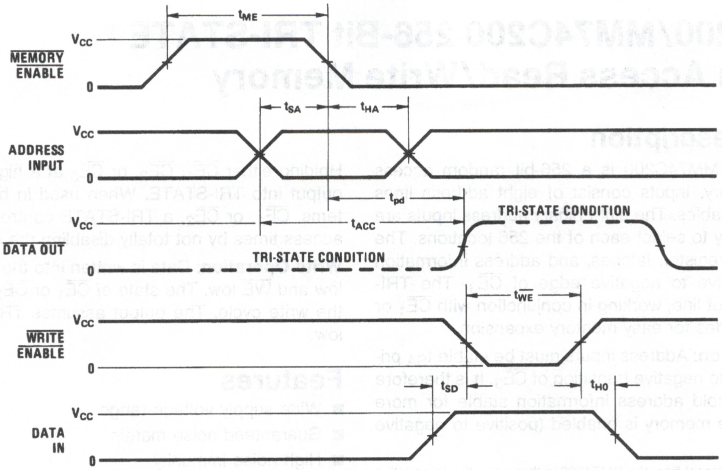
Write Cycle


t_ME
V_CC
MEMORY ENABLE
0
t_SA
t_HA
V_CC
ADDRESS INPUT
0
t_WS
t_WE
V_CC
WRITE ENABLE
0
t_HD
V_CC
DATA INPUT
0

TL/F/5888-8

Switching Time Waveforms (Continued)

Read Modify Write Cycle


t_{ME}
V_{CC}
MEMORY ENABLE
0
t_{SA}
t_{HA}
V_{CC}
ADDRESS INPUT
0
t_{pd}
TRI-STATE CONDITION
t_{ACC}
V_{CC}
DATA OUT
0
TRI-STATE CONDITION
t_{WE}
V_{CC}
WRITE ENABLE
0
t_{SD}
t_{H0}
V_{CC}
DATA IN
0

TL/F/5888-9

Note: $t_r = 60$ ns

$t_f = 10$ ns

National Semiconductor

MM54C200/MM74C200 256-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. The internal address register, latches, and address information are on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line, working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs, provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is therefore unnecessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different from the DM74200 in that a positive to negative transition of the $\overline{CE}_3$ must occur for the memory to be selected.

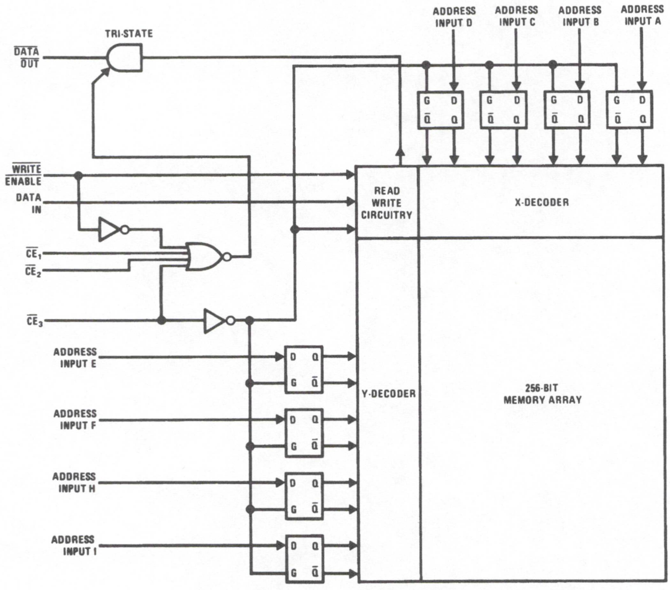
Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and $\overline{WE}$ high. Holding either $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus-organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control provides for fast access times by not totally disabling the chip.

Write Operation: Data is written into the memory with $\overline{CE}_3$ low and $\overline{WE}$ low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with $\overline{WE}$ low.

Features

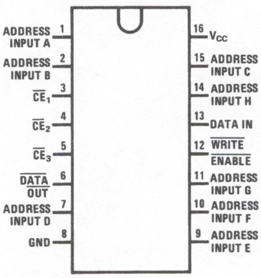
■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	Fan out of 1 driving standard TTL
■ Low power	500 nW (typ.)
■ Internal address register	

Logic and Connection Diagrams


ADDRESS INPUT D
ADDRESS INPUT C
ADDRESS INPUT B
ADDRESS INPUT A
TRI-STATE
DATA OUT
WRITE ENABLE
DATA IN
CE1
CE2
CE3
ADDRESS INPUT E
ADDRESS INPUT F
ADDRESS INPUT H
ADDRESS INPUT I
G D Q̄ Q
D Q G Q̄
READ WRITE CIRCUITRY
X-DECODER
Y-DECODER
256-BIT MEMORY ARRAY

TL/F/5903-1

Dual-In-Line Package


ADDRESS INPUT A 1
ADDRESS INPUT B 2
CE1 3
CE2 4
CE3 5
DATA OUT 6
ADDRESS INPUT D 7
GND 8
16 VCC
15 ADDRESS INPUT C
14 ADDRESS INPUT H
13 DATA IN
12 WRITE ENABLE
11 ADDRESS INPUT G
10 ADDRESS INPUT F
9 ADDRESS INPUT E

TL/F/5903-2

Top View

Order Number MM54C200 or MM74C200

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range (T_A)	
MM54C200	−55°C to +125°C
MM74C200	−40°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C

Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA V_{CC} = 10V, I_O = −10 μA	4.5 9			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = +10 μA V_{CC} = 10V, I_O = +10 μA			0.5 1	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.1	600	μA
CMOS/TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −1.6 mA 74C V_{CC} = 4.75V, I_O = −1.6 mA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 1.6 mA 74C V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V T_A = 25°C	−4 −1.8	−6		mA mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−16 −1.5	−25		mA mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC} T_A = 25°C	5	8		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	20	30		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

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AC Electrical Characteristics* $T_A = 25°C, C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{ACC}	Access Time from Address	$V_{CC} = 5V$		450	900	ns
		$V_{CC} = 10V$		200	400	ns
t_{pd}	Propagation Delay from $\overline{CE}_3$	$V_{CC} = 5V$		360	700	ns
		$V_{CC} = 10V$		120	300	ns
t_{pCE1}	Propagation Delay from $\overline{CE}_1$ or $\overline{CE}_2$	$V_{CC} = 5V$		250	700	ns
		$V_{CC} = 10V$		85	200	ns
t_{SA}	Address Setup Time	$V_{CC} = 5V$	200	80		ns
		$V_{CC} = 10V$	100	30		ns
t_{HA}	Address Hold Time	$V_{CC} = 5V$	50	15		ns
		$V_{CC} = 10V$	25	5.0		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	$V_{CC} = 5V$	300	160		ns
		$V_{CC} = 10V$	150	70		ns
t_{CE}	$\overline{CE}_3$ Pulse Widths	$V_{CC} = 5V$	400	200		ns
		$V_{CC} = 10V$	160	80		ns
C_{IN}	Input Capacity	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity in TRI-STATE	(Note 2)		9.0		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		400		pF

AC Electrical Characteristics* $C_L = 50$ pF

Symbol	Parameter	Conditions	MM54C200 $T_A = -55°C$ to $+125°C$		MM74C200 $T_A = -40°C$ to $+85°C$		Units
			Min	Max	Min	Max	
t_{ACC}	Access Time from Address	$V_{CC} = 5V$		1200		1100	ns
		$V_{CC} = 10V$		520		480	ns
t_{pd}	Propagation Delay from $\overline{CE}_3$	$V_{CC} = 5V$		950		850	ns
		$V_{CC} = 10V$		400		360	ns
$t_{pd\overline{CE1}}$	Propagation Delay from $\overline{CE}_1$ or $\overline{CE}_2$	$V_{CC} = 5V$		650		600	ns
		$V_{CC} = 10V$		300		275	ns
t_{SA}	Address Setup Time	$V_{CC} = 5V$	250		250		ns
		$V_{CC} = 10V$	120		120		ns
t_{HA}	Address Hold Time	$V_{CC} = 5V$	100		100		ns
		$V_{CC} = 10V$	50		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	$V_{CC} = 5V$	450		400		ns
		$V_{CC} = 10V$	225		200		ns
t_{CE}	Disable Pulse Width	$V_{CC} = 5V$	500		460		ns
		$V_{CC} = 10V$	250		230		ns
t_{HD}	Data Hold Time	$V_{CC} = 5V$	50		50		ns
		$V_{CC} = 10V$	25		25		ns

*AC Parameters are guaranteed by DC correlated testing.

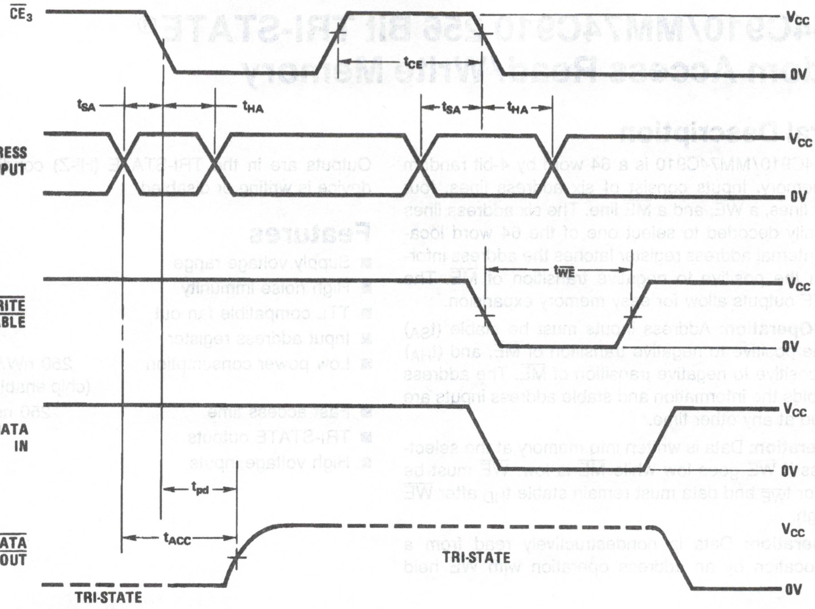
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

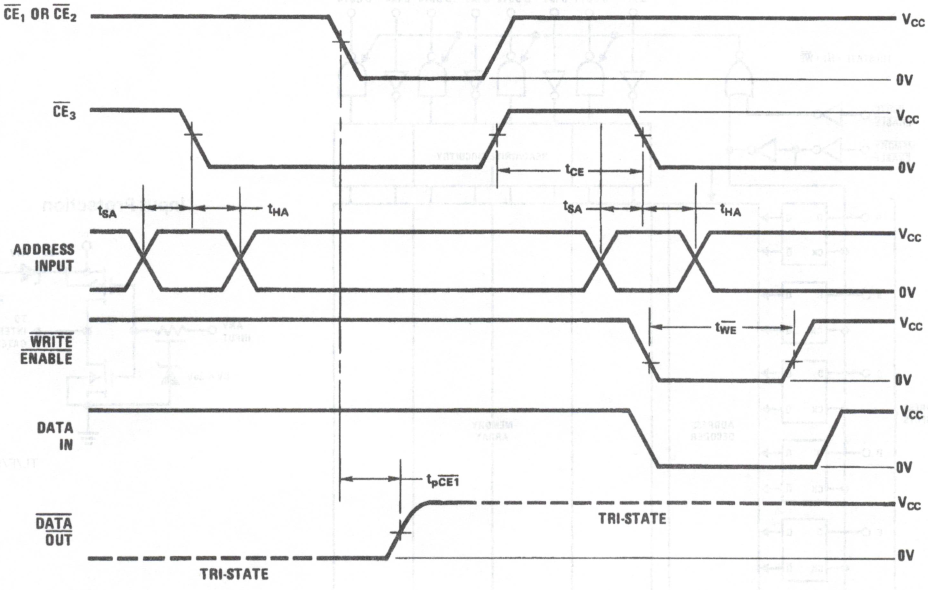
Switching Time Waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1$ = $\overline{CE}_2$ = logic 0)


$\overline{CE}_3$
V_{CC}
0V
t_{CE}
t_{SA}
t_{HA}
t_{SA}
t_{HA}
ADDRESS INPUT
V_{CC}
0V
$t_{\overline{WE}}$
$\overline{\text{WRITE ENABLE}}$
V_{CC}
0V
DATA IN
V_{CC}
0V
t_{pd}
t_{ACC}
$\overline{\text{DATA OUT}}$
V_{CC}
TRI-STATE
TRI-STATE
0V

TL/F/5903–3

Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)


$\overline{CE}_1$ OR $\overline{CE}_2$
V_{CC}
0V
$\overline{CE}_3$
V_{CC}
t_{CE}
0V
t_{SA}
t_{HA}
t_{SA}
t_{HA}
ADDRESS INPUT
V_{CC}
0V
$t_{\overline{WE}}$
$\overline{\text{WRITE ENABLE}}$
V_{CC}
0V
DATA IN
V_{CC}
0V
$t_{p\overline{CE1}}$
$\overline{\text{DATA OUT}}$
V_{CC}
TRI-STATE
0V
TRI-STATE

TL/F/5903–4

Note: Used for fast access time in bused systems.

National Semiconductor

MM54C910/MM74C910 256 Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C910/MM74C910 is a 64 word by 4-bit random access memory. Inputs consist of six address lines, four data input lines, a $\overline{WE}$, and a $\overline{ME}$ line. The six address lines are internally decoded to select one of the 64 word locations. An internal address register latches the address information on the positive to negative transition of $\overline{ME}$. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of $\overline{ME}$, and (t_{HA}) after the positive to negative transition of $\overline{ME}$. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if $\overline{WE}$ goes low while $\overline{ME}$ is low. $\overline{WE}$ must be held low for $t_{\overline{WE}}$ and data must remain stable t_{HD} after $\overline{WE}$ returns high.

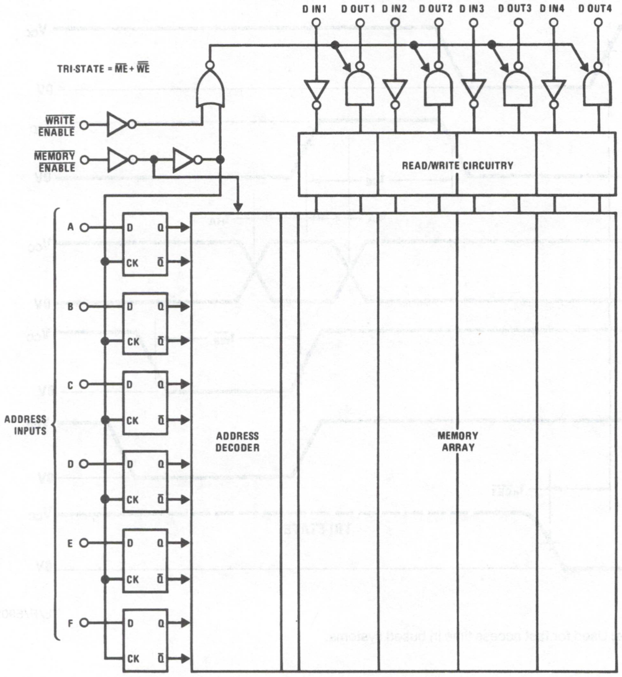
Read Operation: Data is nondestructively read from a memory location by an address operation with $\overline{WE}$ held high.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

Features

■ Supply voltage range	3.0V to 5.5V
■ High noise immunity	$0.45V_{CC}$ (typ.)
■ TTL compatible fan out	1 TTL load
■ Input address register	
■ Low power consumption	250 nW/package (typ.) (chip enabled or disabled)
■ Fast access time	250 ns (typ.) at 5.0V
■ TRI-STATE outputs	
■ High voltage inputs	

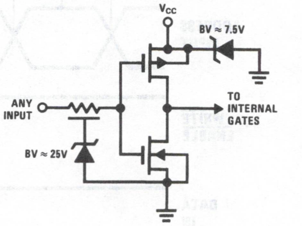
Logic Diagrams



D IN1
D OUT1
D IN2
D OUT2
D IN3
D OUT3
D IN4
D OUT4
TRI-STATE = $\overline{ME}$ + $\overline{WE}$
$\overline{WRITE}$ ENABLE
$\overline{MEMORY}$ ENABLE
READ/WRITE CIRCUITRY
A
B
C
D
E
F
D
Q
CK
$\overline{Q}$
ADDRESS INPUTS
ADDRESS DECODER
MEMORY ARRAY

TL/F/5914–1

Input Protection



V_{CC}
BV ≈ 7.5V
ANY INPUT
BV ≈ 25V
TO INTERNAL GATES

TL/F/5914–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Output Pin	-0.3V to $V_{CC}+0.3\text{V}$
Voltage at Any Input Pin	-0.3V to $+15\text{V}$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 5.5V
Standby V_{CC} Range	1.5V to 5.5V
Absolute Maximum (V_{CC})	6.0V
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
MM54C910	4.5	5.5	V
MM74C910	4.75	5.25	V
Temperature (T_A)			
MM54C910	-55	$+125$	°C
MM74C910	-40	$+85$	°C

DC Electrical Characteristics

Min/Max limits apply accross the temperature and power supply range indicated

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage	Full Range	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	Full Range			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN}=15\text{V}$ $V_{IN}=5\text{V}$		0.005 0.005	2.0 1.0	µA µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN}=0\text{V}$	-1.0	-0.005		µA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O=-150\ \mu\text{A}$ $I_O=-400\ \mu\text{A}$	$V_{CC}-0.5$ 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=1.6\text{ mA}$			0.4	V
I_{OZ}	Output Current in High Impedance State	$V_O=5\text{V}$ $V_O=0\text{V}$	 -1.0	0.005 -0.005	1.0	µA µA
I_{CC}	Supply Current	$V_{CC}=5\text{V}$		5.0	300	µA

AC Electrical Characteristics* $T_A=25°\text{C}, V_{CC}=5.0\text{V}, C_L=50\text{ pF}$

Symbol	Parameter	Min	Typ	Max	Units
t_{ACC}	Access Time from Address		250	500	ns
t_{pd}	Propagation Delay from $\overline{\text{ME}}$		180	360	ns
t_{SA}	Address Input Set-Up Time	140	70		ns
t_{HA}	Address Input Hold Time	20	10		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	200	100		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	200		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	15		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity Any Output (Note 2)		9.0		pF
C_{PD}	Power Dissipation Capacity (Note 3)		350		pF

5

AC Electrical Characteristics* (Continued) $T_A = 25°C, V_{CC} = 5.0V, C_L = 50\ pF$

Symbol	Parameter	MM54C910 $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$		MM74C910 $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.75V$ to $5.25V$		Units
		Min	Max	Min	Max	
t_{ACC}	Access Time from Address		860		700	ns
t_{pd1}, t_{pd0}	Propagation Delay from $\overline{ME}$		660		540	ns
t_{SA}	Address Input Set-Up Time	200		160		ns
t_{HA}	Address Input Hold Time	20		20		ns
$t_{\overline{ME}}$	$\overline{\text{Memory}}$ $\overline{\text{Enable}}$ Pulse Width	280		260		ns
$t_{\overline{ME}}$	$\overline{\text{Memory}}$ $\overline{\text{Enable}}$ Pulse Width	750		600		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	50		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width	200		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		200		200	ns

*AC Parameters are guaranteed by DC correlated testing.

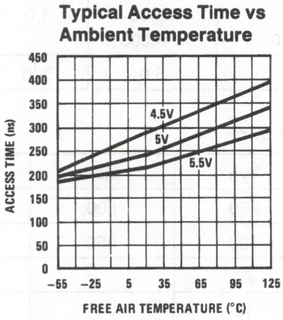
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Note 4: See AC test circuits for t_{1H}, t_{0H}.

Typical Performance Characteristics

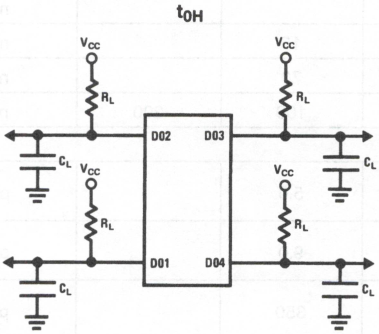


TL/F/5914-4

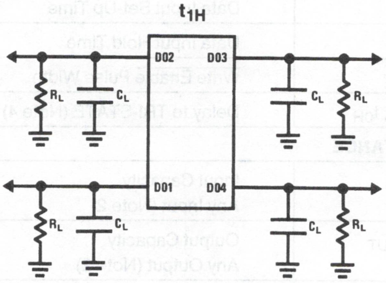
Truth Table

$\overline{ME}$	$\overline{WE}$	Operation	Outputs
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

AC Test Circuits



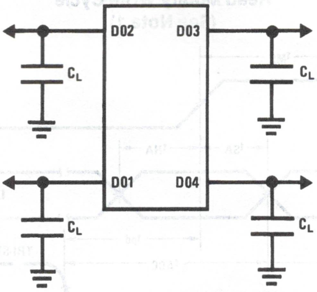
TL/F/5914-5



TL/F/5914-6

AC Test Circuits (Continued)

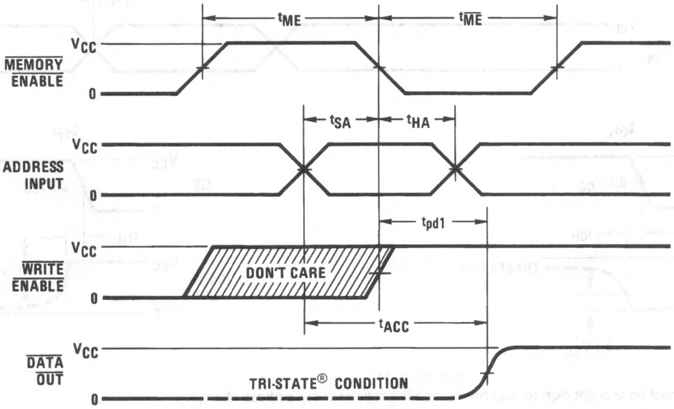
All Other AC Tests


D02
D03
D01
D04
C_L
C_L
C_L
C_L

TL/F/5914-7

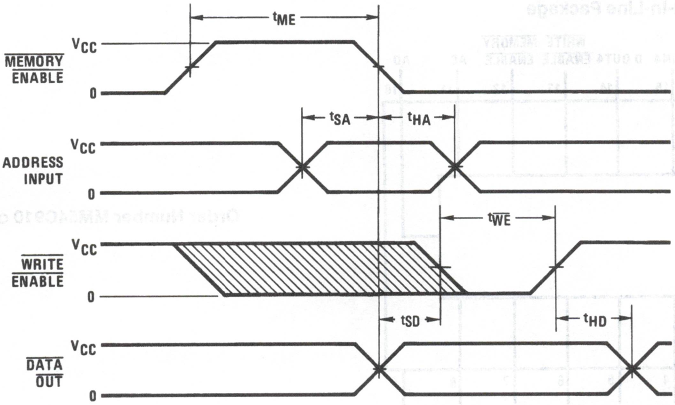
Switching Time Waveforms

Read Cycle
(See Note 1)


tME
tME
VCC
MEMORY ENABLE
0
tSA
tHA
VCC
ADDRESS INPUT
0
tpd1
VCC
WRITE ENABLE
0
DON'T CARE
tACC
VCC
DATA OUT
0
TRI-STATE® CONDITION

TL/F/5914-8

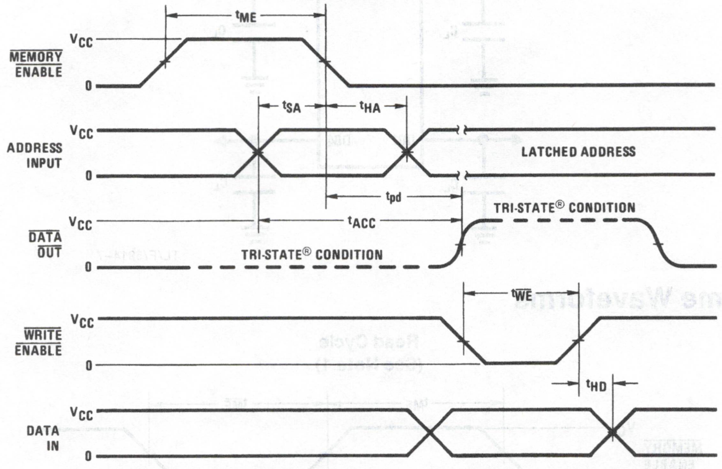
Write Cycle
(See Note 1)


tME
VCC
MEMORY ENABLE
0
tSA
tHA
VCC
ADDRESS INPUT
0
tWE
VCC
WRITE ENABLE
0
tSD
tHD
VCC
DATA OUT
0

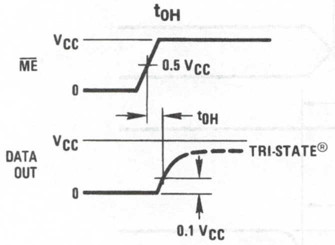
TL/F/5914-9

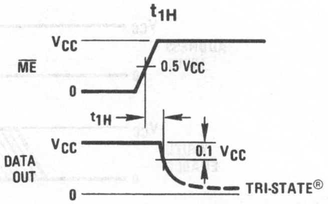
Switching Time Waveforms (Continued)

Read Modify Write Cycle
(See Note 1)


tME
VCC
MEMORY ENABLE
0
tSA
tHA
VCC
ADDRESS INPUT
0
LATCHED ADDRESS
tpd
TRI-STATE® CONDITION
VCC
tACC
DATA OUT
0
TRI-STATE® CONDITION
tWE
VCC
WRITE ENABLE
0
tHD
VCC
DATA IN
0

TL/F/5914-10


tOH
VCC
ME
0
0.5 VCC
tOH
VCC
DATA OUT
0
TRI-STATE®
0.1 VCC


t1H
VCC
ME
0
0.5 VCC
t1H
VCC
0.1 VCC
DATA OUT
0
TRI-STATE®

TL/F/5914-12

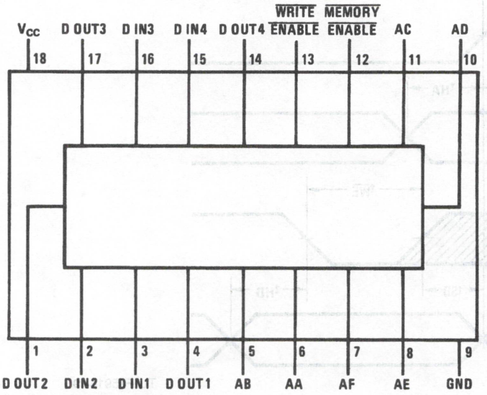
TL/F/5914-11

Note 1: $\overline{\text{MEMORY}}$ $\overline{\text{ENABLE}}$ must be brought high for t_{ME} nanoseconds between every address change.

Note 2: $t_r = t_f = 20$ ns for all inputs.

Connection Diagram

Dual-In-Line Package


VCC
D OUT3
D IN3
D IN4
D OUT4
WRITE ENABLE
MEMORY ENABLE
AC
AD
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9
D OUT2
D IN2
D IN1
D OUT1
AB
AA
AF
AE
GND

TL/F/5914-3

Top View

Order Number MM54C910 or MM74C910

National Semiconductor

MM54C989/MM74C989 64-Bit (16 x 4) TRI-STATE® RAM

General Description

The MM54C989/MM74C989 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of 4 address lines, 4 data input lines. a write enable line and a memory enable line. The 4 binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The 4 TRI-STATE data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

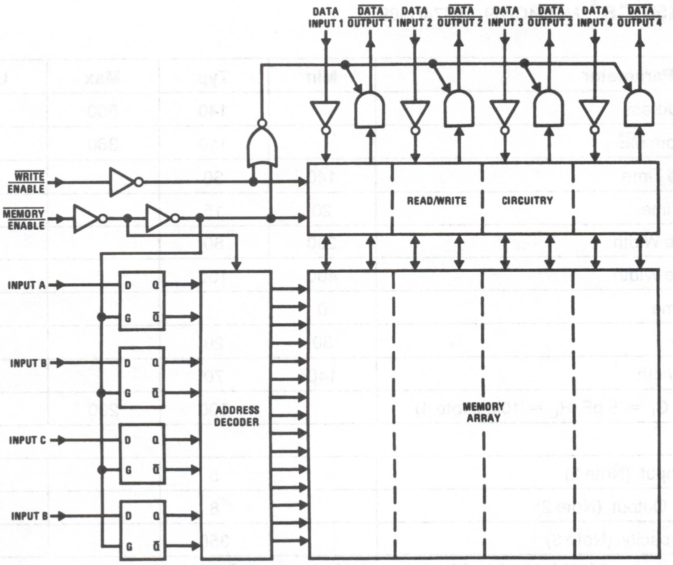
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the 4 outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-Z) condition.

Features

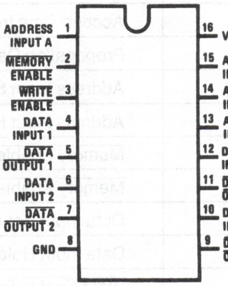
■ Wide supply voltage range	3.0V to 5.5V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L
■ Input address register	
■ Low power consumption	250 nW/package (typ.) @ V_{CC} = 5V
■ Fast access time	140 ns (typ.) at V_{CC} = 5V
■ TRI-STATE output	

Logic and Connection Diagrams


DATA INPUT 1
DATA OUTPUT 1
DATA INPUT 2
DATA OUTPUT 2
DATA INPUT 3
DATA OUTPUT 3
DATA INPUT 4
DATA OUTPUT 4
WRITE ENABLE
MEMORY ENABLE
READ/WRITE
CIRCUITRY
INPUT A
INPUT B
INPUT C
INPUT D
D
Q
G
Q̄
ADDRESS DECODER
MEMORY ARRAY

TL/F/5925–1

Dual-In-Line Package


ADDRESS INPUT A 1
MEMORY ENABLE 2
WRITE ENABLE 3
DATA INPUT 1 4
DATA OUTPUT 1 5
DATA INPUT 2 6
DATA OUTPUT 2 7
GND 8
16 VCC
15 ADDRESS INPUT B
14 ADDRESS INPUT C
13 ADDRESS INPUT D
12 DATA INPUT 4
11 DATA OUTPUT 4
10 DATA INPUT 3
9 DATA OUTPUT 3

TL/F/5925–2

Top View

Order Number MM54C989 or MM74C989

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Absolute Maximum V_{CC}	7.0V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
MM54C989	4.7	5.5	V
MM74C989	4.75	5.25	V
Temperature (T_A)			
MM54C989	−55	+125	°C
MM74C989	−40	+85	°C
Operating V_{CC} Range			3.0V to 5.5V
Standby V_{CC} Range			1.5V to 5.5V

DC Electrical Characteristics MM54C989/MM74C989

Min/Max limits apply across the temperature and power supply range indicated

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5V$		0.005	1	µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−1	−0.005		µA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$	2.4			V
		$I_O = -150\ \mu A$	$V_{CC} - 0.5$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 360\ \mu A$			0.4	V
I_{OZ}	Output Current in High Impedance State	$V_O = 5V$		0.005	1	µA
		$V_O = 0V$	−1	−0.005		µA
I_{CC}	Supply Current Active (Note 1)*	$\overline{ME} = 0V$, $V_{CC} = 5V$		0.05	150	µA
I_{CC}	Supply Current (Stand-By)	$\overline{ME} = 5V$			3	µA

Note 1*: $\overline{\text{MEMORY ENABLE}}$ must be brought high for t_{ME} ns between every address change.

AC Electrical Characteristics* MM54C989/MM74C989

$T_A = 25°C$, $V_{CC} = 5V$, $C_L = 50\ pF$

Symbol	Parameter	Min	Typ	Max	Units
t_{ACC}	Access Time from Address		140	500	ns
t_{PD}	Propagation Delay from $\overline{ME}$		110	360	ns
t_{SA}	Address Input Set-Up Time	140	30		ns
t_{HA}	Address Input Hold Time	20	15		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	200	80		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	100		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	20		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE, $C_L = 5\ pF$, $R_L = 10k$, (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity, Any Input, (Note 2)		5		pF
C_{OUT}	Output Capacity, Any Output, (Note 2)		8		pF
C_{PD}	Power Dissipation Capacity, (Note 3)		350		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

AC Electrical Characteristics* (Continued)

MM54C989: T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF
MM74C989: T_A = −40°C to +85°C, V_{CC} = 4.75V to 5.5V, C_L = 50 pF

Symbol	Parameter	MM54C989		MM74C989		Units
		Min	Max	Min	Max	
t_{ACC}	Access Time from Address		500		620	ns
t_{PD1}, t_{PD0}	Propagation Delay from $\overline{\text{ME}}$		350		430	ns
t_{SA}	Address Input Set-Up Time	150		140		ns
t_{HA}	Address Input Hold Time	50		60		ns
t_{ME}	$\overline{\text{Memory}}$ $\overline{\text{Enable}}$ Pulse Width	250		310		ns
$t_{\overline{ME}}$	$\overline{\text{Memory}}$ $\overline{\text{Enable}}$ Pulse Width	520		400		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	60		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width	220		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE, (Note 4)		200		200	ns

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

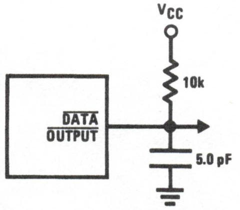
Note 4: See AC test circuit for t_{1H}, t_{0H}.

Truth Table

$\overline{\text{ME}}$	$\overline{\text{WE}}$	Operation	Condition of Outputs
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

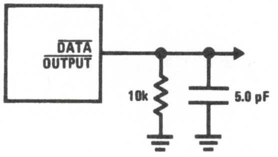
AC Test Circuits

t_{0H}



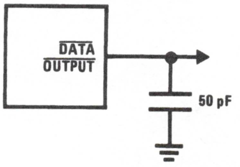
TL/F/5925-3

t_{1H}



TL/F/5925-4

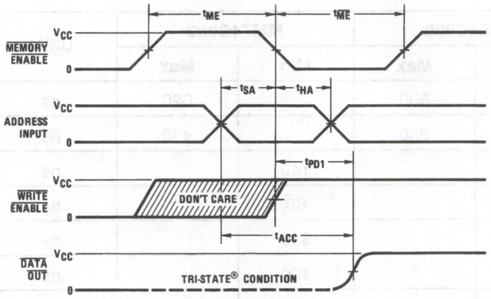
All Other AC Tests



TL/F/5925-5

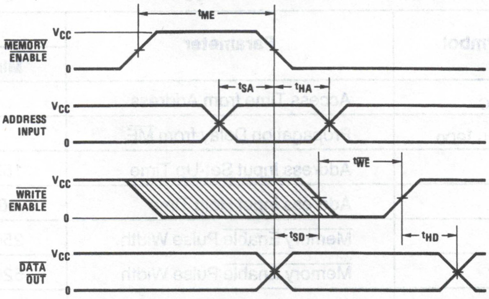
Switching Time Waveforms

Read Cycle (Note 1)*


tME
tME
VCC
MEMORY ENABLE
0
tSA
tHA
VCC
ADDRESS INPUT
0
tPD1
VCC
WRITE ENABLE
0
DON'T CARE
tACC
VCC
DATA OUT
0
TRI-STATE® CONDITION

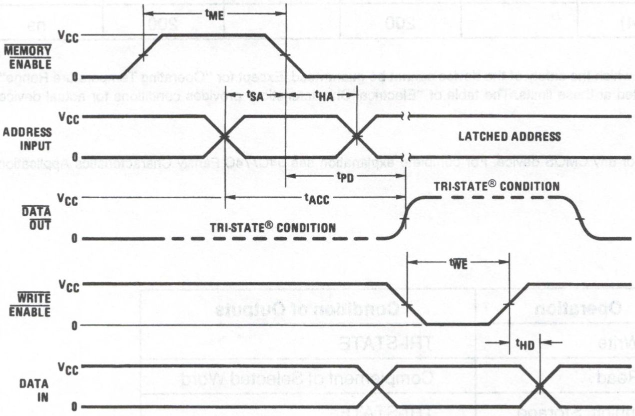
TL/F/5925-6

Write Cycle (Note 1)*


tME
VCC
MEMORY ENABLE
0
tSA
tHA
VCC
ADDRESS INPUT
0
tWE
VCC
WRITE ENABLE
0
tSD
tHD
VCC
DATA OUT
0

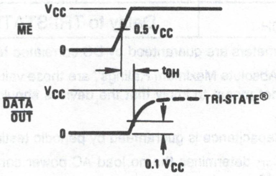
TL/F/5925-7

Read-Modify-Write Cycle (Note 1)*


tME
VCC
MEMORY ENABLE
0
tSA
tHA
VCC
ADDRESS INPUT
0
LATCHED ADDRESS
tPD
tACC
TRI-STATE® CONDITION
VCC
DATA OUT
0
TRI-STATE® CONDITION
tWE
VCC
WRITE ENABLE
0
tHD
VCC
DATA IN
0

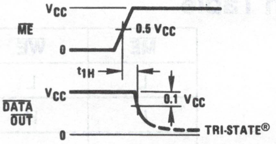
TL/F/5925-8

t_{0H}


VCC
ME
0
0.5 VCC
tOH
VCC
DATA OUT
0
TRI-STATE®
0.1 VCC

TL/F/5925-9

t_{1H}


VCC
ME
0
0.5 VCC
t1H
VCC
DATA OUT
0
0.1 VCC
TRI-STATE®

TL/F/5925-10

Note 1*: $\overline{\text{MEMORY}}$ $\overline{\text{ENABLE}}$ must be brought high for t_{ME} ns between every address change.

Note 2: $t_r = t_f = 20$ ns for all inputs.

National Semiconductor

NMC2147H 4096 x 1-Bit Static RAM

General Description

The NMC2147H is a 4096-word by 1-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

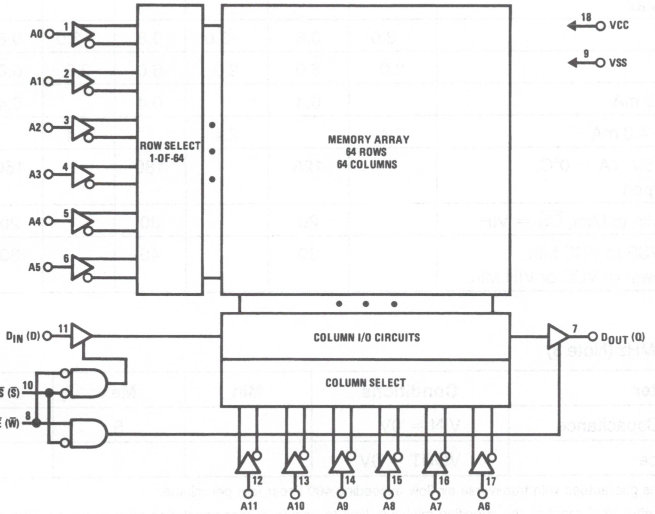
The separate chip select input automatically switches the part to its low power standby mode when it goes high.

The output is held in a high impedance state during write to simplify common I/O applications.

Features

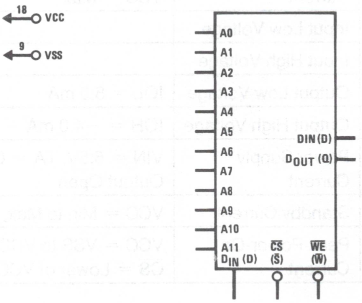
- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power-down
- High-speed—down to 35 ns access time
- TRI-STATE® output for bus interface
- Separate Data In and Data Out pins
- Single +5V supply
- Standard 18-pin dual-in-line package
- Available in MIL-STD-883 class B screening

Block Diagram*


A0
A1
A2
A3
A4
A5
ROW SELECT 1-OF-64
MEMORY ARRAY 64 ROWS 64 COLUMNS
COLUMN I/O CIRCUITS
COLUMN SELECT
D_IN (D)
CS (S)
WE (W)
D_OUT (Q)
A11
A10
A9
A8
A7
A6
1
2
3
4
5
6
7
8
10
11
12
13
14
15
16
17

TL/D/5257–1

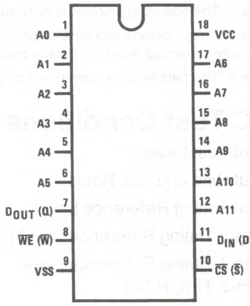
Logic Symbol*


18 VCC
9 VSS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DIN (D)
DOUT (Q)
D_IN (D)
CS (S)
WE (W)

TL/D/5257–2

Connection Diagram*

Dual-In-Line Package


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
DOUT (Q) 7
WE (W) 8
VSS 9
18 VCC
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 DIN (D)
10 CS (S)

TL/D/5257–3

Top View

Pin Names*

A0–A11	Address Inputs
WE (W)	Write Enable
CS (S)	Chip Select
D_{IN} (D)	Data In
D_{OUT} (Q)	Data Out
V_{CC}	Power (5V)
V_{SS}	Ground

Order Number NMC2147HJ-1, NMC2147HJ-2, NMC2147HJ-3, or NMC2147HJ-3L
See NS Package Number J18A

*The symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Relative to VSS	−3.5V to +7V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1.2W
DC Output Current	20 mA
Bias Temperature Range	−65°C to +135°C
Lead Temperature (Soldering, 10 sec.)	300°C

Truth Table*

$\overline{CS}$ (S)	$\overline{WE}$ ($\overline{W}$)	DIN (D)	DOUT (Q)	Mode	Power
H	X	X	Hi-Z	Not Selected	Standby
L	L	H	Hi-Z	Write 1	Active
L	L	L	Hi-Z	Write 0	Active
L	H	X	DOUT	Read	Active

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ± 10% (Notes 1 and 2)

Symbol	Parameter	Conditions	NMC2147H-3L		NMC2147H-1 NMC2147H-2 NMC2147H-3		NMC2147H		Units
			Min	Max	Min	Max	Min	Max	
|ILI|	Input Load Current (All Input Pins)	VIN = 0V to 5.5V, VCC = Max		10		10		10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = GND to 4.5V, VCC = Max		50		50		50	μA
VIL	Input Low Voltage		−3.0	0.8	−3.0	0.8	−3.0	0.8	V
VIH	Input High Voltage		2.0	6.0	2.0	6.0	2.0	6.0	V
VOL	Output Low Voltage	IOL = 8.0 mA		0.4		0.4		0.4	V
VOH	Output High Voltage	IOH = −4.0 mA	2.4		2.4		2.4		V
ICC	Power Supply Current	VIN = 5.5V, TA = 0°C, Output Open		125		180		160	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		20		30		20	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min, $\overline{CS}$ = Lower of VCC or VIH Min		30		40		30	mA

Capacitance TA = 25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
CIN	Address/Control Capacitance	VIN = 0V		5	pF
COUT	Output Capacitance	VOUT = 0V		6	pF

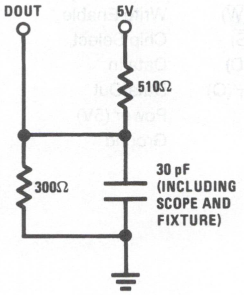
Note 1: The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 2: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper orientation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3: This parameter is guaranteed by periodic testing.

AC Test Conditions

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Level (H-1)	1.5V
Output Timing Reference Level (H-2, H-3, H-3L)	0.8V and 2.0V
Output Load	See *Figure 1*



TL/D/5257–4

FIGURE 1. Output Load

*Symbols in parentheses are proposed industry standard.

Read Cycle AC Electrical Characteristics

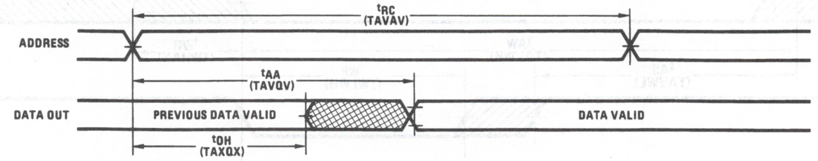
TA = 0°C to 70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	35		45		55		70		ns
t_{AA}	TAVQV	Address Access Time		35		45		55		70	ns
t_{ACS}	TSLQV	Chip Select Access Time (Notes 4)		35		45		55		70	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 5)	5		5		10		10		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 5)	0	30	0	30	0	30	0	30	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		5		ns
t_{PU}	TSLIH	Chip Select to Power-Up	0		0		0		0		ns
t_{PD}	TSHIL	Chip Deselect to Power-Down		20		20		20		30	ns

Max Access/Current	NMC2147H-1	NMC2147H-2	NMC2147H-3	NMC2147H-3L	NMC2147H
Access (TAVQV—ns)	35	45	55	55	70
Active Current (ICC—mA)	180	180	180	125	160
Standby Current (ISB—mA)	30	30	30	20	20

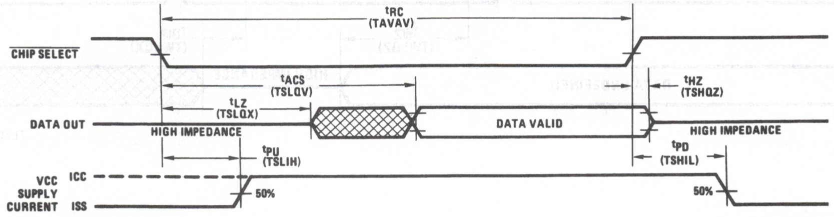
Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)


tRC
(TAVAV)
ADDRESS
tAA
(TAVQV)
DATA OUT
PREVIOUS DATA VALID
DATA VALID
tOH
(TAXQX)

TL/D/5257-5

Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 4)


tRC
(TAVAV)
CHIP SELECT
tACS
(TSLQV)
tHZ
(TSHQZ)
tLZ
(TSLQX)
DATA OUT
HIGH IMPEDANCE
DATA VALID
HIGH IMPEDANCE
tPU
(TSLIH)
tPD
(TSHIL)
VCC
SUPPLY
CURRENT
ICC
ISS
50%
50%

TL/D/5257-6

Note 4: Addresses must be valid coincident with or prior to the chip select transition from high to low.

Note 5: Measured ±50 mV from steady state voltage. This parameter is sampled and not 100% tested.

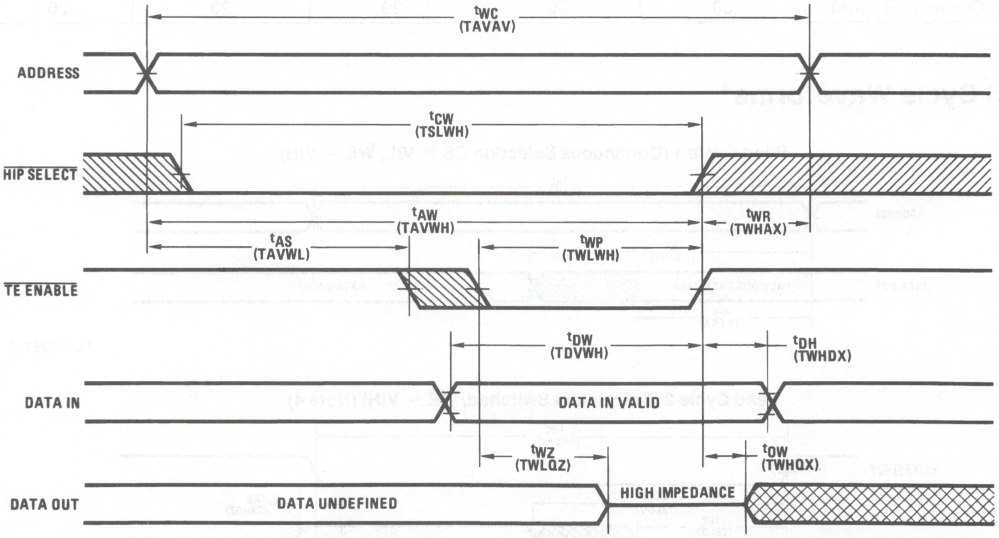
*The symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	35		45		55		70		ns
t_{CW}	TSLWH	Chip Select to End of Write	35		45		45		55		ns
t_{AW}	TAVWH	Address Valid to End of Write	35		45		45		55		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		0		0		ns
t_{WP}	TWLWH	Write Pulse Width	20		25		25		40		ns
t_{WR}	TWHAX	Write Recovery Time	0		0		10		15		ns
t_{DW}	TDVWH	Data Set-Up Time	20		25		25		30		ns
t_{DH}	TWHDX	Data Hold Time	10		10		10		10		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 5)	0	20	0	25	0	25	0	35	ns
t_{OW}	TWHQX	Output Active from End of Write (Note 5)	0		0		0		0		ns

Write Cycle Waveforms* (Note 6)

Write Cycle 1 (Write Enable Limited)

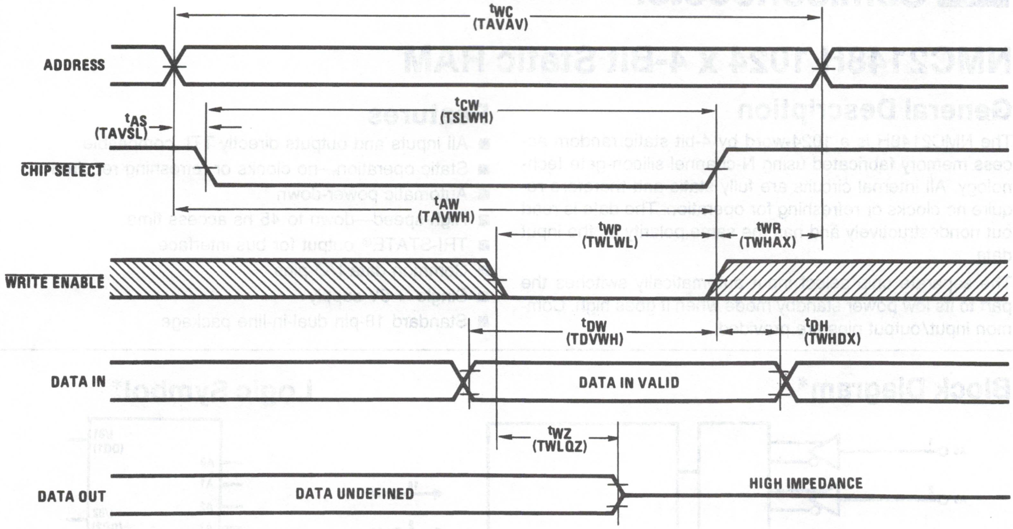


t_{WC} (TAVAV)
ADDRESS
t_{CW} (TSLWH)
HIP SELECT
t_{AW} (TAVWH)
t_{WR} (TWHAX)
t_{AS} (TAVWL)
t_{WP} (TWLWH)
TE ENABLE
t_{DW} (TDVWH)
t_{DH} (TWHDX)
DATA IN
DATA IN VALID
t_{WZ} (TWLQZ)
t_{OW} (TWHQX)
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE

TL/D/5257-7

Write Cycle Waveforms* (Note 6)

Write Cycle 2 (Chip Select Limited)


t_{WC} (TAVAV)
ADDRESS
t_{AS} (TAVSL)
t_{CW} (TSLWH)
CHIP SELECT
t_{AW} (TAVWH)
t_{WP} (TWLWL)
t_{WR} (TWHAX)
WRITE ENABLE
t_{DW} (TDVWH)
t_{DH} (TWHDX)
DATA IN
DATA IN VALID
t_{WZ} (TWLQZ)
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE

TL/D/5257-8

Note 6: The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions to prevent an erroneous write.

*The symbols in parentheses are proposed industry standard.

National Semiconductor

NMC2148H 1024 x 4-Bit Static RAM

General Description

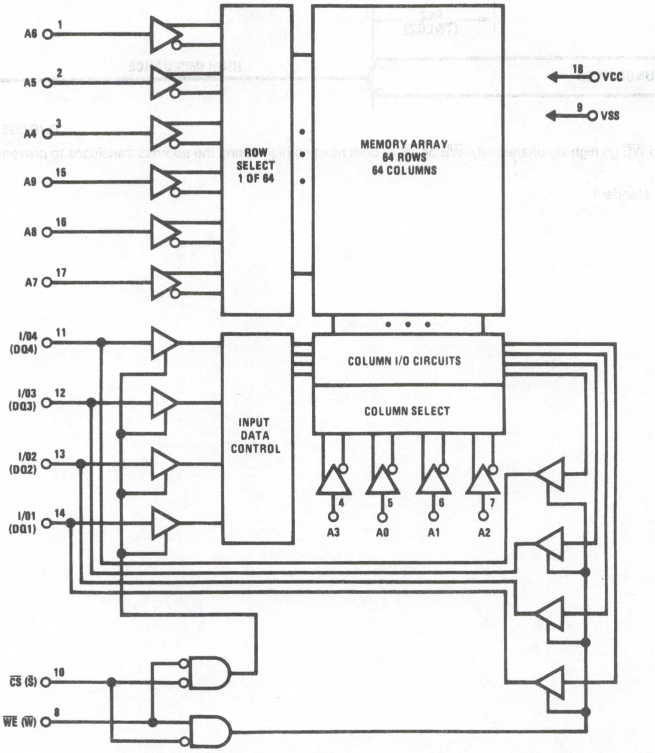
The NMC2148H is a 1024-word by 4-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip select input automatically switches the part to its low power standby mode when it goes high. Common input/output pins are provided.

Features

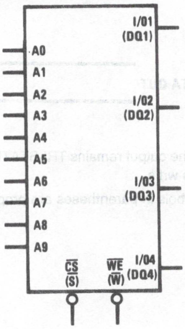
- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power-down
- High-speed—down to 45 ns access time
- TRI-STATE® output for bus interface
- Common data I/O pins
- Single +5V supply
- Standard 18-pin dual-in-line package

Block Diagram*


A6 1
A5 2
A4 3
A9 15
A8 16
A7 17
ROW SELECT 1 OF 64
MEMORY ARRAY 64 ROWS 64 COLUMNS
18 VCC
9 VSS
I/04 (DQ4) 11
I/03 (DQ3) 12
I/02 (DQ2) 13
I/01 (DQ1) 14
INPUT DATA CONTROL
COLUMN I/O CIRCUITS
COLUMN SELECT
4 A3
5 A0
6 A1
7 A2
CS (S) 10
WE (W) 8

TL/D/7404-1

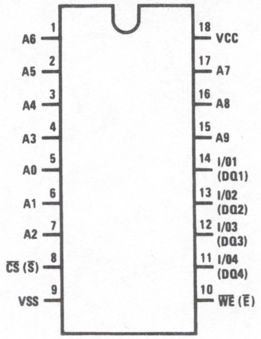
Logic Symbol*


A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
I/01 (DQ1)
I/02 (DQ2)
I/03 (DQ3)
I/04 (DQ4)
CS (S)
WE (W)

TL/D/7404-3

Connection Diagram*

Dual-In-Line Package


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
CS (S) 8
VSS 9
18 VCC
17 A7
16 A8
15 A9
14 I/01 (DQ1)
13 I/02 (DQ2)
12 I/03 (DQ3)
11 I/04 (DQ4)
10 WE (E)

TL/D/7404-2

Top View

Pin Names*

A0–A9	Address Inputs
WE (W)	Write Enable
CS (S)	Chip Select
1/01–1/04 (DQ1–DQ4)	Data Input/Output
VCC	Power (5V)
VSS	Ground

Order Number NMC2148HJ-L, NMC2148HJ-3L, NMC2148HJ, NMC2148HJ-2 or NMC2148HJ-3
See NS Package Number J18A

*Symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin with Respect to VSS	−3.5V to +7V
Storate Temperature	−65°C to +150°C
Temperature with Bias	−10°C to +85°C
DC Output Current	20 mA
Power Dissipation	1.2W
Lead Temperature (Soldering, 10 sec.)	300°C

Truth Table

$\overline{CS}$	$\overline{WE}$	I/O	Mode	Power
H	X	Hi-Z	Standby	Standby
L	L	H	Write 1	Active
L	L	L	Write 0	Active
L	H	DOUT	Read	Active

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ± 10% (Notes 1 and 2)

Symbol	Parameter	Conditions	NMC2148H-L NMC2148H-3L		NMC2148H NMC2148H-2 NMC2148H-3		Units
			Min	Max	Min	Max	
|ILI|	Input Load Current (All Input Pins)	VIN = 0V to 5.5V, VCC = Max		10		10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = GND to 4.5V, VCC = Max		50		50	μA
VIL	Input Low Voltage		−2.5	0.8	−2.5	0.8	V
VIH	Input High Voltage		2.1	6.0	2.1	6.0	V
VOL	Output Low Voltage	IOL = 8.0 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −4.0 mA	2.4		2.4		V
ICC	Power Supply Current	VIN = 5.5V, TA = 0°C, Output Open		125		180	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		20		30	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min, $\overline{CS}$ = Lower of VCC or VIH Min		30		40	mA
|IOS|	Output Short Circuit Current	VOUT = GND to VCC		250		250	mA

Capacitance TA = 25°C, f = 1.0 MHz (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
CIN	Address/Control Capacitance	VIN = 0V		5	pF
CI/O	Input/Output Capacitance	VI/O = 0V		7	pF

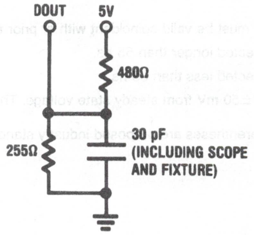
Note 1: The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 2: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper operation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3: This parameter is guaranteed by periodic testing.

AC Test Conditions

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Levels	0.8V and 2.0V
Output Load	See *Figure 1*



TL/D/7404–4

FIGURE 1. Output Load

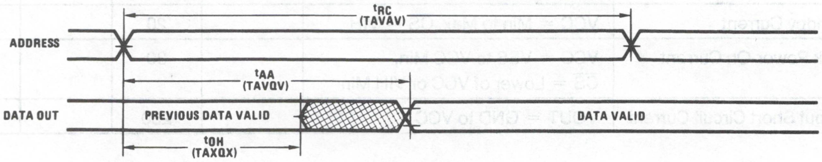
Read Cycle AC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2148H-2		NMC2148H-3 NMC2148H-3L		NMC2148H NMC2148H-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	45		55		70		ns
t_{AA}	TAVQV	Address Access Time		45		55		70	ns
t_{ACS1}	TSLQV1	Chip Select Access Time (Notes 4 and 5)		45		55		70	ns
t_{ACS2}	TLSQV2	Chip Select Access Time (Notes 4 and 6)		55		65		80	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 7)	20		20		20		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 7)	0	20	0	20	0	20	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		ns
t_{PU}	TSLIH	Chip Select to Power-Up	0		0		0		ns
t_{PD}	TSHIL	Chip Deselect to Power-Down		30		30		30	ns

Max Access/Current	NMC2148H-2	NMC2148H-3	NMC2148H	NMC2148H-3L	NMC2148H-L
Access (TAVQV—ns)	45	55	70	55	70
Active Current (ICC—mA)	180	180	180	125	125
Standby Current (ISB—mA)	30	30	30	20	20

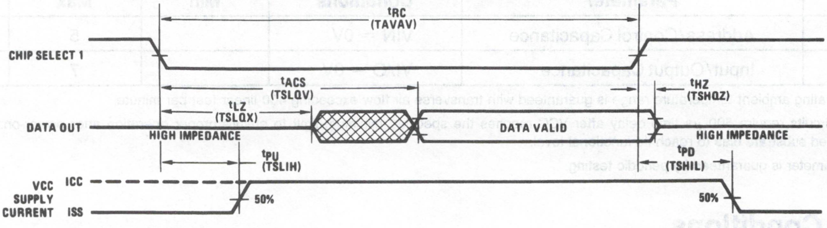
Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)


tRC
(TAVAV)
ADDRESS
tAA
(TAVQV)
DATA OUT
PREVIOUS DATA VALID
DATA VALID
tOH
(TAXQX)

TL/D/7404-5

Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 4)


tRC
(TAVAV)
CHIP SELECT 1
tACS
(TSLQV)
tLZ
(TSLQX)
DATA OUT
HIGH IMPEDANCE
DATA VALID
tHZ
(TSHQZ)
HIGH IMPEDANCE
tPU
(TSLIH)
tPD
(TSHIL)
VCC
SUPPLY
CURRENT
ICC
ISS
50%
50%

TL/D/7404-6

Note 4: Addresses must be valid coincident with or prior to the chip select transition from high to low.

Note 5: Chip deselected longer than 55 ns.

Note 6: Chip deselected less than 55 ns.

Note 7: Measured ±50 mV from steady state voltage. This parameter is sampled and not 100% tested.

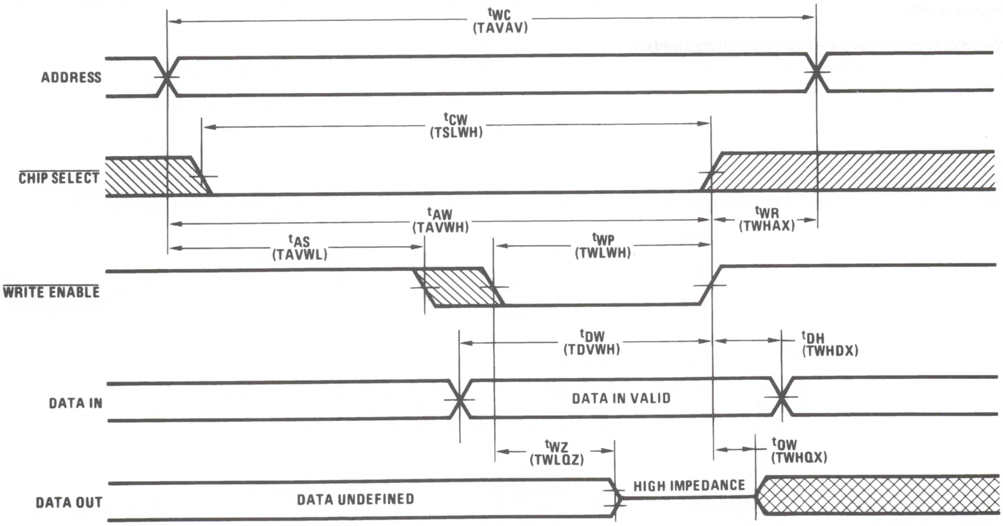
*The symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2148H-2		NMC2148H-3 NMC2148H-3L		NMC2148H NMC2148H-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	45		55		70		ns
t_{CW}	TSLWH	Chip Select to End of Write	40		50		65		ns
t_{AW}	TAVWH	Address Valid to End of Write	40		50		65		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		0		ns
t_{WP}	TWLWH	Write Pulse Width	35		40		50		ns
t_{WR}	TWHAX	Write Recovery Time	5		5		5		ns
t_{DW}	TDVWH	Data Set-Up Time	20		20		25		ns
t_{DH}	TWHDX	Data Hold Time	0		0		0		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 7)	0	15	0	20	0	25	ns
t_{OW}	TWHQX	Output Active from End of Write (Note 7)	0		0		0		ns

Write Cycle Waveforms* (Note 8)

Write Cycle 1 (Write Enable Limited)

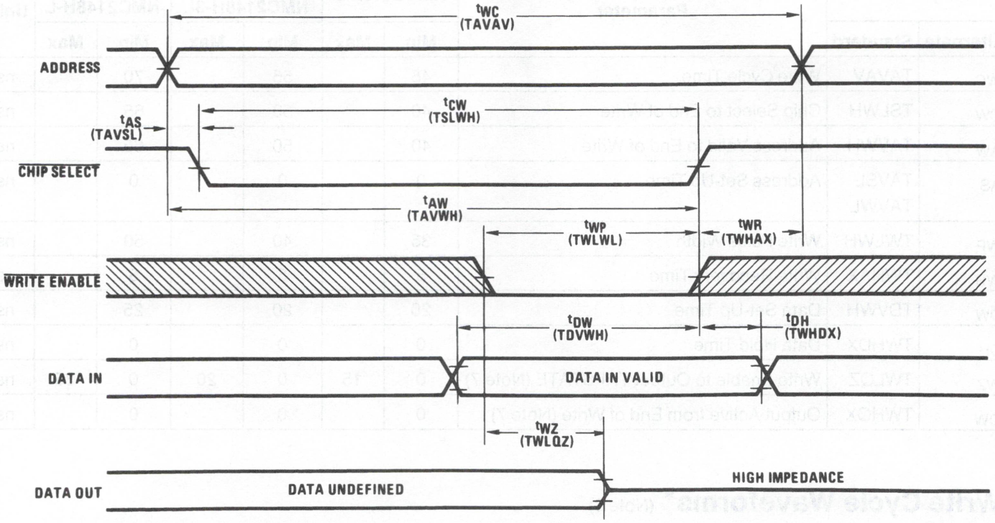


tWC
(TAVAV)
ADDRESS
tCW
(TSLWH)
CHIP SELECT
tAW
(TAVWH)
tWR
(TWHAX)
tAS
(TAVWL)
tWP
(TWLWH)
WRITE ENABLE
tDW
(TDVWH)
tDH
(TWHDX)
DATA IN
DATA IN VALID
tWZ
(TWLQZ)
tOW
(TWHQX)
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE

TL/D/7404–7

Write Cycle Waveforms* (Note 8) (Continued)

Write Cycle 2 (Chip Select Limited)


tWC
(TAVAV)
ADDRESS
tAS
(TAVSL)
tCW
(TSLWH)
CHIP SELECT
tAW
(TAVWH)
tWP
(TWLWL)
tWR
(TWHAX)
WRITE ENABLE
tDW
(TDVWH)
tDH
(TWHDX)
DATA IN
DATA IN VALID
tWZ
(TWLQZ)
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE

TL/D/7404-8

Note 8: The output remains TRI-STATE if the $\overline{\text{CS}}$ and $\overline{\text{WE}}$ go high simulataneously. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ or both must be high during the address transitions to prevent an erroneous write.

*Symbols in parentheses are proposed industry standard.

National Semiconductor

DM75S68/DM85S68/DM75S68A/DM85S68A 16 x 4 Edge Triggered Registers

General Description

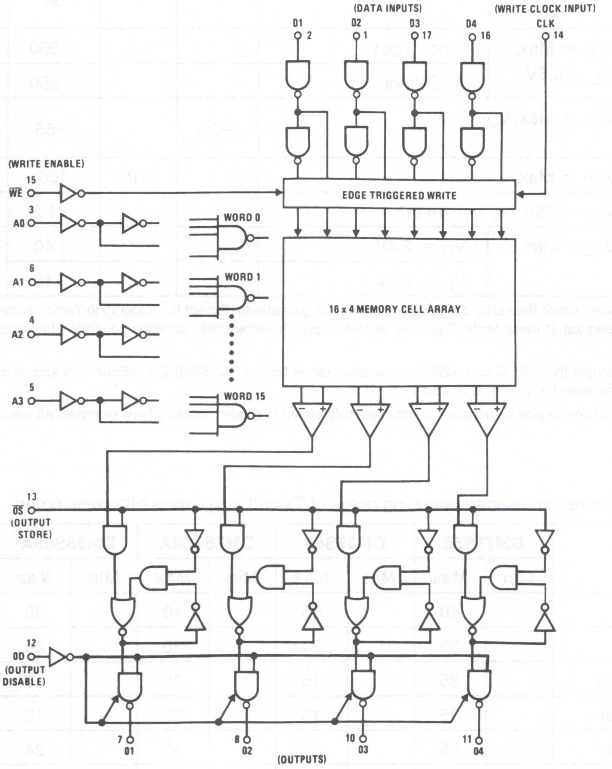
These Schottky memories are addressable "D" register files. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a TRI-STATE® output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state. This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance TRI-STATE condition.

Features

- On-chip output register
- PNP inputs reduce input loading
- Edge triggered write
- High speed—20 ns typ
- All parameters guaranteed over temperature
- TRI-STATE output
- Schottky-clamped for high speed
- Optimized for register stack applications
- Typical power dissipation—350 mW

Logic and Block Diagram


(DATA INPUTS)
(WRITE CLOCK INPUT)
D1 2
D2 1
D3 17
D4 16
CLK 14
(WRITE ENABLE)
15 WE
3 A0
6 A1
4 A2
5 A3
WORD 0
WORD 1
WORD 15
EDGE TRIGGERED WRITE
16 x 4 MEMORY CELL ARRAY
13 OS (OUTPUT STORE)
12 OD (OUTPUT DISABLE)
7 O1
8 O2
10 O3
11 O4
(OUTPUTS)

TL/F/9233–1

Pin Names

A_0–A_3	**Address Inputs**
D_1–D_4	Data Inputs
O_1–O_4	Data Outputs
$\overline{WE}$	Write Enable
CLK	Write Clock Input
$\overline{OS}$	Output Store
OD	Output Disable

O_D	$\overline{W_E}$	CLK	$\overline{O_S}$	MODE	OUTPUTS
0	X	X	0	Output Store	Data From Last Addressed Location
X	0	↑	X	Write Data	Dependent on State of OD and $\overline{OS}$
0	X	X	1	Read Data	Data Stored in Addressed Location
1	X	X	0	Output Store	High Impedance State
1	X	X	1	Output Disable	High Impedance State

0 = Low Level
1 = High Level
X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DM85S68/DM85S68A	4.75	5.25	V
DM75S68/DM75S68A	4.5	5.5	V
Temperature, T_A			
DM85S68/DM85S68A	0	70	°C
DM75S68/DM75S68A	−55	+125	°C

Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM75S68/DM75S68A	2.4			V
			I_{OH} = −5.2 mA, DM85S68/DM85S68A	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM75S68/DM75S68A			0.5	V
			DM85S68/DM85S68A			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.4V				25	µA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_{IH} = 5.5V				50	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IL} = 0.5V	Clock Input			−500	µA
			All Others			−250	µA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_{OL} = 0V		−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max			70	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{OZ}	TRI-STATE Output Current	V_{CC}= Max	V_O = 2.4V			+40	µA
			V_O = 0.5V			−40	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2. Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75S68/DM75S68A and across the 0°C to +70°C range for the DM85S68/DM85S68A. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics over recommended operating range of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		DM75S68		DM85S68		DM75S68A		DM85S68A		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZH}	Output Enable to High Level			40		35		40		35	ns
t_{ZL}	Output Enable to Low Level			30		24		30		24	ns
t_{HZ}	Output Disable Time from High Level			35		15		35		15	ns
t_{LZ}	Output Disable Time from Low Level			35		18		35		18	ns
t_{AA}	Access Time	Address to Output		55		40		45		24	ns
t_{OSA}		Output Store to Output		35		30		35		20	ns
t_{CA}		Clock to Output		50		40		50		35	ns

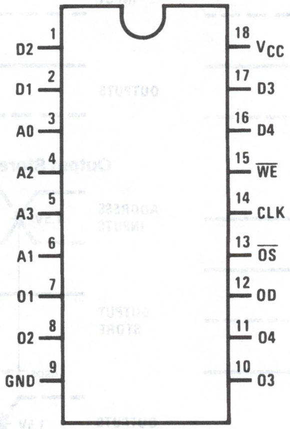
Switching Characteristics

over recommended operating range of T_A and V_{CC} unless otherwise noted (Continued)

Symbol	Parameter		DM75S68		DM85S68		DM75S68A		DM85S68A		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ASC}	Set-Up Time	Address to Clock	25		15		25		15		ns
t_{DSC}		Data to Clock	15		5		15		5		ns
t_{ASOS}		Address to Output Store	40		30		40		10		ns
t_{WESC}		Write Enable Set-Up Time	10		5		10		5		ns
t_{OSSC}		Store before Write	15		10		15		10		ns
t_{AHC}	Hold Time	Address from Clock	15		10		15		10		ns
t_{DHC}		Data from Clock	20		15		20		15		ns
t_{AHOS}		Address from Output Store	10		5		10		2		ns
t_{WEHC}		Write Enable Hold Time	20		15		20		10		ns

Connection Diagram

Dual-In-Line Package



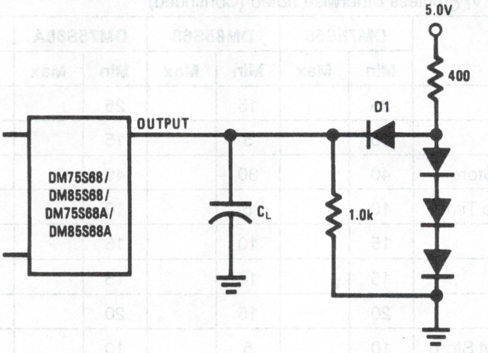
D2 1
D1 2
A0 3
A2 4
A3 5
A1 6
O1 7
O2 8
GND 9
18 V_{CC}
17 D3
16 D4
15 $\overline{WE}$
14 CLK
13 $\overline{OS}$
12 OD
11 O4
10 O3

TL/F/9233-2

Top View

Order Number DM75S68J, DM85S68J, DM85S68N, DM75S68AJ, DM85S68AJ or DM85S68AN
See NS Package Number J18A or N18A

AC Test Circuit and Switching Time Waveforms

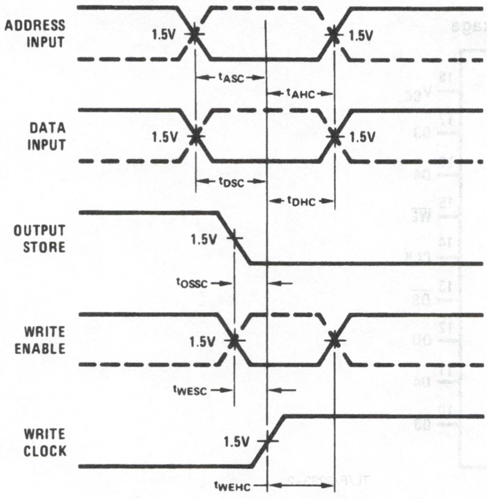

5.0V
400
D1
OUTPUT
DM75S68/
DM85S68/
DM75S68A/
DM85S68A
C_L
1.0k

C_L = 5.0 pF for t_{HZ}, t_{LZ}
C_L = 30 pF for all others
C_L includes probe and jig capacitance
All diodes are 1N3064

TL/L/9233-3

Write Cycle

Clock Set-Up and Hold Time


ADDRESS INPUT
1.5V
1.5V
t_{ASC}
t_{AHC}
DATA INPUT
1.5V
1.5V
t_{DSC}
t_{DHC}
OUTPUT STORE
1.5V
t_{OSSC}
WRITE ENABLE
1.5V
t_{WESC}
WRITE CLOCK
1.5V
t_{WEHC}

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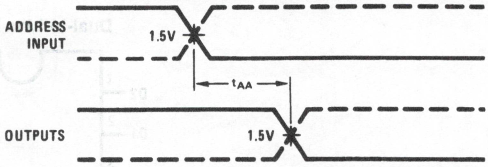
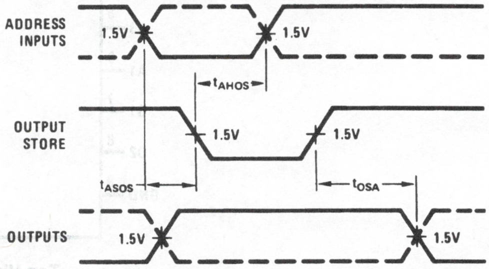
Read Cycle

Address to Output Access Time


ADDRESS INPUT
1.5V
t_{AA}
OUTPUTS
1.5V

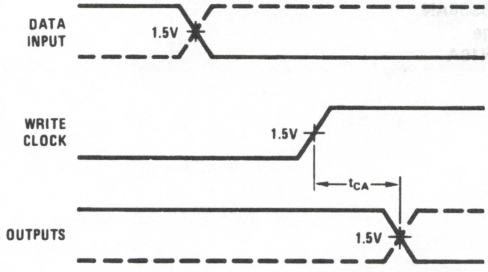
TL/L/9233-6

Output Store Access, Set-Up and Hold Time


ADDRESS INPUTS
1.5V
1.5V
t_{AHOS}
OUTPUT STORE
1.5V
1.5V
t_{ASOS}
t_{OSA}
OUTPUTS
1.5V
1.5V

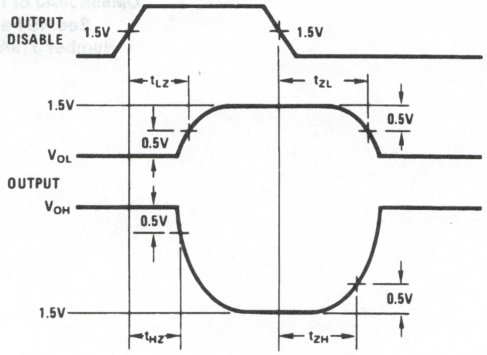
TL/L/9233-7

Clock to Output Access


DATA INPUT
1.5V
WRITE CLOCK
1.5V
t_{CA}
OUTPUTS
1.5V

TL/L/9233-5

Output Disable and Enable Time


OUTPUT DISABLE
1.5V
1.5V
t_{LZ}
t_{ZL}
1.5V
0.5V
0.5V
V_{OL}
OUTPUT
V_{OH}
0.5V
0.5V
1.5V
t_{HZ}
t_{ZH}

TL/L/9233-8

Note: Input waveforms supplied by pulse generator having the following characteristics: V = 3.0V, $t_R \leq 2.5$ ns, PRR ≤ 1.0 MHz and Z_{OUT} = 50M.

Section 6

Appendices/ Physical Dimensions

Section 6 Contents

STAR™ Surface Mount Tape-and-Reel Specification 6-3
Physical Dimensions 6-31

Bookshelf
Distributors

National Semiconductor

PRELIMINARY

STAR™
SEMICONDUCTOR TAPE-AND-REEL SYSTEM

STAR™ Surface Mount Tape-and-Reel Specification

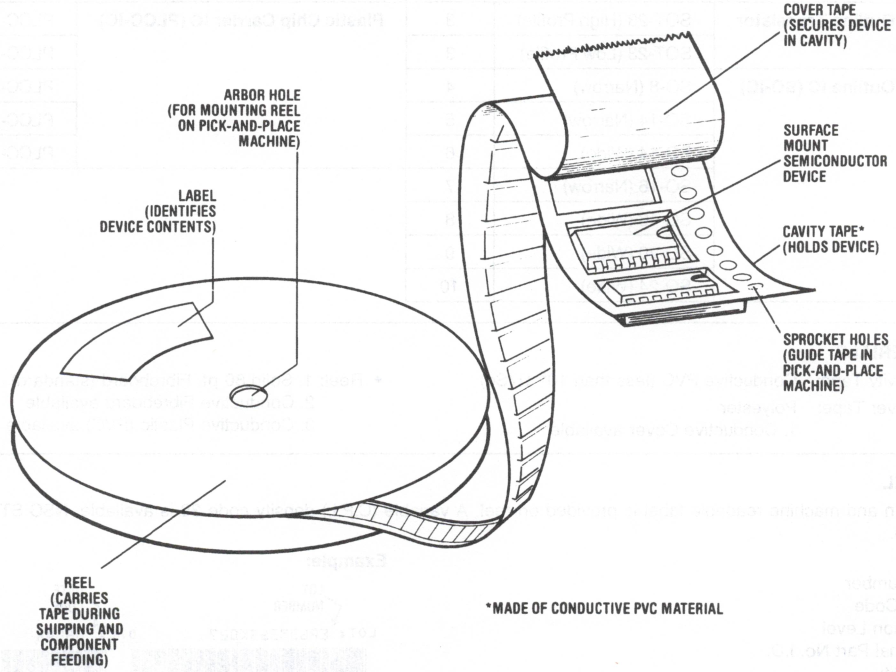
General Description

Tape-and-Reel is a new method for shipment of surface mount devices. This approach simplifies the handling of semiconductors for automated circuit board assembly systems. A Tape-and-Reel holds hundreds-to-thousands of surface mount devices (as compared with less than 100 devices in a rail), so that pick-and-place machines have to be reloaded less frequently. This savings in labor will further reduce manufacturing costs for automated circuit board assembly.

Features

- Conductive PVC material redeuces static charge build-up
- Fully meets proposed EIA standard RS-481A (taping of surface-mounted components for automatic placing)
- Fully compatible with National's surface mount package types
- Variable code density code 39 bar code label for Automated Inventory Management availability
- Mechanical samples of surface mount packages available in Tape-and-Reel for automated assembly process development
- Single Tape-and-Reel holds hundreds-to-thousands of surface mount semiconductors for additional labor savings
- Conductive cover Tape-and-Reel availability
- Reels individually packed

Tape-and-Reel Diagram

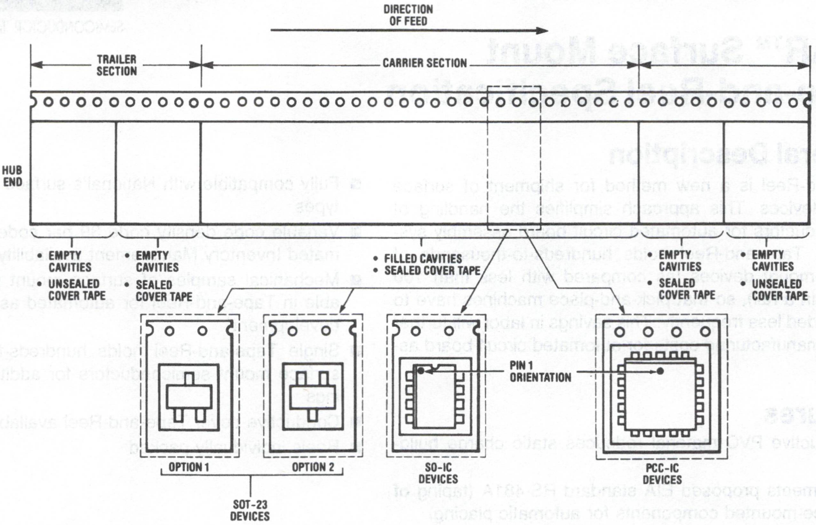

COVER TAPE (SECURES DEVICE IN CAVITY)
ARBOR HOLE (FOR MOUNTING REEL ON PICK-AND-PLACE MACHINE)
SURFACE MOUNT SEMICONDUCTOR DEVICE
LABEL (IDENTIFIES DEVICE CONTENTS)
CAVITY TAPE* (HOLDS DEVICE)
SPROCKET HOLES (GUIDE TAPE IN PICK-AND-PLACE MACHINE)
REEL (CARRIES TAPE DURING SHIPPING AND COMPONENT FEEDING)

*MADE OF CONDUCTIVE PVC MATERIAL

TL/HH/8352–1

Tape-and-Reel Overview

TAPE FORMAT AND DEVICE ORIENTATION


DIRECTION OF FEED
TRAILER SECTION
CARRIER SECTION
HUB END
• EMPTY CAVITIES
• UNSEALED COVER TAPE
• EMPTY CAVITIES
• SEALED COVER TAPE
• FILLED CAVITIES
• SEALED COVER TAPE
• EMPTY CAVITIES
• SEALED COVER TAPE
• EMPTY CAVITIES
• UNSEALED COVER TAPE
OPTION 1
OPTION 2
SOT-23 DEVICES
SO-IC DEVICES
PIN 1 ORIENTATION
PCC-IC DEVICES

TL/HH/8352-2

		Page
Small Outline Transistor	SOT-23 (High Profile)	3
	SOT-23 (Low Profile)	3
Small Outline IC (SO-IC)	SO-8 (Narrow)	4
	SO-14 (Narrow)	5
	SO-14 (Wide)	6
	SO-16 (Narrow)	7
	SO-16 (Wide)	8
	SO-20 (Wide)	9
	SO-24 (Wide)	10

		Page
Plastic Chip Carrier IC (PLCC-IC)	PLCC-20	11
	PLCC-28	12
	PLCC-44	13
	PLCC-68	14
	PLCC-84	15

MATERIALS

- Cavity Tape: Conductive PVC (less than 10^5 Ω/Sq)
- Cover Tape: Polyester
  1. Conductive Cover available
- Reel: 1. Solid 80 pt. Fibreboard (standard)
  2. Conductive Fibreboard available
  3. Conductive Plastic (PVC) available

LABEL

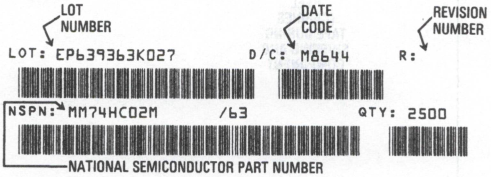
Human and machine readable label is provided on reel. A variable (C.P.I.) density code 39 is available. NSC STD Label (7.6 C.P.I.).

Field
Lot Number
Date Code
Revision Level
National Part No. I.D.
Quantity

Fields are separated by at least one blank space.

Future Tape-and-Reel packs will also include a smaller-size bar code label (high-density code 39) at the beginning of the tape. (This tape label is not available on current production.)

Example:


LOT NUMBER
DATE CODE
REVISION NUMBER
NATIONAL SEMICONDUCTOR PART NUMBER

LOT: EP6393 63K027 D/C: M8644 R:
NSPN: MM74HC02M /63 QTY: 2500

TL/HH/8352-3

National Semiconductor will also offer additional labels containing information per your specific specification.

SOT-23 (High Profile), SOT-23 (Low Profile)

TAPE FORMAT

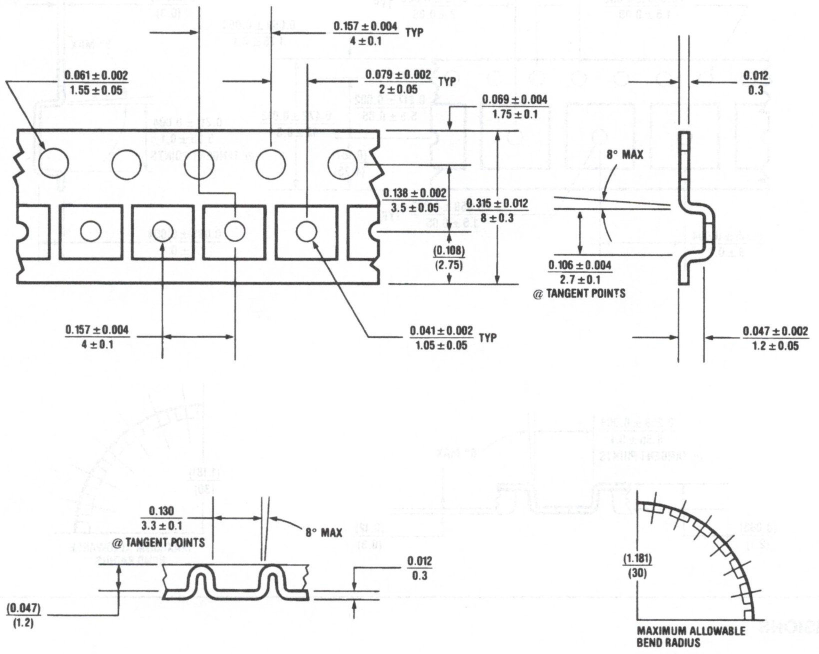
Direction of Feed ↑

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	5 (min)	Empty	Unsealed
	5 (min)	Empty	Sealed
Carrier	†*2500 (High)	Filled	Sealed
	†*3000 (Low)	Filled	Sealed
Trailer (Hub End)	2 (min)	Empty	Sealed
	2 (min)	Empty	Unsealed

*These quantities represent 7″ Reel Quantity availability.

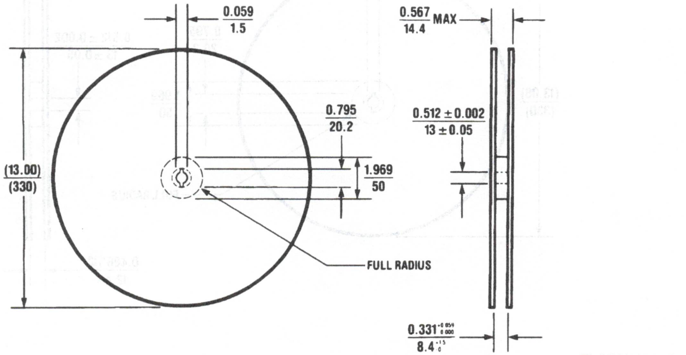
†10,000 For 13″ Reel.

TAPE DIMENSIONS


0.157 ± 0.004 / 4 ± 0.1 TYP
0.061 ± 0.002 / 1.55 ± 0.05
0.079 ± 0.002 / 2 ± 0.05 TYP
0.069 ± 0.004 / 1.75 ± 0.1
0.012 / 0.3
8° MAX
0.138 ± 0.002 / 3.5 ± 0.05
0.315 ± 0.012 / 8 ± 0.3
(0.108) / (2.75)
0.106 ± 0.004 / 2.7 ± 0.1 @ TANGENT POINTS
0.157 ± 0.004 / 4 ± 0.1
0.041 ± 0.002 / 1.05 ± 0.05 TYP
0.047 ± 0.002 / 1.2 ± 0.05
0.130 / 3.3 ± 0.1 @ TANGENT POINTS
8° MAX
0.012 / 0.3
(0.047) / (1.2)
(1.181) / (30)
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352-4

REEL DIMENSIONS


0.059 / 1.5
0.567 MAX / 14.4
0.795 / 20.2
0.512 ± 0.002 / 13 ± 0.05
(13.00) / (330)
1.969 / 50
FULL RADIUS
0.331 +0.059 / 0.000 / 8.4 +1.5 / 0

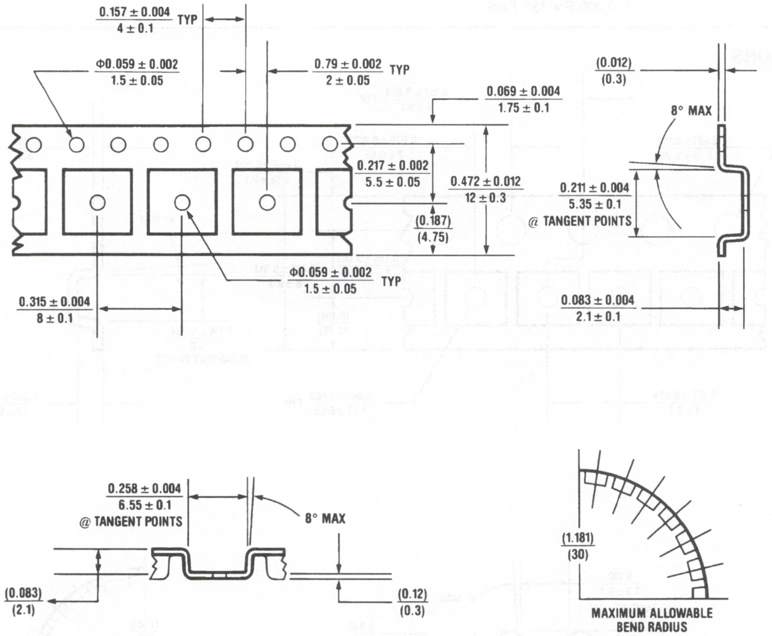
TL/HH/8352-5

SO-8 (Narrow)

TAPE FORMAT

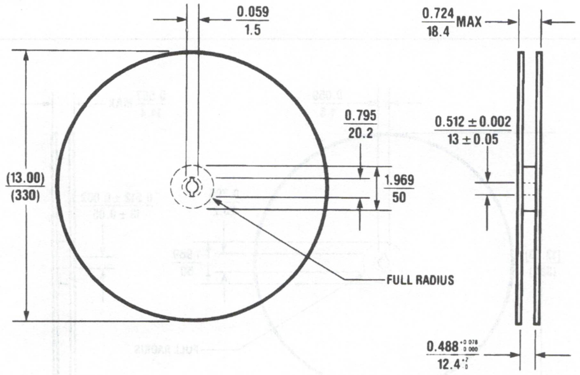
	Tape Section	# Cavities	Cavity Status	Cover Tape Status
	Leader (Start End)	5 (min)	Empty	Unsealed
Direction ↑ of Feed		5 (min)	Empty	Sealed
	Carrier	2500	Filled	Sealed
	Trailer (Hub End)	2 (min)	Empty	Sealed
		2 (min)	Empty	Unsealed

TAPE DIMENSIONS


0.157 ± 0.004 / 4 ± 0.1 TYP
Φ0.059 ± 0.002 / 1.5 ± 0.05
0.79 ± 0.002 / 2 ± 0.05 TYP
0.069 ± 0.004 / 1.75 ± 0.1
(0.012) / (0.3)
8° MAX
0.217 ± 0.002 / 5.5 ± 0.05
0.472 ± 0.012 / 12 ± 0.3
0.211 ± 0.004 / 5.35 ± 0.1 @ TANGENT POINTS
(0.187) / (4.75)
Φ0.059 ± 0.002 / 1.5 ± 0.05 TYP
0.315 ± 0.004 / 8 ± 0.1
0.083 ± 0.004 / 2.1 ± 0.1
0.258 ± 0.004 / 6.55 ± 0.1 @ TANGENT POINTS
8° MAX
(0.083) / (2.1)
(0.12) / (0.3)
(1.181) / (30)
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352-6

REEL DIMENSIONS


0.059 / 1.5
0.724 / 18.4 MAX
0.795 / 20.2
0.512 ± 0.002 / 13 ± 0.05
(13.00) / (330)
1.969 / 50
FULL RADIUS
0.488 +0.078/−0.000 / 12.4 +2/−0

TL/HH/8352-7

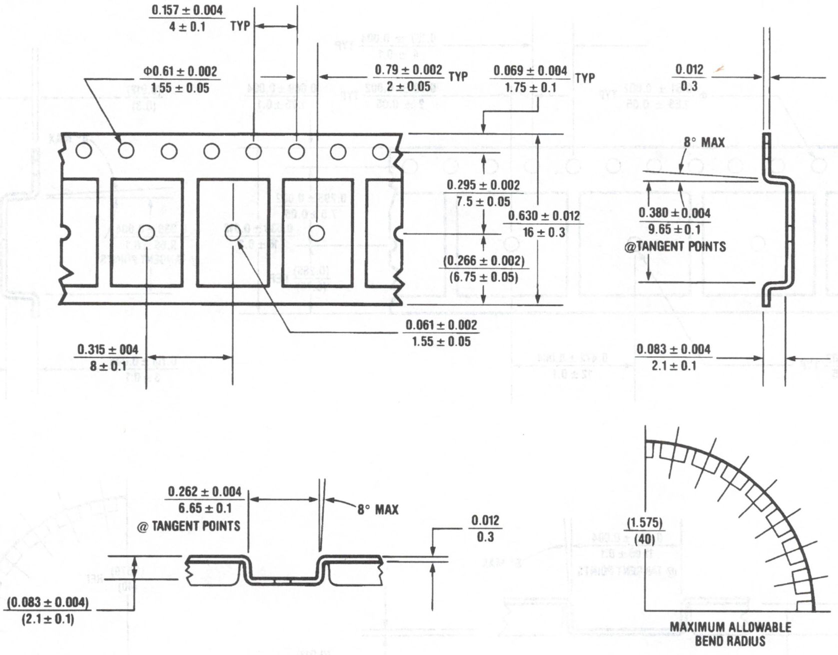
SO-14 (Narrow)

TAPE FORMAT

Direction of Feed ↑

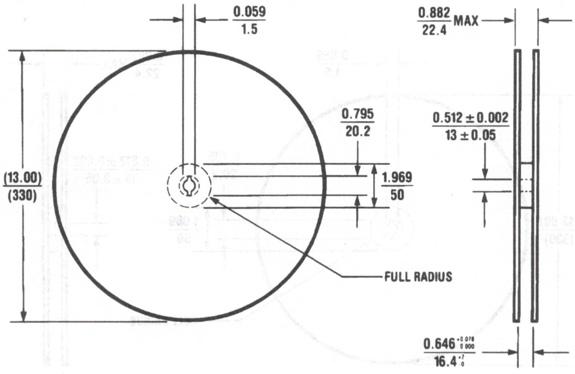
Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	5 (min)	Empty	Unsealed
	5 (min)	Empty	Sealed
Carrier	2500	Filled	Sealed
Trailer (Hub End)	2 (min)	Empty	Sealed
	2 (min)	Empty	Unsealed

TAPE DIMENSIONS


0.157 ± 0.004 / 4 ± 0.1 TYP
Φ0.61 ± 0.002 / 1.55 ± 0.05
0.79 ± 0.002 / 2 ± 0.05 TYP
0.069 ± 0.004 / 1.75 ± 0.1 TYP
0.012 / 0.3
8° MAX
0.295 ± 0.002 / 7.5 ± 0.05
0.630 ± 0.012 / 16 ± 0.3
0.380 ± 0.004 / 9.65 ± 0.1 @TANGENT POINTS
(0.266 ± 0.002) / (6.75 ± 0.05)
0.061 ± 0.002 / 1.55 ± 0.05
0.315 ± 004 / 8 ± 0.1
0.083 ± 0.004 / 2.1 ± 0.1
0.262 ± 0.004 / 6.65 ± 0.1 @ TANGENT POINTS
8° MAX
0.012 / 0.3
(0.083 ± 0.004) / (2.1 ± 0.1)
(1.575) / (40)
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352-8

REEL DIMENSIONS


0.059 / 1.5
0.882 / 22.4 MAX
0.795 / 20.2
1.969 / 50
0.512 ± 0.002 / 13 ± 0.05
(13.00) / (330)
FULL RADIUS
0.646 +0.078 / 0.000 / 16.4 +2 / 0

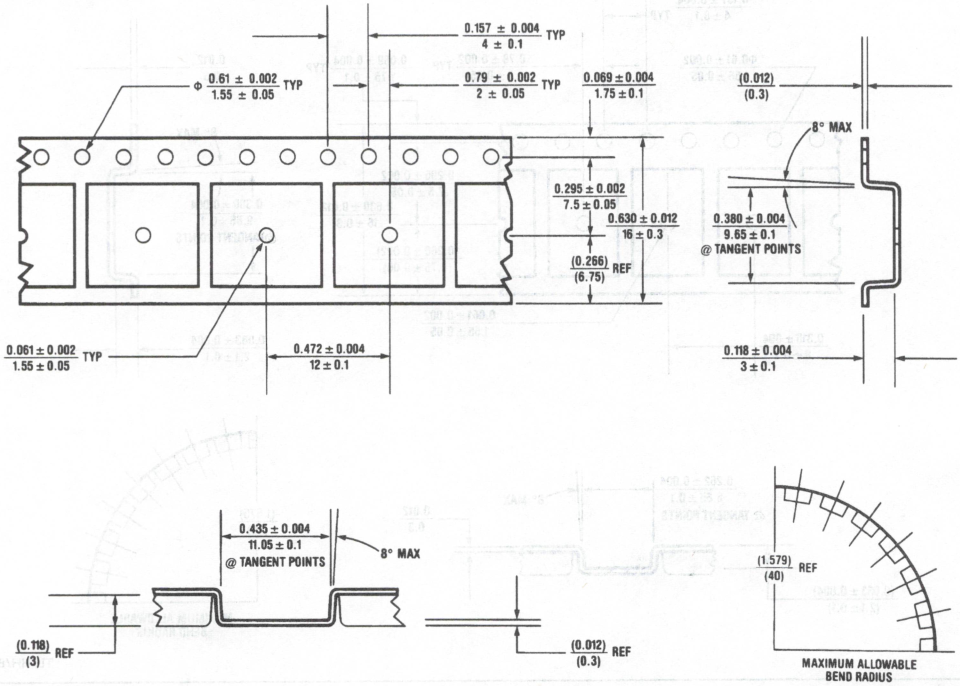
TL/HH/8352-9

SO-14 (Wide)

TAPE FORMAT

	Tape Section	# Cavities	Cavity Status	Cover Tape Status
Direction of Feed ↑	Leader (Start End)	5 (min)	Empty	Unsealed
		5 (min)	Empty	Sealed
	Carrier	1000	Filled	Sealed
	Trailer (Hub End)	2 (min)	Empty	Sealed
		2 (min)	Empty	Unsealed

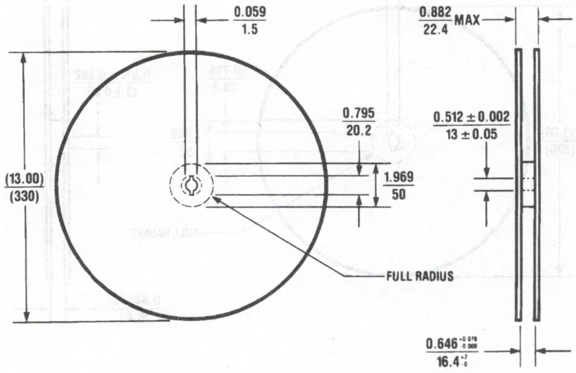
TAPE DIMENSIONS



0.157 ± 0.004 / 4 ± 0.1 TYP
Φ 0.61 ± 0.002 / 1.55 ± 0.05 TYP
0.79 ± 0.002 / 2 ± 0.05 TYP
0.069 ± 0.004 / 1.75 ± 0.1
(0.012) / (0.3)
8° MAX
0.295 ± 0.002 / 7.5 ± 0.05
0.630 ± 0.012 / 16 ± 0.3
0.380 ± 0.004 / 9.65 ± 0.1 @ TANGENT POINTS
(0.266) / (6.75) REF
0.061 ± 0.002 / 1.55 ± 0.05 TYP
0.472 ± 0.004 / 12 ± 0.1
0.118 ± 0.004 / 3 ± 0.1
0.435 ± 0.004 / 11.05 ± 0.1 @ TANGENT POINTS
8° MAX
(0.118) / (3) REF
(0.012) / (0.3) REF
(1.579) / (40) REF
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352-10

REEL DIMENSIONS



0.059 / 1.5
0.882 / 22.4 MAX
0.795 / 20.2
0.512 ± 0.002 / 13 ± 0.05
(13.00) / (330)
1.969 / 50
FULL RADIUS
0.646 +0.078 -0.000 / 16.4 +2 -0

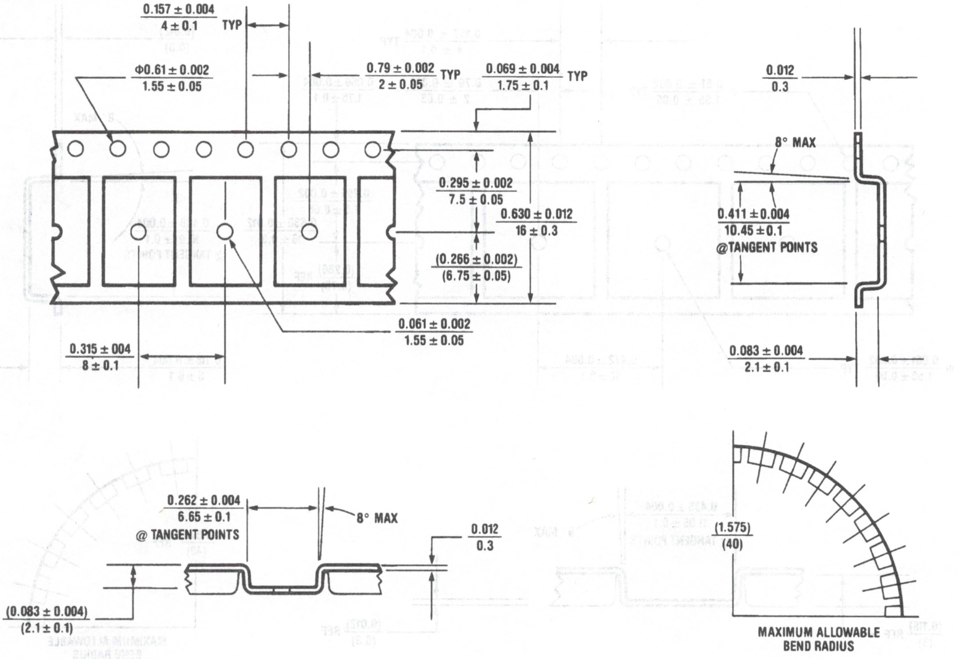
TL/HH/8352-11

SO-16 (Narrow)

TAPE FORMAT

	Tape Section	# Cavities	Cavity Status	Cover Tape Status
Direction of Feed ↑	Leader (Start End)	5 (min)	Empty	Unsealed
		5 (min)	Empty	Sealed
	Carrier	2500	Filled	Sealed
	Trailer (Hub End)	2 (min)	Empty	Sealed
		2 (min)	Empty	Unsealed

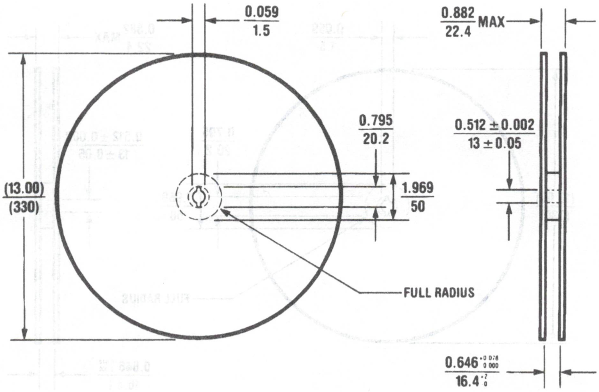
TAPE DIMENSIONS



0.157 ± 0.004 / 4 ± 0.1 TYP
Φ0.61 ± 0.002 / 1.55 ± 0.05
0.79 ± 0.002 / 2 ± 0.05 TYP
0.069 ± 0.004 / 1.75 ± 0.1 TYP
0.012 / 0.3
8° MAX
0.295 ± 0.002 / 7.5 ± 0.05
0.630 ± 0.012 / 16 ± 0.3
0.411 ± 0.004 / 10.45 ± 0.1 @TANGENT POINTS
(0.266 ± 0.002) / (6.75 ± 0.05)
0.061 ± 0.002 / 1.55 ± 0.05
0.315 ± 004 / 8 ± 0.1
0.083 ± 0.004 / 2.1 ± 0.1
0.262 ± 0.004 / 6.65 ± 0.1 @ TANGENT POINTS
8° MAX
0.012 / 0.3
(0.083 ± 0.004) / (2.1 ± 0.1)
(1.575) / (40)
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352–12

REEL DIMENSIONS



0.059 / 1.5
0.882 / 22.4 MAX
0.795 / 20.2
0.512 ± 0.002 / 13 ± 0.05
(13.00) / (330)
1.969 / 50
FULL RADIUS
$0.646^{+0.078}_{-0.000}$ / 16.4^{+2}_{-0}

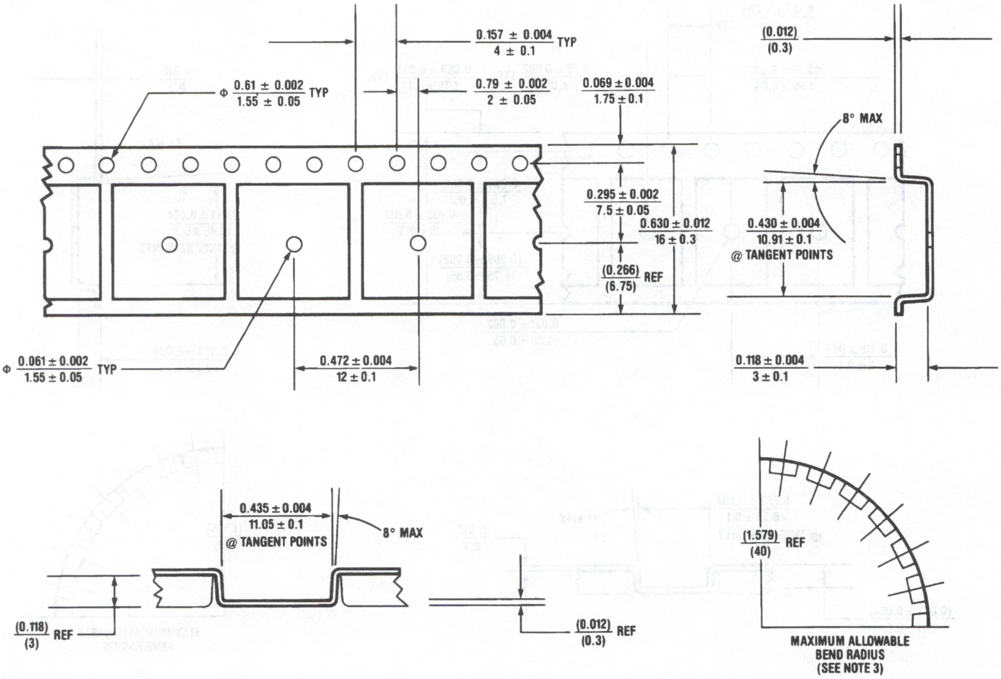
TL/HH/8352–13

SO-16 (Wide)

TAPE FORMAT

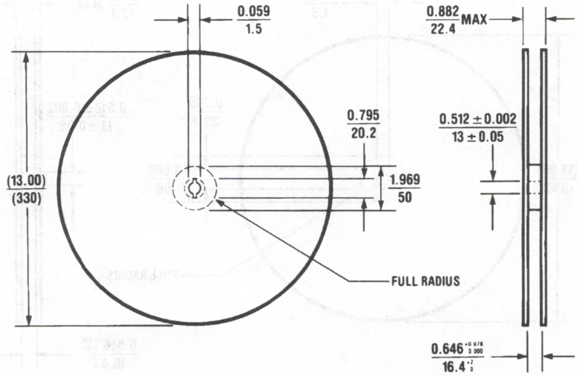
	Tape Section	# Cavities	Cavity Status	Cover Tape Status
Direction ↑ of Feed	Leader (Start End)	5 (min)	Empty	Unsealed
		5 (min)	Empty	Sealed
	Carrier	1000	Filled	Sealed
	Trailer (Hub End)	2 (min)	Empty	Sealed
		2 (min)	Empty	Unsealed

TAPE DIMENSIONS


0.157 ± 0.004 / 4 ± 0.1 TYP
(0.012) / (0.3)
Φ 0.61 ± 0.002 / 1.55 ± 0.05 TYP
0.79 ± 0.002 / 2 ± 0.05
0.069 ± 0.004 / 1.75 ± 0.1
8° MAX
0.295 ± 0.002 / 7.5 ± 0.05
0.630 ± 0.012 / 16 ± 0.3
0.430 ± 0.004 / 10.91 ± 0.1 @ TANGENT POINTS
(0.266) / (6.75) REF
Φ 0.061 ± 0.002 / 1.55 ± 0.05 TYP
0.472 ± 0.004 / 12 ± 0.1
0.118 ± 0.004 / 3 ± 0.1
0.435 ± 0.004 / 11.05 ± 0.1 @ TANGENT POINTS
8° MAX
(0.118) / (3) REF
(0.012) / (0.3) REF
(1.579) / (40) REF
MAXIMUM ALLOWABLE BEND RADIUS (SEE NOTE 3)

TL/HH/8352-14

REEL DIMENSIONS


0.059 / 1.5
0.882 / 22.4 MAX
(13.00) / (330)
0.795 / 20.2
1.969 / 50
0.512 ± 0.002 / 13 ± 0.05
FULL RADIUS
0.646 +0.078 -0.000 / 16.4 +2 -0

TL/HH/8352-15

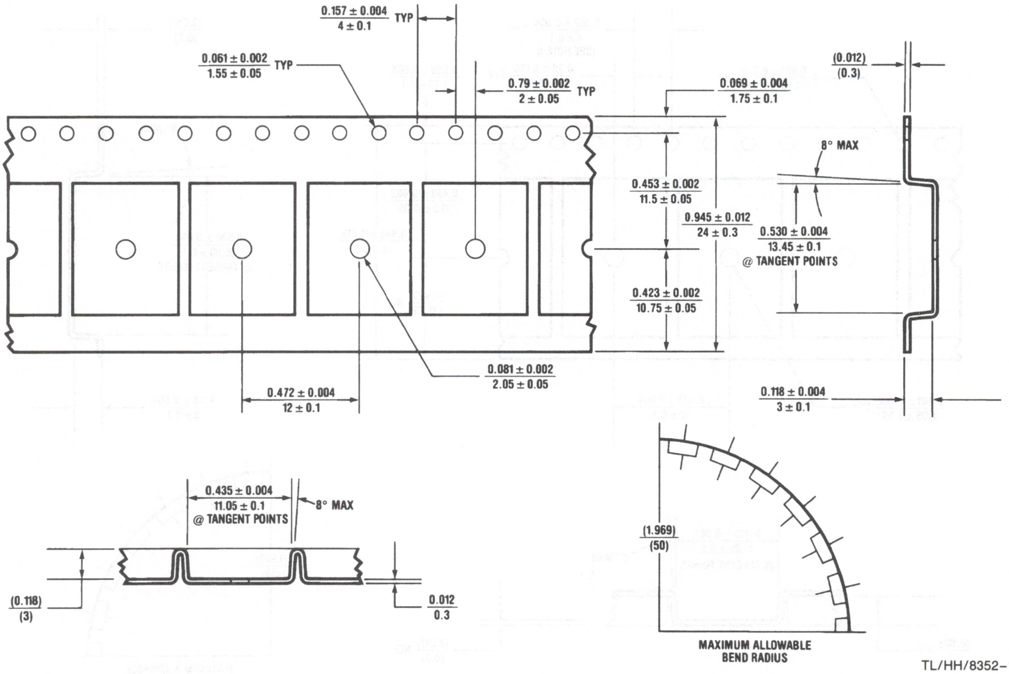
SO-20 (Wide)

TAPE FORMAT

Direction of Feed ↑

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	5 (min)	Empty	Unsealed
	5 (min)	Empty	Sealed
Carrier	1000	Filled	Sealed
Trailer (Hub End)	2 (min)	Empty	Sealed
	2 (min)	Empty	Unsealed

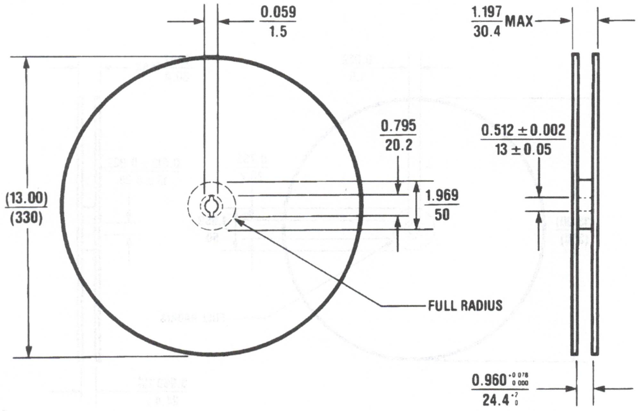
TAPE DIMENSIONS



0.157 ± 0.004
4 ± 0.1
TYP
0.061 ± 0.002
1.55 ± 0.05
TYP
0.79 ± 0.002
2 ± 0.05
TYP
(0.012)
(0.3)
0.069 ± 0.004
1.75 ± 0.1
8° MAX
0.453 ± 0.002
11.5 ± 0.05
0.945 ± 0.012
24 ± 0.3
0.530 ± 0.004
13.45 ± 0.1
@ TANGENT POINTS
0.423 ± 0.002
10.75 ± 0.05
0.081 ± 0.002
2.05 ± 0.05
0.472 ± 0.004
12 ± 0.1
0.118 ± 0.004
3 ± 0.1
0.435 ± 0.004
11.05 ± 0.1
@ TANGENT POINTS
8° MAX
(0.118)
(3)
0.012
0.3
(1.969)
(50)
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352-16

REEL DIMENSIONS



0.059
1.5
1.197
30.4
MAX
0.795
20.2
0.512 ± 0.002
13 ± 0.05
1.969
50
(13.00)
(330)
FULL RADIUS
0.960 +0.078 −0.000
24.4 +2 −0

TL/HH/8352-17

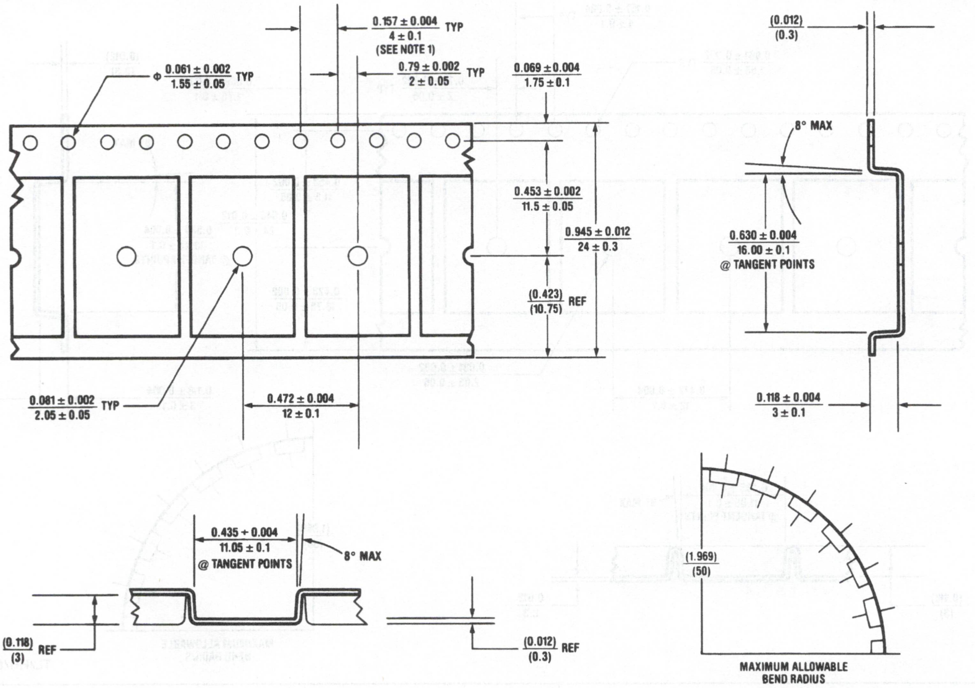
SO-24 (Wide)

TAPE FORMAT

Direction of Feed ↑

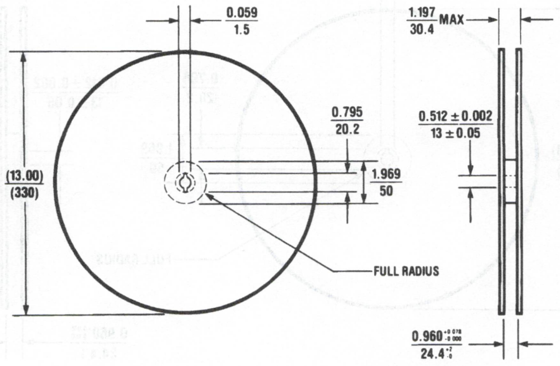
Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	5 (min)	Empty	Unsealed
	5 (min)	Empty	Sealed
Carrier	1000	Filled	Sealed
Trailer (Hub End)	2 (min)	Empty	Sealed
	2 (min)	Empty	Unsealed

TAPE DIMENSIONS


0.157 ± 0.004 / 4 ± 0.1 TYP (SEE NOTE 1)
Φ 0.061 ± 0.002 / 1.55 ± 0.05 TYP
0.79 ± 0.002 / 2 ± 0.05 TYP
0.069 ± 0.004 / 1.75 ± 0.1
(0.012) / (0.3)
8° MAX
0.453 ± 0.002 / 11.5 ± 0.05
0.945 ± 0.012 / 24 ± 0.3
0.630 ± 0.004 / 16.00 ± 0.1 @ TANGENT POINTS
(0.423) / (10.75) REF
0.081 ± 0.002 / 2.05 ± 0.05 TYP
0.472 ± 0.004 / 12 ± 0.1
0.118 ± 0.004 / 3 ± 0.1
0.435 + 0.004 / 11.05 ± 0.1 @ TANGENT POINTS
8° MAX
(0.118) / (3) REF
(0.012) / (0.3) REF
(1.969) / (50)
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352-18

REEL DIMENSIONS


0.059 / 1.5
1.197 / 30.4 MAX
0.795 / 20.2
0.512 ± 0.002 / 13 ± 0.05
(13.00) / (330)
1.969 / 50
FULL RADIUS
0.960 +0.078 -0.000 / 24.4 +2 -0

TL/HH/8352-19

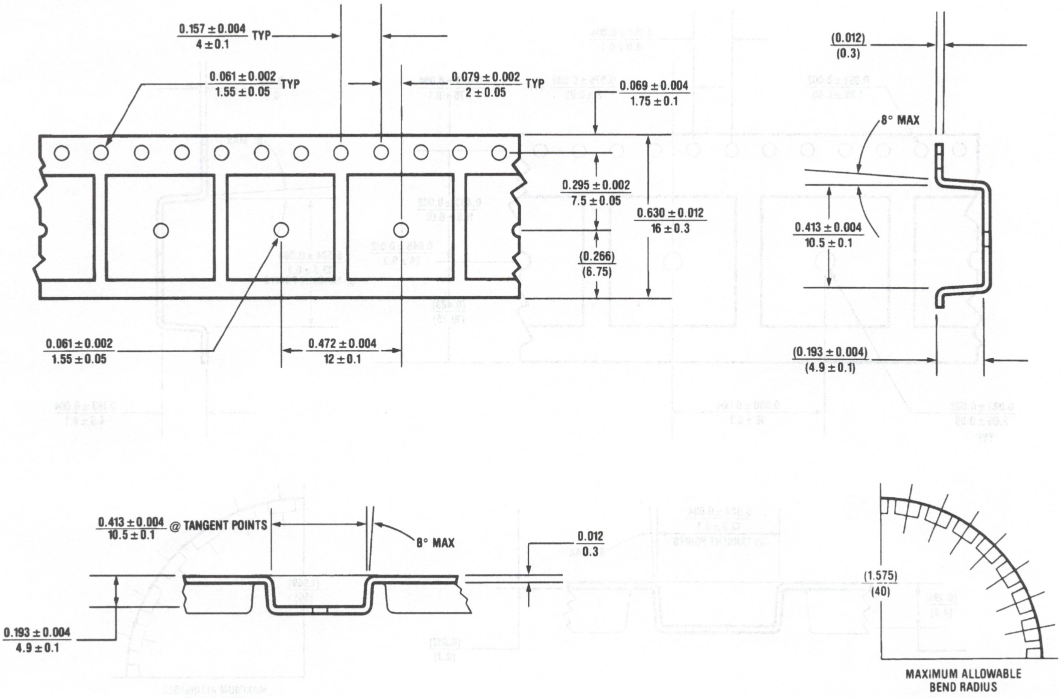
PLCC-20

TAPE FORMAT

Direction of Feed ↑

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	5 (min)	Empty	Unsealed
	5 (min)	Empty	Sealed
Carrier	1000	Filled	Sealed
Trailer (Hub End)	2 (min)	Empty	Sealed
	2 (min)	Empty	Unsealed

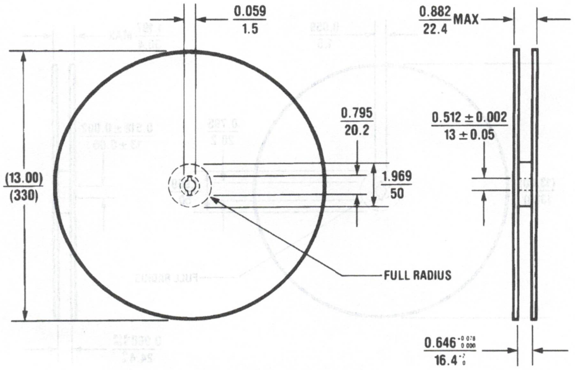
TAPE DIMENSIONS



0.157 ± 0.004 / 4 ± 0.1 TYP
0.061 ± 0.002 / 1.55 ± 0.05 TYP
0.079 ± 0.002 / 2 ± 0.05 TYP
0.069 ± 0.004 / 1.75 ± 0.1
0.295 ± 0.002 / 7.5 ± 0.05
0.630 ± 0.012 / 16 ± 0.3
(0.266) / (6.75)
0.061 ± 0.002 / 1.55 ± 0.05
0.472 ± 0.004 / 12 ± 0.1
(0.012) / (0.3)
8° MAX
0.413 ± 0.004 / 10.5 ± 0.1
(0.193 ± 0.004) / (4.9 ± 0.1)
0.413 ± 0.004 / 10.5 ± 0.1 @ TANGENT POINTS
8° MAX
0.012 / 0.3
0.193 ± 0.004 / 4.9 ± 0.1
(1.575) / (40)
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352-20

REEL DIMENSIONS



0.059 / 1.5
0.882 / 22.4 MAX
0.795 / 20.2
0.512 ± 0.002 / 13 ± 0.05
(13.00) / (330)
1.969 / 50
FULL RADIUS
0.646 +0.078 −0.000 / 16.4 +2 −0

TL/HH/8352-21

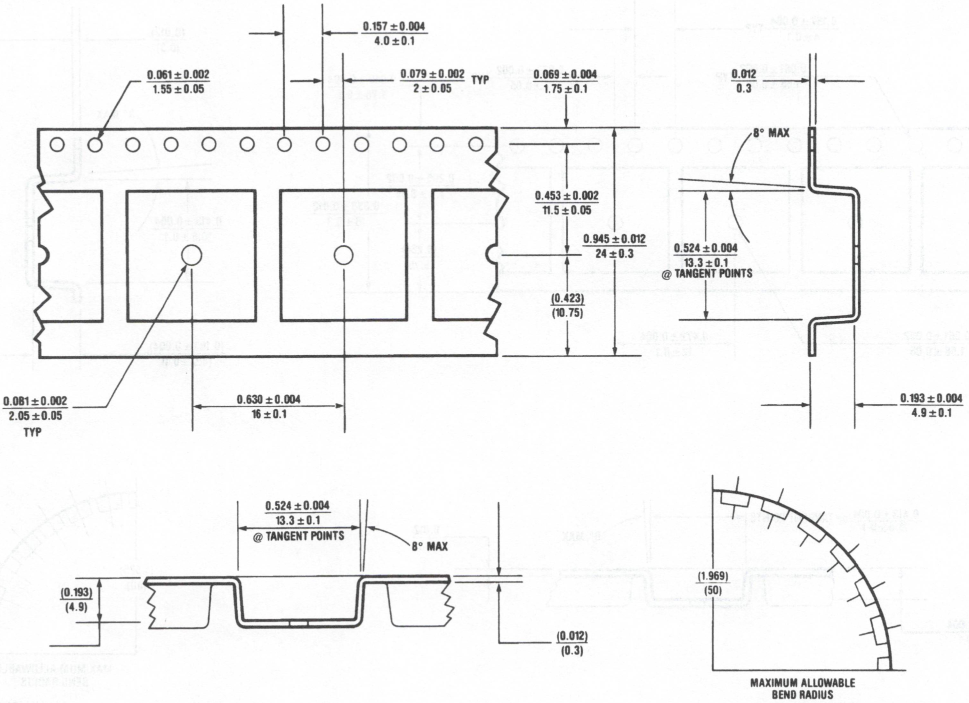
PLCC-28

TAPE FORMAT

Direction of Feed ↑

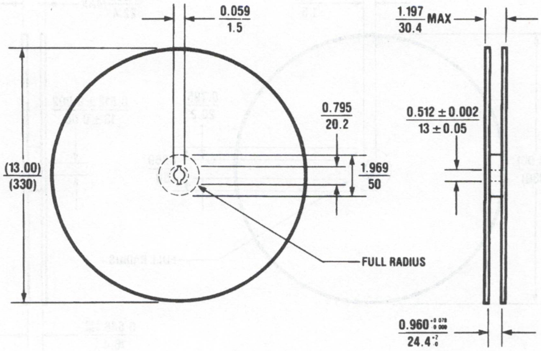
Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	5 (min)	Empty	Unsealed
	5 (min)	Empty	Sealed
Carrier	750	Filled	Sealed
Trailer (Hub End)	2 (min)	Empty	Sealed
	2 (min)	Empty	Unsealed

TAPE DIMENSIONS


0.157 ± 0.004 / 4.0 ± 0.1
0.061 ± 0.002 / 1.55 ± 0.05
0.079 ± 0.002 / 2 ± 0.05 TYP
0.069 ± 0.004 / 1.75 ± 0.1
0.012 / 0.3
8° MAX
0.453 ± 0.002 / 11.5 ± 0.05
0.945 ± 0.012 / 24 ± 0.3
0.524 ± 0.004 / 13.3 ± 0.1 @ TANGENT POINTS
(0.423) / (10.75)
0.081 ± 0.002 / 2.05 ± 0.05 TYP
0.630 ± 0.004 / 16 ± 0.1
0.193 ± 0.004 / 4.9 ± 0.1
0.524 ± 0.004 / 13.3 ± 0.1 @ TANGENT POINTS
8° MAX
(0.193) / (4.9)
(0.012) / (0.3)
(1.969) / (50)
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352-22

REEL DIMENSIONS


0.059 / 1.5
1.197 / 30.4 MAX
0.795 / 20.2
0.512 ± 0.002 / 13 ± 0.05
(13.00) / (330)
1.969 / 50
FULL RADIUS
0.960 +0.078 -0.000 / 24.4 +2 -0

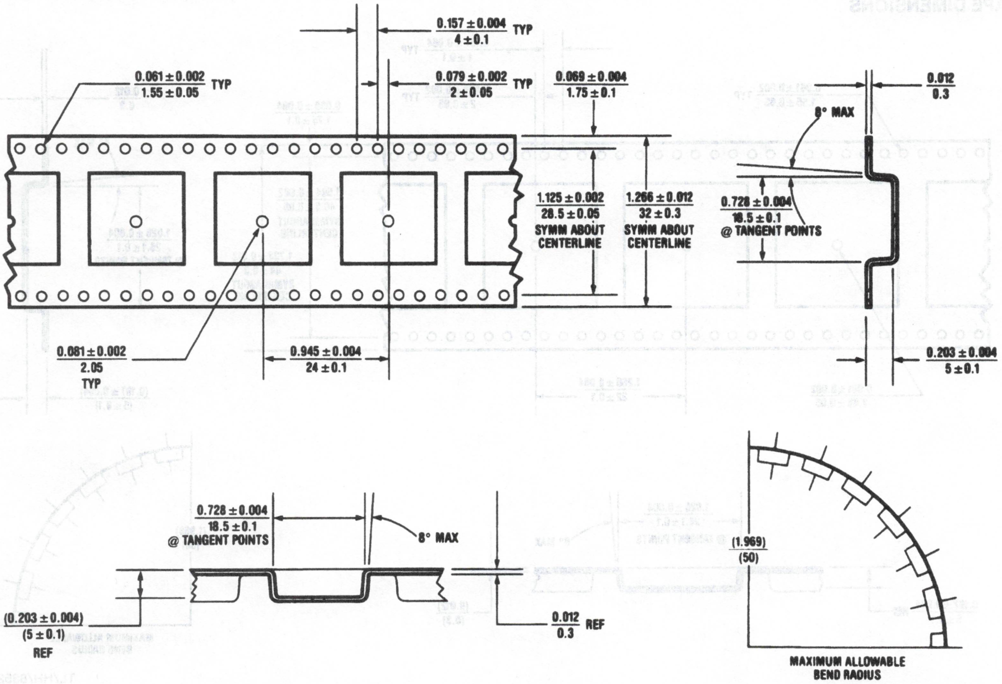
TL/HH/8352-23

PLCC-44

Direction
of ↑
Feed

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	5 (min)	Empty	Unsealed
	5 (min)	Empty	Sealed
Carrier	500	Filled	Sealed
Trailer (Hub End)	2 (min)	Empty	Sealed
	2 (min)	Empty	Unsealed

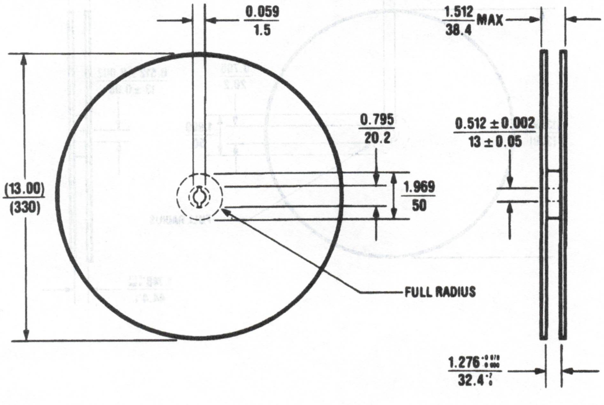
TAPE DIMENSIONS



0.157 ± 0.004 / 4 ± 0.1 TYP
0.061 ± 0.002 / 1.55 ± 0.05 TYP
0.079 ± 0.002 / 2 ± 0.05 TYP
0.069 ± 0.004 / 1.75 ± 0.1
0.012 / 0.3
8° MAX
1.125 ± 0.002 / 28.5 ± 0.05 SYMM ABOUT CENTERLINE
1.266 ± 0.012 / 32 ± 0.3 SYMM ABOUT CENTERLINE
0.728 ± 0.004 / 18.5 ± 0.1 @ TANGENT POINTS
0.081 ± 0.002 / 2.05 TYP
0.945 ± 0.004 / 24 ± 0.1
0.203 ± 0.004 / 5 ± 0.1
0.728 ± 0.004 / 18.5 ± 0.1 @ TANGENT POINTS
8° MAX
(0.203 ± 0.004) / (5 ± 0.1) REF
0.012 / 0.3 REF
(1.969) / (50)
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352-24

REEL DIMENSIONS



0.059 / 1.5
1.512 / 38.4 MAX
0.795 / 20.2
0.512 ± 0.002 / 13 ± 0.05
(13.00) / (330)
1.969 / 50
FULL RADIUS
$1.276^{+0.078}_{-0.000}$ / 32.4^{+2}_{-0}

TL/HH/8352-25

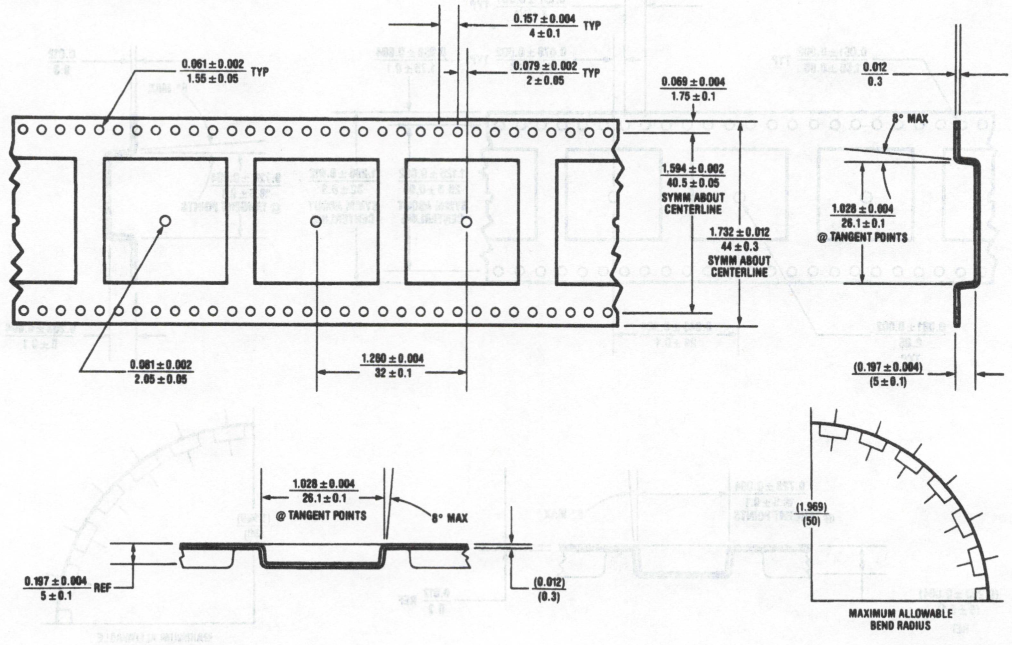
PLCC-68

TAPE FORMAT

Direction of Feed ↑

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	5 (min)	Empty	Unsealed
	5 (min)	Empty	Sealed
Carrier	250	Filled	Sealed
Trailer (Hub End)	2 (min)	Empty	Sealed
	2 (min)	Empty	Unsealed

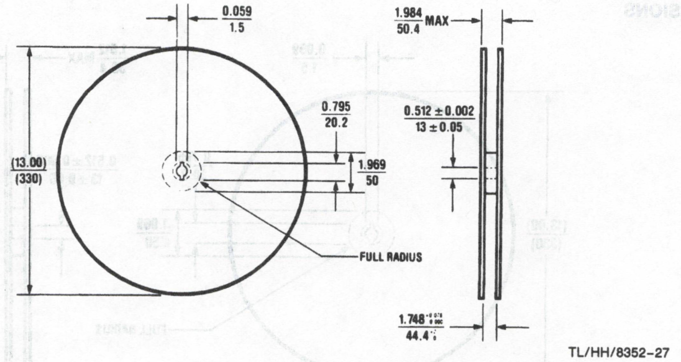
TAPE DIMENSIONS



0.157 ± 0.004 / 4 ± 0.1 TYP
0.061 ± 0.002 / 1.55 ± 0.05 TYP
0.079 ± 0.002 / 2 ± 0.05 TYP
0.069 ± 0.004 / 1.75 ± 0.1
0.012 / 0.3
8° MAX
1.594 ± 0.002 / 40.5 ± 0.05 SYMM ABOUT CENTERLINE
1.732 ± 0.012 / 44 ± 0.3 SYMM ABOUT CENTERLINE
1.028 ± 0.004 / 26.1 ± 0.1 @ TANGENT POINTS
0.061 ± 0.002 / 2.05 ± 0.05
1.260 ± 0.004 / 32 ± 0.1
(0.197 ± 0.004) / (5 ± 0.1)
1.028 ± 0.004 / 26.1 ± 0.1 @ TANGENT POINTS
8° MAX
0.197 ± 0.004 / 5 ± 0.1 REF
(0.012) / (0.3)
(1.969) / (50)
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352-26

REEL DIMENSIONS



0.059 / 1.5
1.984 / 50.4 MAX
(13.00) / (330)
0.795 / 20.2
0.512 ± 0.002 / 13 ± 0.05
1.969 / 50
FULL RADIUS
1.748 +0.078 0.000 / 44.4 +2 0

TL/HH/8352-27

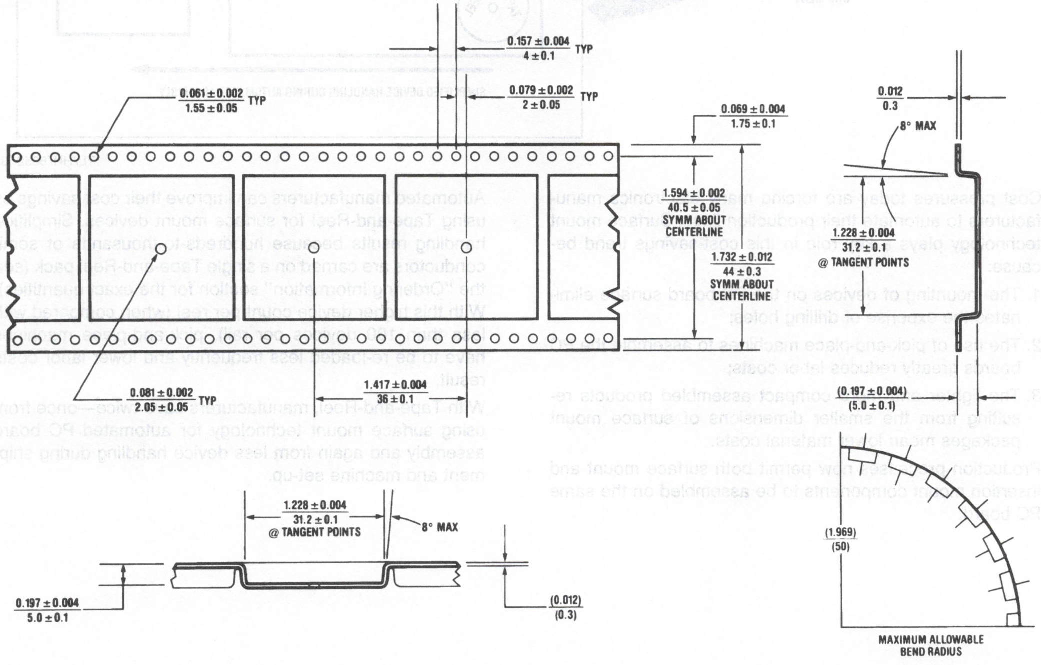
PLCC-84

TAPE FORMAT

Direction of Feed ↑

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	5 (min)	Empty	Unsealed
	5 (min)	Empty	Sealed
Carrier	250	Filled	Sealed
Trailer (Hub End)	2 (min)	Empty	Sealed
	2 (min)	Empty	Unsealed

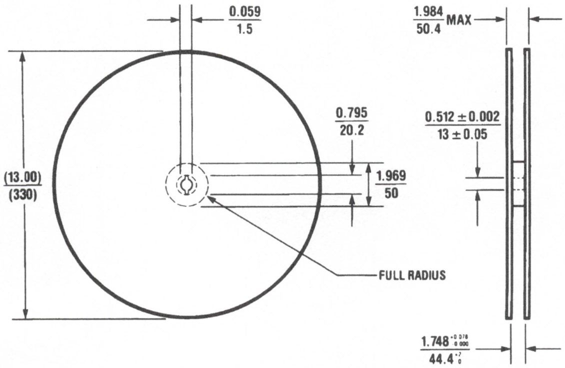
TAPE DIMENSIONS



0.157 ± 0.004 / 4 ± 0.1 TYP
0.079 ± 0.002 / 2 ± 0.05 TYP
0.061 ± 0.002 / 1.55 ± 0.05 TYP
0.069 ± 0.004 / 1.75 ± 0.1
0.012 / 0.3
8° MAX
1.594 ± 0.002 / 40.5 ± 0.05 SYMM ABOUT CENTERLINE
1.732 ± 0.012 / 44 ± 0.3 SYMM ABOUT CENTERLINE
1.228 ± 0.004 / 31.2 ± 0.1 @ TANGENT POINTS
0.081 ± 0.002 / 2.05 ± 0.05 TYP
1.417 ± 0.004 / 36 ± 0.1
(0.197 ± 0.004) / (5.0 ± 0.1)
1.228 ± 0.004 / 31.2 ± 0.1 @ TANGENT POINTS
8° MAX
0.197 ± 0.004 / 5.0 ± 0.1
(0.012) / (0.3)
(1.969) / (50)
MAXIMUM ALLOWABLE BEND RADIUS

TL/HH/8352-28

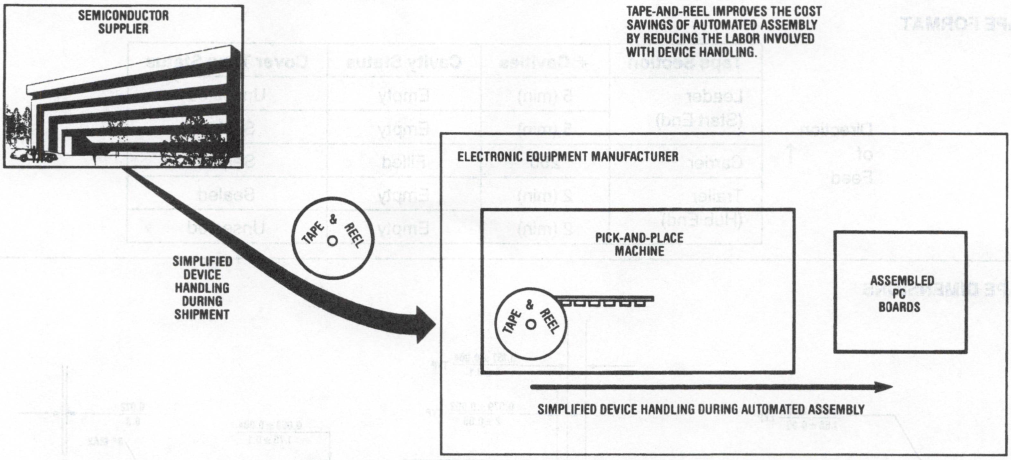
REEL DIMENSIONS



0.059 / 1.5
1.984 / 50.4 MAX
0.795 / 20.2
0.512 ± 0.002 / 13 ± 0.05
(13.00) / (330)
1.969 / 50
FULL RADIUS
1.748 +0.078 −0.000 / 44.4 +2 0

TL/HH/8352-29

Application—Total System Saving


SEMICONDUCTOR SUPPLIER
TAPE-AND-REEL IMPROVES THE COST SAVINGS OF AUTOMATED ASSEMBLY BY REDUCING THE LABOR INVOLVED WITH DEVICE HANDLING.
ELECTRONIC EQUIPMENT MANUFACTURER
TAPE & REEL
PICK-AND-PLACE MACHINE
ASSEMBLED PC BOARDS
SIMPLIFIED DEVICE HANDLING DURING SHIPMENT
TAPE & REEL
SIMPLIFIED DEVICE HANDLING DURING AUTOMATED ASSEMBLY

TL/HH/8352-32

Cost pressures today are forcing many electronics manufacturers to automate their production lines. Surface mount technology plays a key role in this cost-savings trend because:

1. The mounting of devices on the PC board surface eliminates the expense of drilling holes;
2. The use of pick-and-place machines to assemble the PC boards greatly reduces labor costs;
3. The lighter and more compact assembled products resulting from the smaller dimensions of surface mount packages mean lower material costs.

Production processes now permit both surface mount and insertion mount components to be assembled on the same PC board.

Automated manufacturers can improve their cost savings by using Tape-and-Reel for surface mount devices. Simplified handling results because hundreds-to-thousands of semiconductors are carried on a single Tape-and-Reel pack (see the "Ordering Information" section for the exact quantities). With this higher device count per reel (when compared with less than 100 devices per rail), pick-and-place machines have to be re-loaded less frequently and lower labor costs result.

With Tape-and-Reel, manufacturers save twice—once from using surface mount technology for automated PC board assembly and again from less device handling during shipment and machine set-up.

Ordering Information

When you order a surface mount semiconductor, it will be in one of the 15 available surface mount package types (see Appendix II for the physical dimensions of the surface mount packages). Specifying the Tape-and-Reel method of shipment (Note 1) means that you will receive your devices in the following quantities per Tape-and-Reel pack:

		Device Quantity	
Small Outline Transistor	SOT-23 (High Profile) (Note 2)	10000	2500*
	SOT-23 (Low Profile) (Note 2)	10000	3000*
Small Outline IC	SO-8 (Narrow)	2500	
	SO-14 (Narrow)	2500	
	SO-14 (Wide)	1000	
	SO-16 (Narrow)	2500	
	SO-16 (Wide)	1000	
	SO-20 (Wide)	1000	
	SO-24 (Wide)	1000	
Plastic Chip Carrier IC	PLCC-20	1000	
	PLCC-28	750	
	PLCC-44	500	
	PLCC-68	250	
	PLCC-84	250	

*This denotes 7″ reel quantity availability.

Note 1: For small outline transistors, your order will automatically be shipped in Tape-and-Reel unless you indicate otherwise. For surface mount integrated circuits, your order will automatically be shipped in conductive rails unless you indicate "Tape-and-Reel" after the device description on your purchase order.

Note 2: Your SOT-23 devices will automatically have Option 1 orientation unless you indicate "Option 2 Orientation" after the device description on your purchase order (see "Tape-and-Reel Overview" for definition of SOT-23 orientations). In addition, your SOT-23 devices will automatically have the high-profile outline unless you indicate "Low-Profile Outline" after the device description on your purchase order (see "Appendix II—Physical Dimensions of Surface Mount Package" for definition of SOT-23 outlines).

Example: You order 5,000 LM324M ICs shipped in Tape-and-Reel.

- All 5,000 devices have the same date code
  - You receive 2 SO-14 (Narrow) Tape-and-Reel packs, each having 2500 LM324M ICs

Appendix I—Short-Form Procurement Specification

TAPE FORMAT

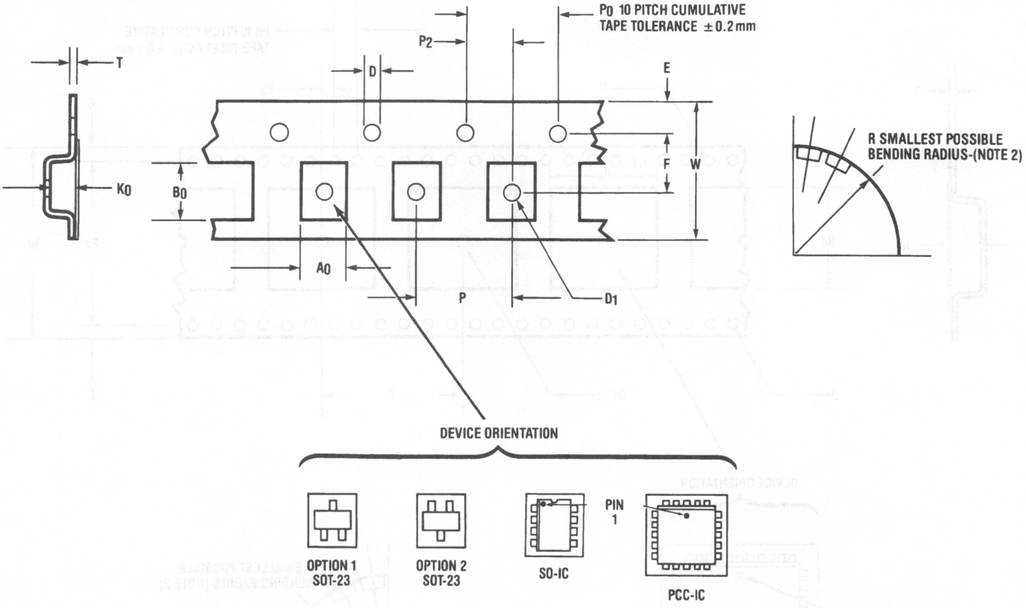
→ Direction of Feed

	Trailer (Hub End)		Carrier		Leader (Start End)	
	Empty Cavities, min (Unsealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Filled Cavities (Sealed Cover Tape)		Empty Cavities, min Sealed Cover Tape	Empty Cavities, min (Unsealed Cover Tape)
SMALL OUTLINE TRANSISTOR						
SOT-23 (High Profile)	2	2	10000	2500*	5	5
SOT-23 (Low Profile)	2	2	10000	3000*	5	5
SMALL OUTLINE IC						
SO-8 (Narrow)	2	2	2500		5	5
SO-14 (Narrow)	2	2	2500		5	5
SO-14 (Wide)	2	2	1000		5	5
SO-16 (Narrow)	2	2	2500		5	5
SO-16 (Wide)	2	2	1000		5	5
SO-20 (Wide)	2	2	1000		5	5
SO-24 (Wide)	2	2	1000		5	5
PLASTIC CHIP CARRIER IC						
PLCC-20	2	2	1000		5	5
PLCC-28	2	2	750		5	5
PLCC-44	2	2	500		5	5
PLCC-68	2	2	250		5	5
PLCC-84	2	2	250		5	5

*This denotes 7″ reel quantity availability.

Appendix I—Short-Form Procurement Specification (Continued)

TAPE DIMENSIONS (24 Millimeter Tape or Less)


T
K0
B0
D
P2
P0 10 PITCH CUMULATIVE TAPE TOLERANCE ±0.2mm
E
F
W
A0
P
D1
R SMALLEST POSSIBLE BENDING RADIUS-(NOTE 2)
DEVICE ORIENTATION
OPTION 1 SOT-23
OPTION 2 SOT-23
SO-IC
PIN 1
PCC-IC

TL/HH/8352-33

	W	P	F	E	P_2	P_0	D	T	A_0	B_0	K_0	D_1	R
SMALL OUTLINE TRANSISTOR													
SOT-23 (High Profile)	8 ± .30	4.0 ± .10	3.5 ± .05	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	3.15 ± .05	2.55 ± .05	1.20 ± .05	1.05 ± .05	25
SOT-23 (Low Profile)	8 ± .30	4.0 ± .10	3.5 ± .05	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	3.15 ± .05	2.55 ± .05	1.20 ± .05	1.05 ± .05	25
SMALL OUTLINE IC													
SO-8 (Narrow)	12 ± .30	8.0 ± .10	5.5 ± .05	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	6.4 ± .10	5.2 ± .10	2.1 ± .10	1.55 ± .05	30
SO-14 (Narrow)	16 ± .30	8.0 ± .10	7.5 ± .10	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	6.5 ± .10	9.0 ± .10	2.1 ± .10	1.55 ± .05	40
SO-14 (Wide)	16 ± .30	12.0 ± .10	7.5 ± .10	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	10.9 ± .10	9.5 ± .10	3.0 ± .10	1.55 ± .05	40
SO-16 (Narrow)	16 ± .30	8.0 ± .10	7.5 ± .10	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	6.5 ± .10	10.3 ± .10	2.1 ± .10	1.55 ± .05	40
SO-16 (Wide)	16 ± .30	12.0 ± .10	5.5 ± .10	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	10.9 ± .10	10.76 ± .10	3.0 ± .10	1.55 ± .05	40
SO-20 (Wide)	24 ± .30	12.0 ± .10	11.5 ± .10	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	10.9 ± .10	13.3 ± .10	3.0 ± .10	2.05 ± .05	50
SO-24 (Wide)	24 ± .30	12.0 ± .10	11.5 ± .10	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	10.9 ± .10	15.85 ± .10	3.0 ± .10	2.05 ± .05	50
PLASTIC CHIP CARRIER IC													
PLCC-20	16 ± .30	12.0 ± .10	7.5 ± .10	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	9.3 ± .10	9.3 ± .10	4.9 ± .10	1.55 ± .05	40
PLCC-28	24 ± .30	16.0 ± .10	11.5 ± .10	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	13.0 ± .10	13.0 ± .10	4.9 ± .10	2.05 ± .05	50

Note 1: A_0, B_0 and K_0 dimensions are measured 0.3 mm above the inside wall of the cavity bottom.

Note 2: Tape with components shall pass around a mandril radius R without damage.

Note 3: Cavity tape material shall be PVC conductive (less than 10^5 Ω/Sq).

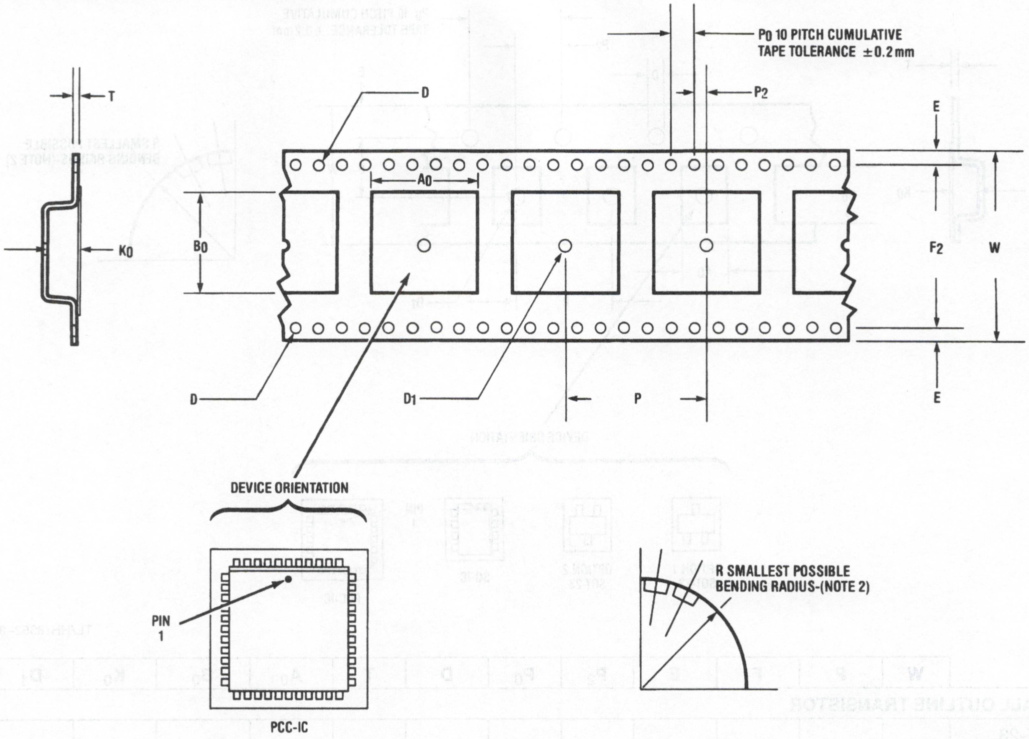
Note 4: Cover tape material shall be polyester (30–65 grams peel-back force).

Note 5: D_1 Dimension is centered within cavity.

Note 6: All dimensions are in millimeters.

Appendix I—Short-Form Procurement Specification (Continued)

TAPE DIMENSIONS (32 Millimeter Tape or Greater)


T
K0
B0
D
A0
D
D1
P0 10 PITCH CUMULATIVE TAPE TOLERANCE ±0.2mm
P2
E
F2
W
E
P
DEVICE ORIENTATION
PIN 1
PCC-IC
R SMALLEST POSSIBLE BENDING RADIUS-(NOTE 2)

TL/HH/8352-34

	W	P	F_2	E	P_2	P_0	D	T	A_0	B_0	K_0	D_1	R
PLASTIC CHIP CARRIER IC													
PLCC-44	32±.3	24.0±.1	14.25±.1	1.75±.1	2.0±.05	4.0±.1	1.55±.05	.30±.1	18.0±.1	18.0±.1	5.0±.1	2.05±.05	50
PLCC-68	44.3±.3	32.0±.1	20.25±.1	1.75±.1	2.0±.05	4.0±.1	1.55±.05	.30±.1	25.6±.1	25.6±.1	5.0±.1	2.05±.05	50
PLCC-84	44.3±.3	36.0±.1	20.25±.1	1.75±.1	2.0±.05	4.0±.1	1.55±.05	.30±.1	30.7±.1	30.7±.1	5.0±.1	2.05±.05	50

Note 1: A_0, B_0 and K_0 dimensions are measured 0.3 mm above the inside wall of the cavity bottom.

Note 2: Tape with components shall pass around a mandril radius R without damage.

Note 3: Cavity tape material shall be PVC conductive (less than 10^5 Ω/Sq).

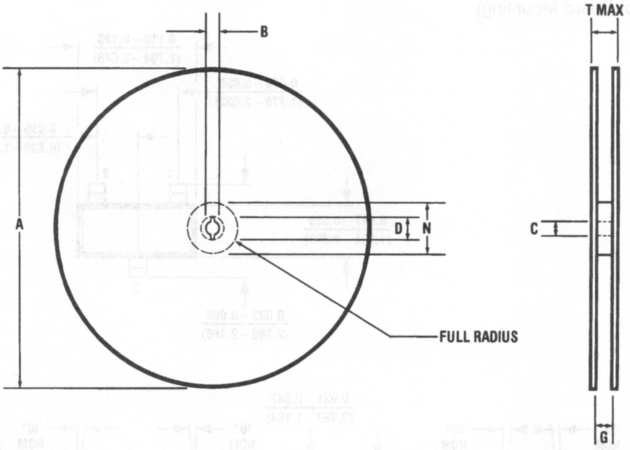
Note 4: Cover tape material shall be polyester (30–65 grams peel-back force).

Note 5: D_1 Dimension is centered within cavity.

Note 6: All dimensions are in millimeters.

Appendix I—Short-Form Procurement Specification (Continued)

REEL DIMENSIONS



TL/HH/8352-35

		A (Max)	B (Min)	C	D (Min)	N (Min)	G	T (Max)
8 mm Tape	SOT-23 (High Profile) SOT-23 (Low Profile)	(13.00) (330)	0.059 1.5	0.512 ± 0.002 13 ± 0.05	0.795 20.2	1.969 50	$0.331^{+0.059}_{-0.000}$ $8.4^{+1.5}_{-0}$	0.567 14.4
12 mm Tape	SO-8 (Narrow)	(13.00) (330)	0.059 1.5	0.512 ± 0.002 13 ± 0.05	0.795 20.2	1.969 50	$0.488^{+0.078}_{-0.000}$ 12.4^{+2}_{-0}	0.724 18.4
16 mm Tape	SO-14 (Narrow) SO-14 (Wide) SO-16 (Narrow) SO-16 (Wide) PLCC-20	(13.00) (330)	0.059 1.5	0.512 ± 0.002 13 ± 0.05	0.795 20.2	1.969 50	$0.646^{+0.078}_{-0.000}$ 16.4^{+2}_{-0}	0.882 22.4
24 mm Tape	SO-20 (Wide) SO-24 (Wide) PLCC-28	(13.00) (330)	0.059 1.5	0.512 ± 0.002 13 ± 0.05	0.795 20.2	1.969 50	$0.960^{+0.078}_{-0.000}$ 24.4^{+2}_{-0}	1.197 30.4
32 mm Tape	PLCC-44	(13.00) (330)	0.059 1.5	0.512 ± 0.002 13 ± 0.05	0.795 20.2	1.969 50	$1.276^{+0.078}_{-0.000}$ 32.4^{+2}_{-0}	1.512 38.4
44 mm Tape	PLCC-68 PLCC-84	(13.00) (330)	0.059 1.5	0.512 ± 0.002 13 ± 0.05	0.795 20.2	1.969 50	$1.748^{+0.078}_{-0.000}$ 44.4^{+2}_{-0}	1.984 50.4

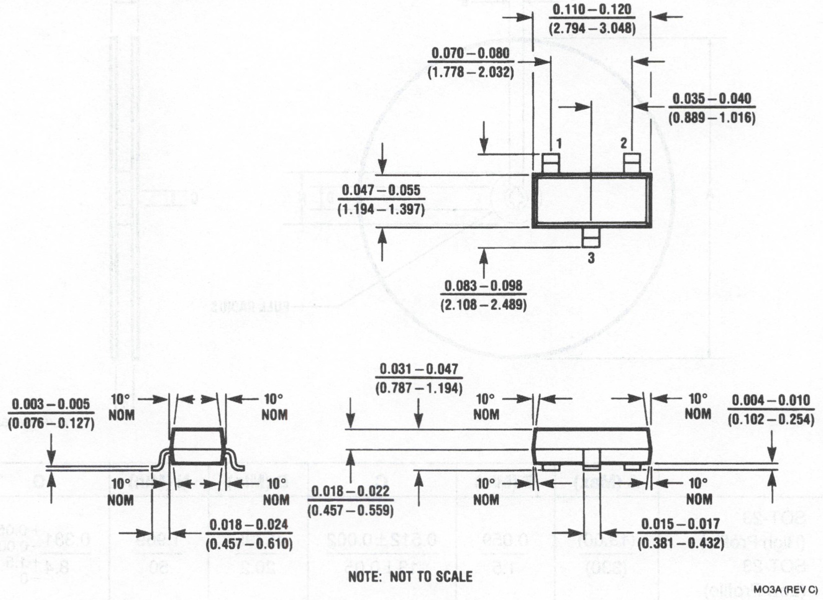
Units: $\frac{\textbf{Inches}}{\textbf{Millimeters}}$

Material: Paperboard (Non-Flaking)

Appendix II—Physical Dimensions of Surface Mount Packages

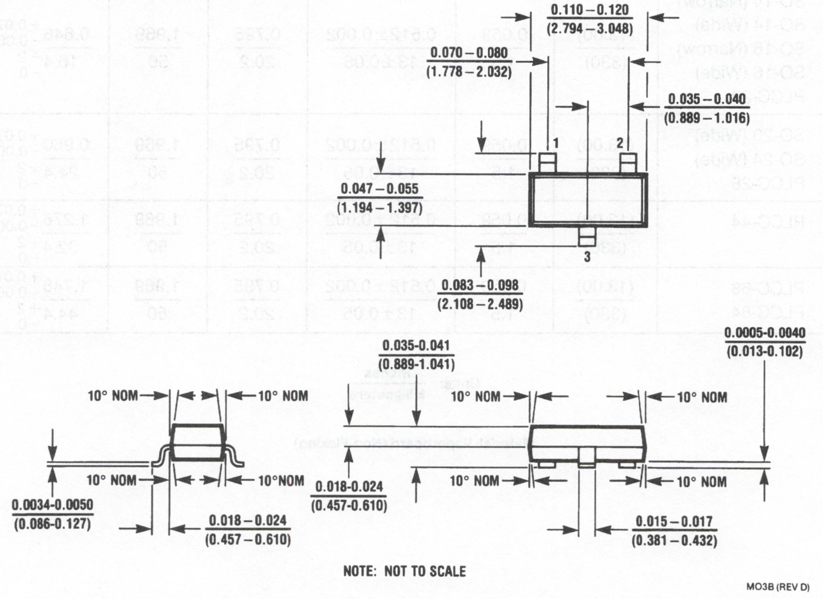
SOT-23 (High Profile)

(Generally used for Top-of-Board Mounting)


0.110 – 0.120
(2.794 – 3.048)
0.070 – 0.080
(1.778 – 2.032)
0.035 – 0.040
(0.889 – 1.016)
1
2
0.047 – 0.055
(1.194 – 1.397)
3
0.083 – 0.098
(2.108 – 2.489)
0.031 – 0.047
(0.787 – 1.194)
0.003 – 0.005
(0.076 – 0.127)
10° NOM
10° NOM
10° NOM
10° NOM
0.004 – 0.010
(0.102 – 0.254)
10° NOM
10° NOM
10° NOM
10° NOM
0.018 – 0.022
(0.457 – 0.559)
0.018 – 0.024
(0.457 – 0.610)
0.015 – 0.017
(0.381 – 0.432)
NOTE: NOT TO SCALE
MO3A (REV C)

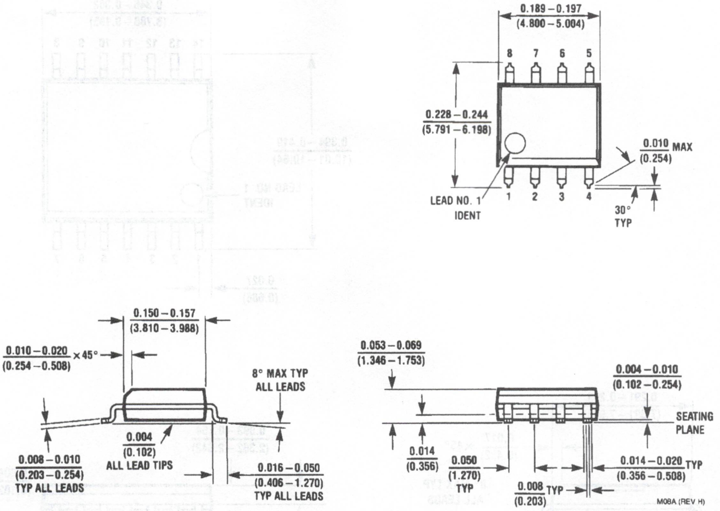
SOT-23 (Low Profile)

(Generally used for Underside-of-Board Mounting)

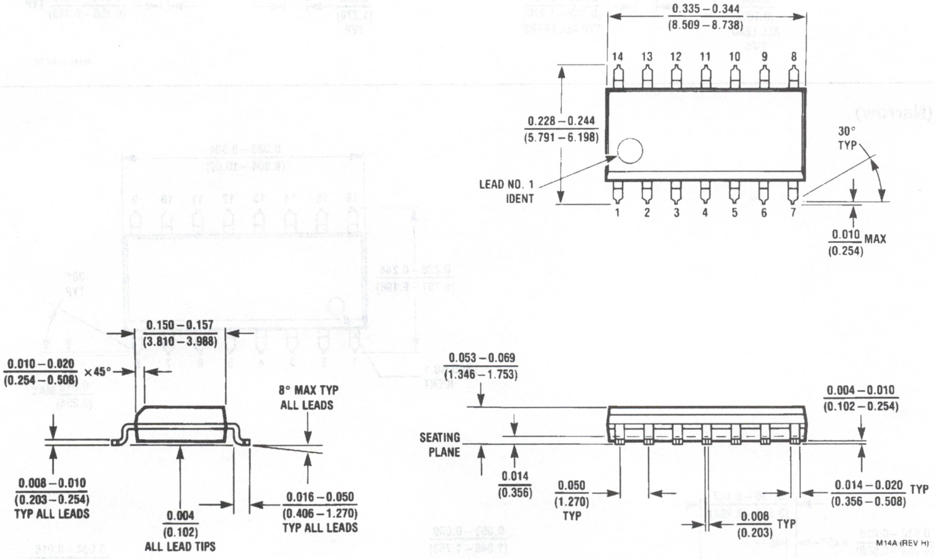

0.110 – 0.120
(2.794 – 3.048)
0.070 – 0.080
(1.778 – 2.032)
0.035 – 0.040
(0.889 – 1.016)
1
2
0.047 – 0.055
(1.194 – 1.397)
3
0.083 – 0.098
(2.108 – 2.489)
0.035-0.041
(0.889-1.041)
0.0005-0.0040
(0.013-0.102)
10° NOM
10° NOM
10° NOM
10° NOM
10° NOM
10°NOM
0.018-0.024
(0.457-0.610)
10° NOM
10° NOM
0.0034-0.0050
(0.086-0.127)
0.018 – 0.024
(0.457 – 0.610)
0.015 – 0.017
(0.381 – 0.432)
NOTE: NOT TO SCALE
MO3B (REV D)

Appendix II—Physical Dimensions of Surface Mount Packages (Continued)

SO-8 (Narrow)

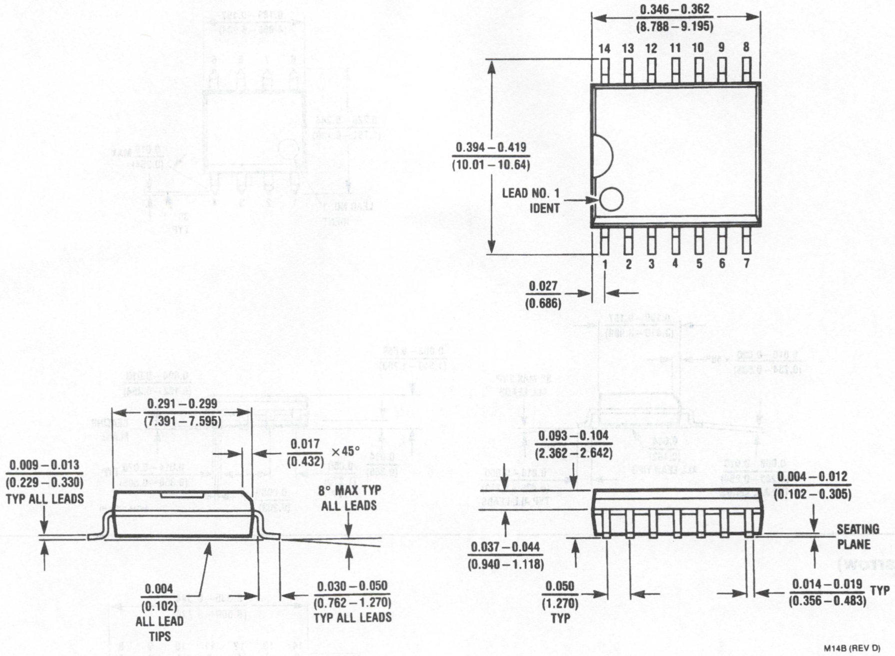

0.189 – 0.197
(4.800 – 5.004)
8 7 6 5
0.228 – 0.244
(5.791 – 6.198)
0.010 MAX
(0.254)
LEAD NO. 1
IDENT
1 2 3 4
30°
TYP
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508)
× 45°
8° MAX TYP
ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
SEATING
PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.014 – 0.020 TYP
(0.356 – 0.508)
0.008 TYP
(0.203)
M08A (REV H)

SO-14 (Narrow)

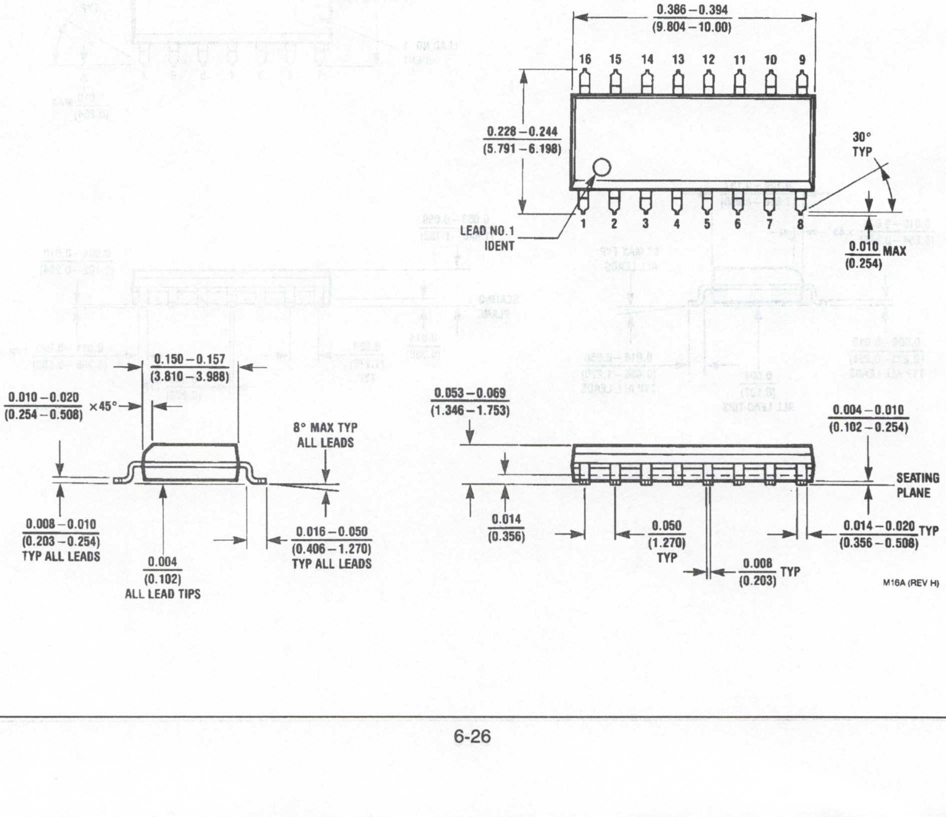

0.335 – 0.344
(8.509 – 8.738)
14 13 12 11 10 9 8
0.228 – 0.244
(5.791 – 6.198)
30°
TYP
LEAD NO. 1
IDENT
1 2 3 4 5 6 7
0.010 MAX
(0.254)
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508)
× 45°
8° MAX TYP
ALL LEADS
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
SEATING
PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.014 – 0.020 TYP
(0.356 – 0.508)
0.008 TYP
(0.203)
M14A (REV H)

Appendix II—Physical Dimensions of Surface Mount Packages (Continued)

SO-14 (Wide)

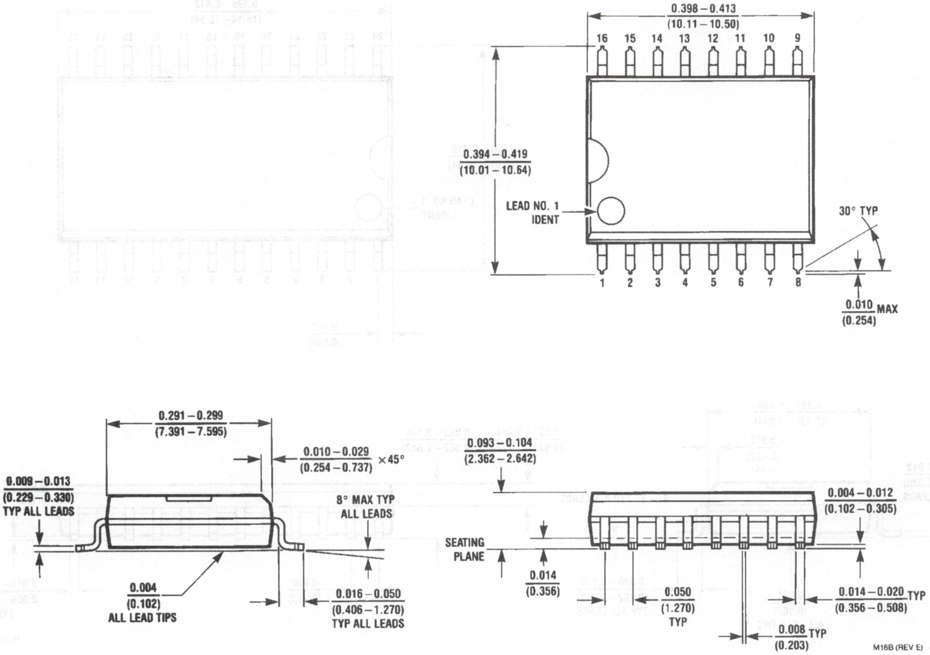

0.346 – 0.362
(8.788 – 9.195)
14 13 12 11 10 9 8
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1
IDENT
1 2 3 4 5 6 7
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.595)
0.017
(0.432)
×45°
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
8° MAX TYP
ALL LEADS
0.004
(0.102)
ALL LEAD
TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
SEATING
PLANE
0.037 – 0.044
(0.940 – 1.118)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M14B (REV D)

SO-16 (Narrow)

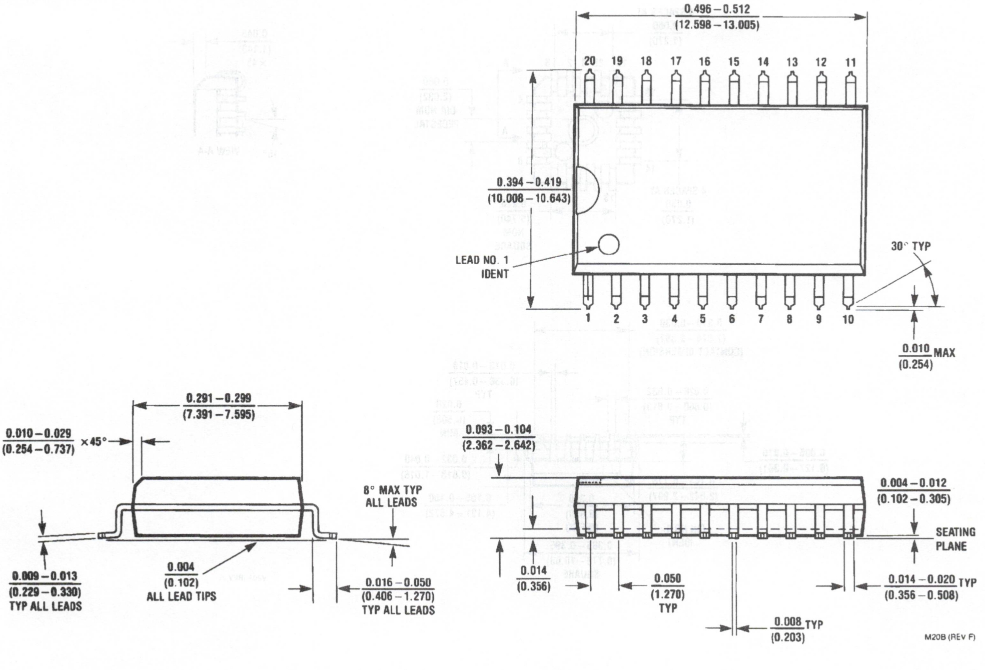

0.386 – 0.394
(9.804 – 10.00)
16 15 14 13 12 11 10 9
0.228 – 0.244
(5.791 – 6.198)
30°
TYP
1 2 3 4 5 6 7 8
LEAD NO.1
IDENT
0.010
(0.254)
MAX
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508)
×45°
8° MAX TYP
ALL LEADS
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
SEATING
PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.014 – 0.020
(0.356 – 0.508)
TYP
0.008
(0.203)
TYP
M16A (REV H)

Appendix II—Physical Dimensions of Surface Mount Packages (Continued)

SO-16 (Wide)

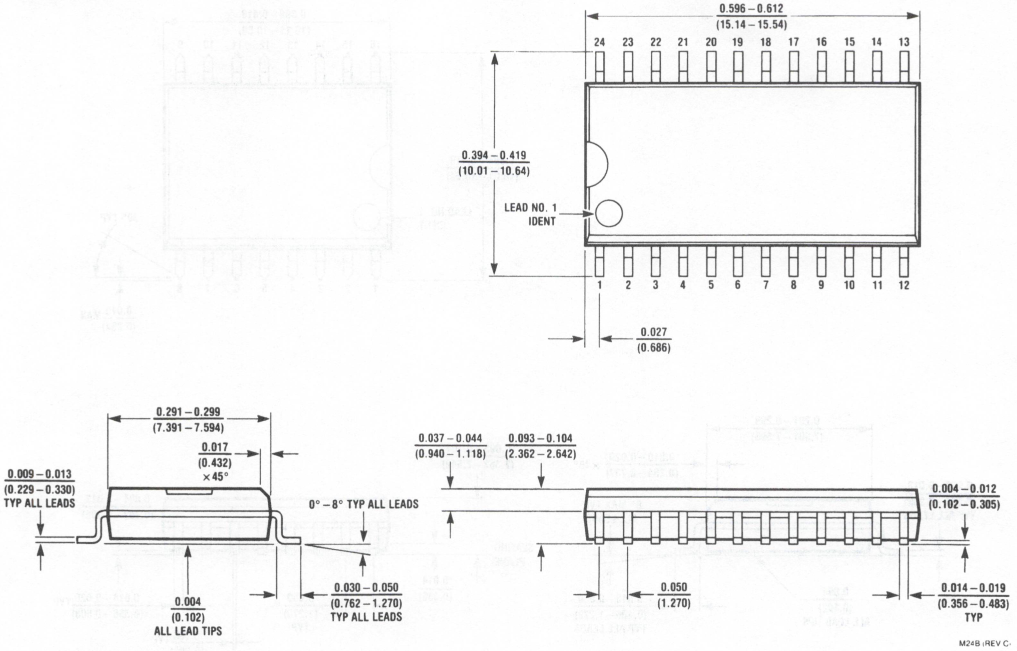

0.398 – 0.413
(10.11 – 10.50)
16 15 14 13 12 11 10 9
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1
IDENT
30° TYP
1 2 3 4 5 6 7 8
0.010 MAX
(0.254)
0.291 – 0.299
(7.391 – 7.595)
0.010 – 0.029
(0.254 – 0.737)
×45°
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
8° MAX TYP
ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
SEATING
PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.004 – 0.012
(0.102 – 0.305)
0.014 – 0.020 TYP
(0.356 – 0.508)
0.008 TYP
(0.203)
M16B (REV E)

SO-20 (Wide)

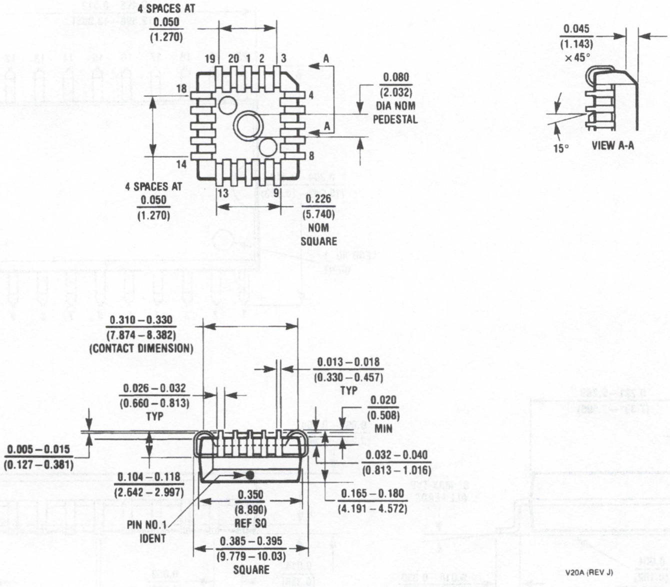

0.496 – 0.512
(12.598 – 13.005)
20 19 18 17 16 15 14 13 12 11
0.394 – 0.419
(10.008 – 10.643)
LEAD NO. 1
IDENT
30° TYP
1 2 3 4 5 6 7 8 9 10
0.010 MAX
(0.254)
0.291 – 0.299
(7.391 – 7.595)
0.010 – 0.029
(0.254 – 0.737)
×45°
8° MAX TYP
ALL LEADS
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
SEATING
PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.014 – 0.020 TYP
(0.356 – 0.508)
0.008 TYP
(0.203)
M20B (REV F)

Appendix II—Physical Dimensions of Surface Mount Packages (Continued)

SO-24 (Wide)

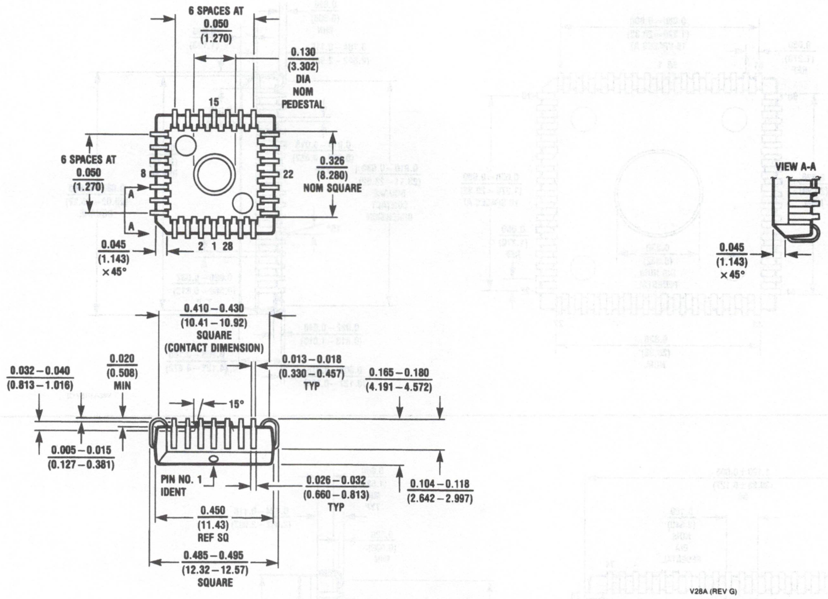

0.596 – 0.612
(15.14 – 15.54)
24 23 22 21 20 19 18 17 16 15 14 13
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1
IDENT
1 2 3 4 5 6 7 8 9 10 11 12
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.594)
0.017
(0.432)
× 45°
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
0° – 8° TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.037 – 0.044
(0.940 – 1.118)
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
0.050
(1.270)
0.014 – 0.019
(0.356 – 0.483)
TYP
M24B (REV C)

PLCC-20

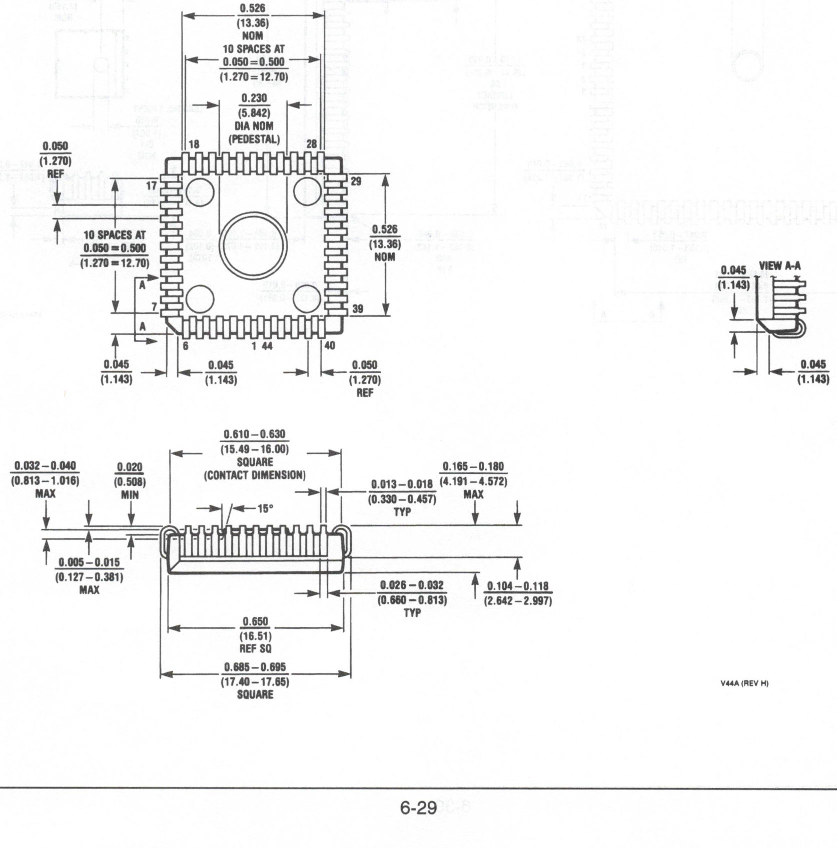

4 SPACES AT
0.050
(1.270)
19 20 1 2 3
A
18
4
0.080
(2.032)
DIA NOM
PEDESTAL
A
14
8
13
9
4 SPACES AT
0.050
(1.270)
0.226
(5.740)
NOM
SQUARE
0.045
(1.143)
× 45°
15°
VIEW A-A
0.310 – 0.330
(7.874 – 8.382)
(CONTACT DIMENSION)
0.013 – 0.018
(0.330 – 0.457)
TYP
0.026 – 0.032
(0.660 – 0.813)
TYP
0.020
(0.508)
MIN
0.005 – 0.015
(0.127 – 0.381)
0.032 – 0.040
(0.813 – 1.016)
0.104 – 0.118
(2.642 – 2.997)
0.350
(8.890)
REF SQ
0.165 – 0.180
(4.191 – 4.572)
PIN NO.1
IDENT
0.385 – 0.395
(9.779 – 10.03)
SQUARE
V20A (REV J)

Appendix II—Physical Dimensions of Surface Mount Packages (Continued)

PLCC-28

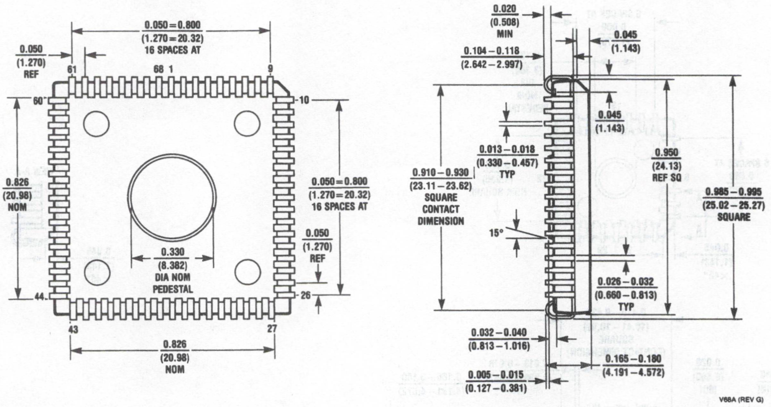

6 SPACES AT
0.050
(1.270)
0.130
(3.302)
DIA
NOM
PEDESTAL
15
6 SPACES AT
0.050
(1.270)
8
22
0.326
(8.280)
NOM SQUARE
A
A
0.045
(1.143)
×45°
2 1 28
VIEW A-A
0.045
(1.143)
×45°
0.410−0.430
(10.41−10.92)
SQUARE
(CONTACT DIMENSION)
0.032−0.040
(0.813−1.016)
0.020
(0.508)
MIN
0.013−0.018
(0.330−0.457)
TYP
0.165−0.180
(4.191−4.572)
15°
0.005−0.015
(0.127−0.381)
PIN NO. 1
IDENT
0.026−0.032
(0.660−0.813)
TYP
0.104−0.118
(2.642−2.997)
0.450
(11.43)
REF SQ
0.485−0.495
(12.32−12.57)
SQUARE
V28A (REV G)

PLCC-44

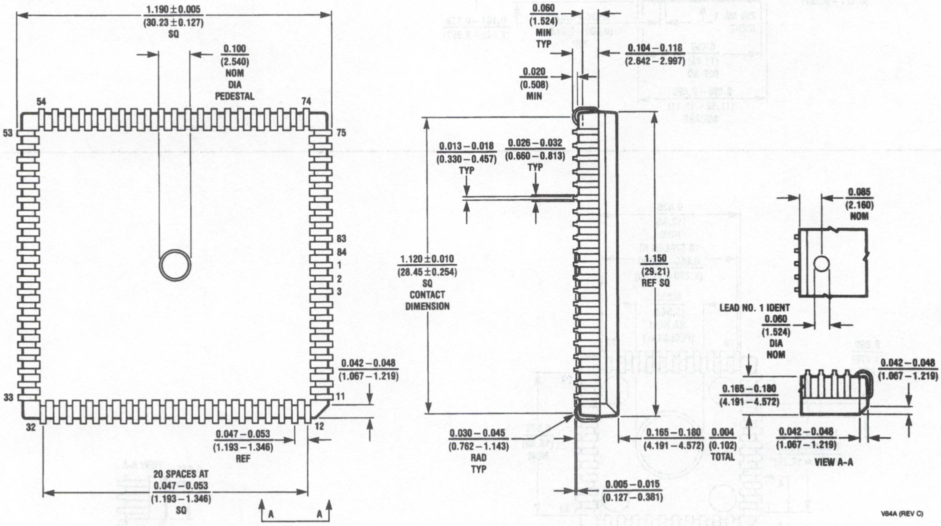

0.526
(13.36)
NOM
10 SPACES AT
0.050=0.500
(1.270=12.70)
0.230
(5.842)
DIA NOM
(PEDESTAL)
18
28
0.050
(1.270)
REF
17
29
10 SPACES AT
0.050=0.500
(1.270=12.70)
0.526
(13.36)
NOM
A
A
7
39
6
1 44
40
0.045
(1.143)
0.045
(1.143)
0.050
(1.270)
REF
VIEW A-A
0.045
(1.143)
0.045
(1.143)
0.610−0.630
(15.49−16.00)
SQUARE
(CONTACT DIMENSION)
0.032−0.040
(0.813−1.016)
MAX
0.020
(0.508)
MIN
0.013−0.018
(0.330−0.457)
TYP
0.165−0.180
(4.191−4.572)
MAX
15°
0.005−0.015
(0.127−0.381)
MAX
0.026−0.032
(0.660−0.813)
TYP
0.104−0.118
(2.642−2.997)
0.650
(16.51)
REF SQ
0.685−0.695
(17.40−17.65)
SQUARE
V44A (REV H)

Appendix II—Physical Dimensions of Surface Mount Packages (Continued)

PLCC-68


0.050=0.800
(1.270=20.32)
16 SPACES AT
0.050
(1.270)
REF
61
68 1
9
60
10
0.826
(20.98)
NOM
0.050=0.800
(1.270=20.32)
16 SPACES AT
0.050
(1.270)
REF
0.330
(8.382)
DIA NOM
PEDESTAL
44
26
43
27
0.826
(20.98)
NOM
0.020
(0.508)
MIN
0.045
(1.143)
0.104−0.118
(2.642−2.997)
0.045
(1.143)
0.013−0.018
(0.330−0.457)
TYP
0.910−0.930
(23.11−23.62)
SQUARE
CONTACT
DIMENSION
0.950
(24.13)
REF SQ
0.985−0.995
(25.02−25.27)
SQUARE
15°
0.026−0.032
(0.660−0.813)
TYP
0.032−0.040
(0.813−1.016)
0.165−0.180
(4.191−4.572)
0.005−0.015
(0.127−0.381)
V68A (REV G)

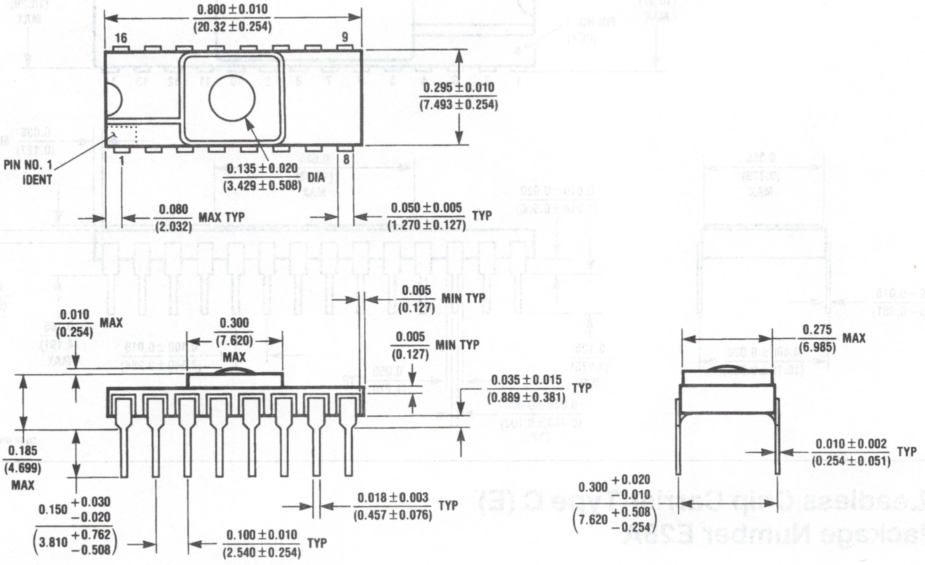
PLCC-84


1.190±0.005
(30.23±0.127)
SQ
0.100
(2.540)
NOM
DIA
PEDESTAL
54
74
53
75
83
84
1
2
3
33
11
32
12
0.042−0.048
(1.067−1.219)
0.047−0.053
(1.193−1.346)
REF
20 SPACES AT
0.047−0.053
(1.193−1.346)
SQ
A
A
0.060
(1.524)
MIN
TYP
0.104−0.118
(2.642−2.997)
0.020
(0.508)
MIN
0.013−0.018
(0.330−0.457)
TYP
0.026−0.032
(0.660−0.813)
TYP
1.120±0.010
(28.45±0.254)
SQ
CONTACT
DIMENSION
1.150
(29.21)
REF SQ
0.030−0.045
(0.762−1.143)
RAD
TYP
0.165−0.180
(4.191−4.572)
0.004
(0.102)
TOTAL
0.005−0.015
(0.127−0.381)
0.085
(2.160)
NOM
LEAD NO. 1 IDENT
0.060
(1.524)
DIA
NOM
0.165−0.180
(4.191−4.572)
0.042−0.048
(1.067−1.219)
0.042−0.048
(1.067−1.219)
VIEW A-A
V84A (REV C)

National Semiconductor

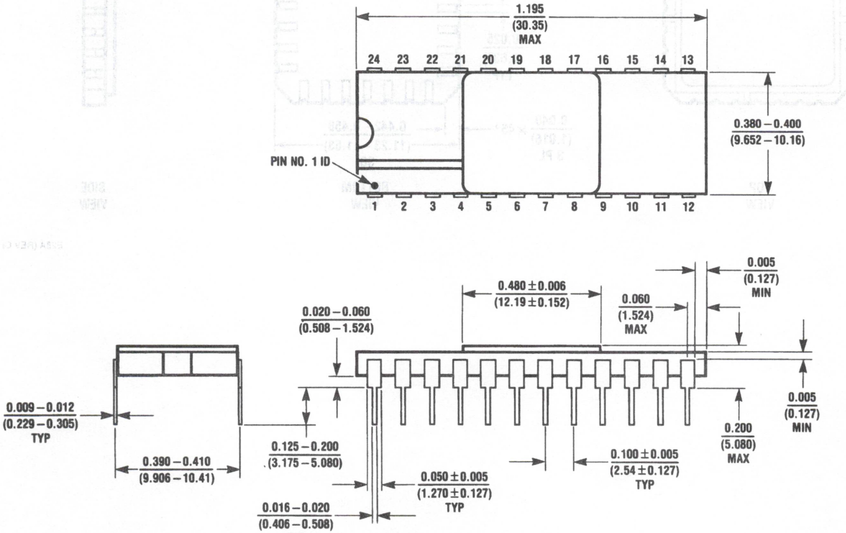
All dimensions are in inches (millimeters)

16 Lead Hermetic Dual-In-Line Package (D)
NS Package Number D16EQ


0.800 ± 0.010
(20.32 ± 0.254)
16
9
1
8
0.295 ± 0.010
(7.493 ± 0.254)
PIN NO. 1
IDENT
0.135 ± 0.020
(3.429 ± 0.508)
DIA
0.080
(2.032)
MAX TYP
0.050 ± 0.005
(1.270 ± 0.127)
TYP
0.005
(0.127)
MIN TYP
0.010
(0.254)
MAX
0.300
(7.620)
MAX
0.005
(0.127)
MIN TYP
0.035 ± 0.015
(0.889 ± 0.381)
TYP
0.275
(6.985)
MAX
0.185
(4.699)
MAX
0.010 ± 0.002
(0.254 ± 0.051)
TYP
0.300 +0.020 −0.010
(7.620 +0.508 −0.254)
0.150 +0.030 −0.020
(3.810 +0.762 −0.508)
0.018 ± 0.003
(0.457 ± 0.076)
TYP
0.100 ± 0.010
(2.540 ± 0.254)
TYP

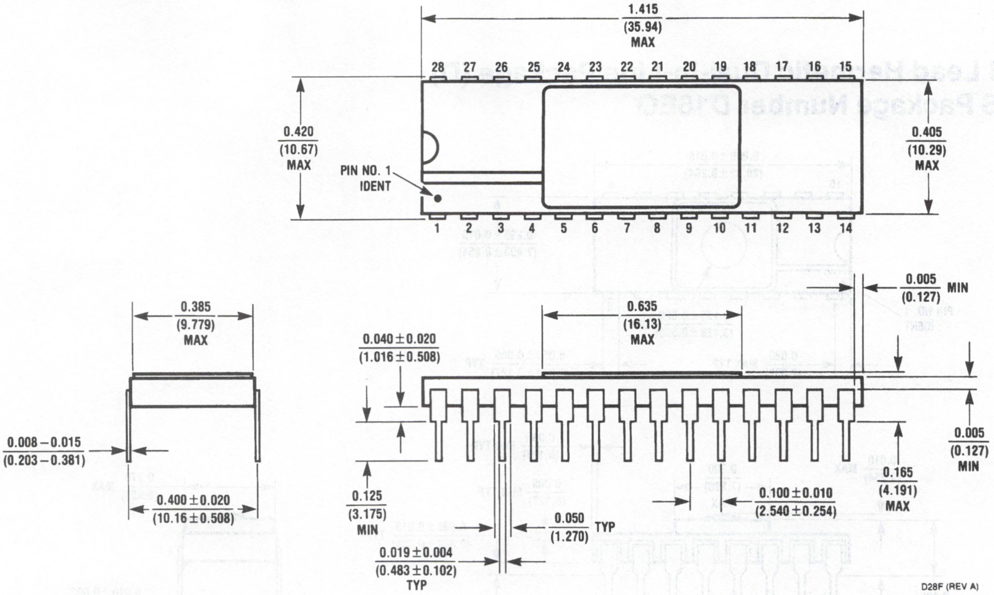
D16EQ (REV A)

24 Lead Hermetic Sidebraze Dual-In-Line Package (D)
NS Package Number D24K

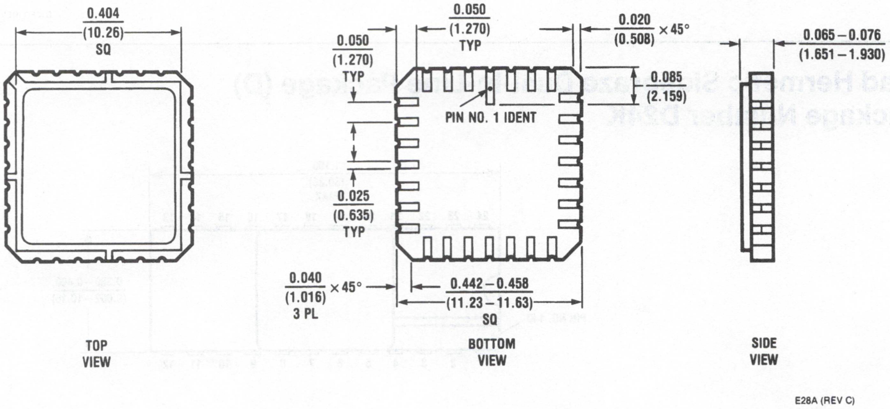

1.195
(30.35)
MAX
24
23
22
21
20
19
18
17
16
15
14
13
0.380 − 0.400
(9.652 − 10.16)
PIN NO. 1 ID
1
2
3
4
5
6
7
8
9
10
11
12
0.005
(0.127)
MIN
0.480 ± 0.006
(12.19 ± 0.152)
0.060
(1.524)
MAX
0.020 − 0.060
(0.508 − 1.524)
0.009 − 0.012
(0.229 − 0.305)
TYP
0.005
(0.127)
MIN
0.200
(5.080)
MAX
0.125 − 0.200
(3.175 − 5.080)
0.100 ± 0.005
(2.54 ± 0.127)
TYP
0.390 − 0.410
(9.906 − 10.41)
0.050 ± 0.005
(1.270 ± 0.127)
TYP
0.016 − 0.020
(0.406 − 0.508)
TYP

D24K (REV A)

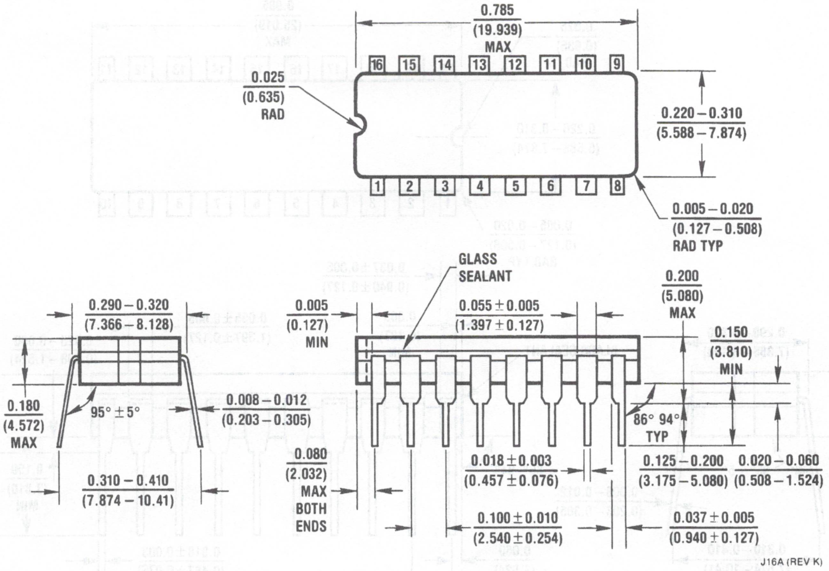
28 Lead Ceramic Sidebraze Dual-In-Line Package (D)
NS Package Number D28F


1.415
(35.94)
MAX
28 27 26 25 24 23 22 21 20 19 18 17 16 15
0.420
(10.67)
MAX
PIN NO. 1
IDENT
1 2 3 4 5 6 7 8 9 10 11 12 13 14
0.405
(10.29)
MAX
0.005
(0.127)
MIN
0.385
(9.779)
MAX
0.635
(16.13)
MAX
0.040 ± 0.020
(1.016 ± 0.508)
0.008 – 0.015
(0.203 – 0.381)
0.400 ± 0.020
(10.16 ± 0.508)
0.125
(3.175)
MIN
0.050
(1.270)
TYP
0.019 ± 0.004
(0.483 ± 0.102)
TYP
0.100 ± 0.010
(2.540 ± 0.254)
0.165
(4.191)
MAX
0.005
(0.127)
MIN
D28F (REV A)

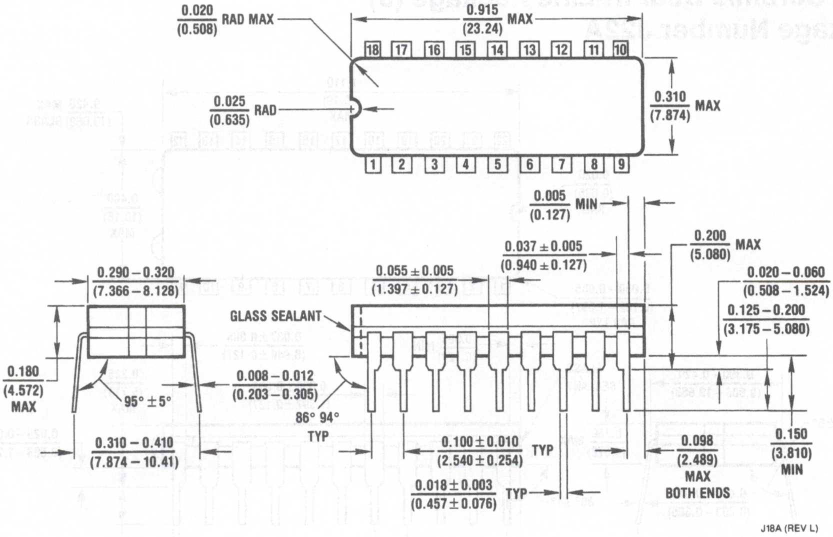
28L Leadless Chip Carrier Type C (E)
NS Package Number E28A


0.404
(10.26)
SQ
0.050
(1.270)
TYP
0.050
(1.270)
TYP
0.020
(0.508)
× 45°
0.065 – 0.076
(1.651 – 1.930)
0.085
(2.159)
PIN NO. 1 IDENT
0.025
(0.635)
TYP
0.040
(1.016)
3 PL
× 45°
0.442 – 0.458
(11.23 – 11.63)
SQ
TOP
VIEW
BOTTOM
VIEW
SIDE
VIEW
E28A (REV C)

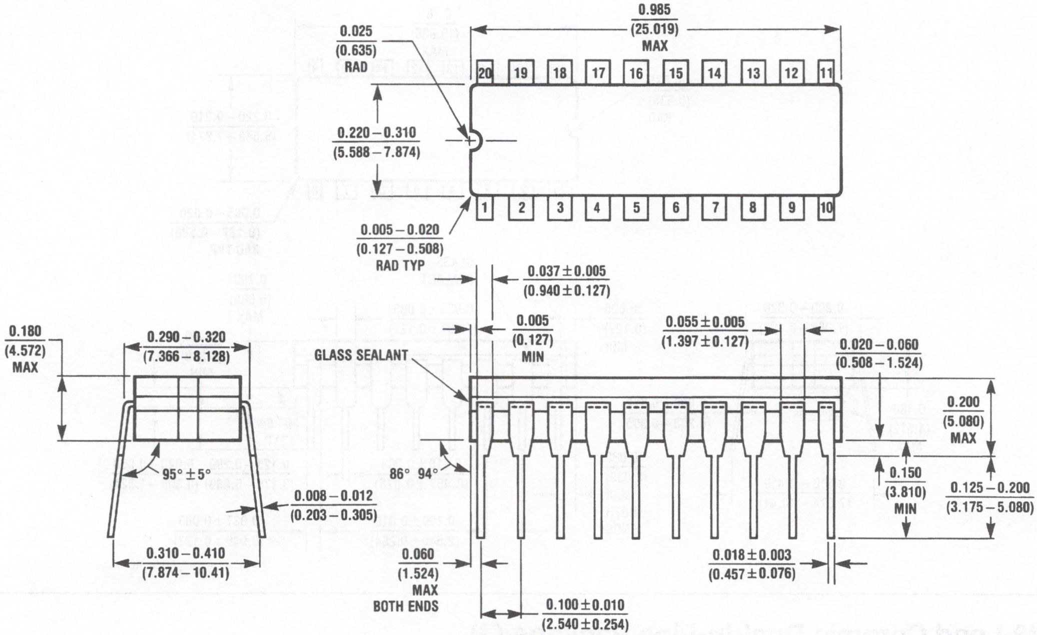
16 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J16A


0.785
(19.939)
MAX
16 15 14 13 12 11 10 9
0.025
(0.635)
RAD
0.220 – 0.310
(5.588 – 7.874)
1 2 3 4 5 6 7 8
0.005 – 0.020
(0.127 – 0.508)
RAD TYP
GLASS
SEALANT
0.200
(5.080)
MAX
0.290 – 0.320
(7.366 – 8.128)
0.005
(0.127)
MIN
0.055 ± 0.005
(1.397 ± 0.127)
0.150
(3.810)
MIN
0.180
(4.572)
MAX
95° ± 5°
0.008 – 0.012
(0.203 – 0.305)
86° 94°
TYP
0.080
(2.032)
MAX
BOTH
ENDS
0.018 ± 0.003
(0.457 ± 0.076)
0.125 – 0.200
(3.175 – 5.080)
0.020 – 0.060
(0.508 – 1.524)
0.310 – 0.410
(7.874 – 10.41)
0.100 ± 0.010
(2.540 ± 0.254)
0.037 ± 0.005
(0.940 ± 0.127)
J16A (REV K)

18 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J18A

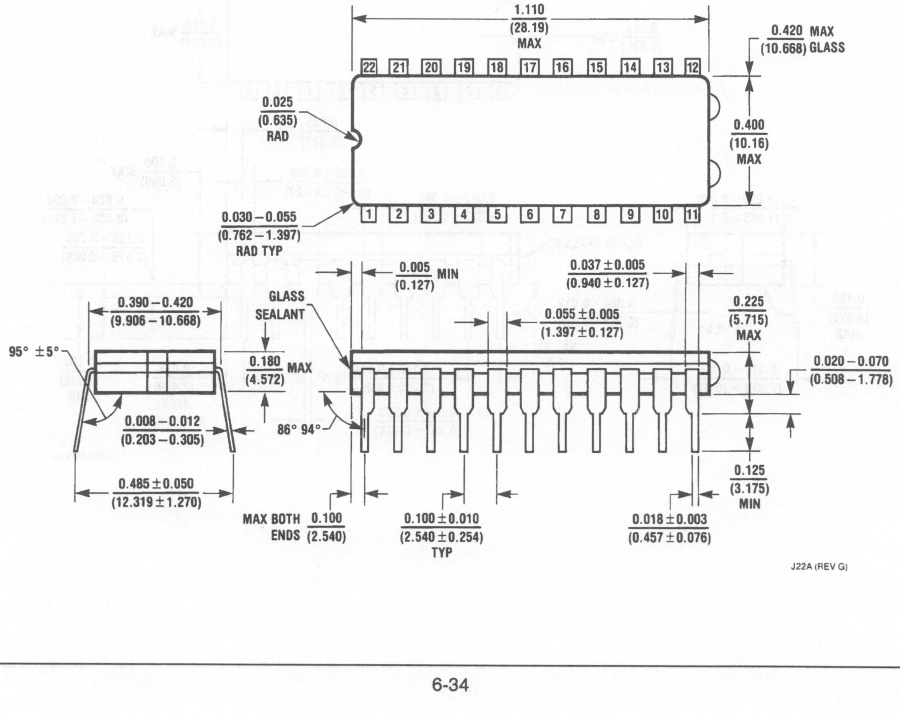

0.020
(0.508)
RAD MAX
0.915
(23.24)
MAX
18 17 16 15 14 13 12 11 10
0.025
(0.635)
RAD
0.310
(7.874)
MAX
1 2 3 4 5 6 7 8 9
0.005
(0.127)
MIN
0.200
(5.080)
MAX
0.037 ± 0.005
(0.940 ± 0.127)
0.290 – 0.320
(7.366 – 8.128)
0.055 ± 0.005
(1.397 ± 0.127)
0.020 – 0.060
(0.508 – 1.524)
0.125 – 0.200
(3.175 – 5.080)
GLASS SEALANT
0.180
(4.572)
MAX
0.008 – 0.012
(0.203 – 0.305)
95° ± 5°
86° 94°
TYP
0.310 – 0.410
(7.874 – 10.41)
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.098
(2.489)
MAX
BOTH ENDS
0.150
(3.810)
MIN
0.018 ± 0.003
(0.457 ± 0.076)
TYP
J18A (REV L)

20 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J20A


0.985 (25.019) MAX
0.025 (0.635) RAD
20
19
18
17
16
15
14
13
12
11
0.220 – 0.310 (5.588 – 7.874)
1
2
3
4
5
6
7
8
9
10
0.005 – 0.020 (0.127 – 0.508) RAD TYP
0.037 ± 0.005 (0.940 ± 0.127)
0.180 (4.572) MAX
0.290 – 0.320 (7.366 – 8.128)
GLASS SEALANT
0.005 (0.127) MIN
0.055 ± 0.005 (1.397 ± 0.127)
0.020 – 0.060 (0.508 – 1.524)
0.200 (5.080) MAX
95° ± 5°
86° 94°
0.150 (3.810) MIN
0.125 – 0.200 (3.175 – 5.080)
0.008 – 0.012 (0.203 – 0.305)
0.310 – 0.410 (7.874 – 10.41)
0.060 (1.524) MAX BOTH ENDS
0.018 ± 0.003 (0.457 ± 0.076)
0.100 ± 0.010 (2.540 ± 0.254)

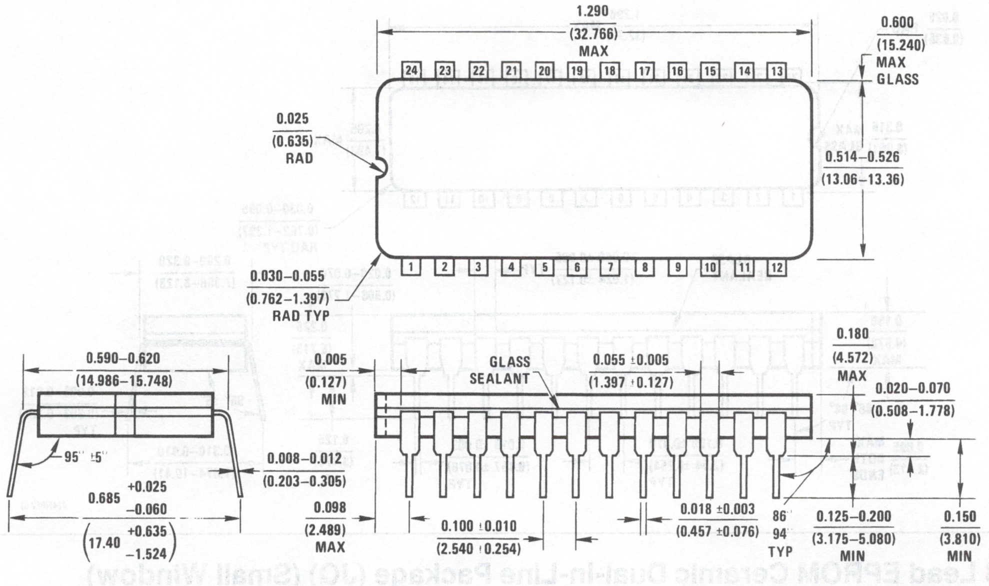
J20A (REV M)

22 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J22A


1.110 (28.19) MAX
0.420 MAX (10.668) GLASS
22
21
20
19
18
17
16
15
14
13
12
0.025 (0.635) RAD
0.400 (10.16) MAX
1
2
3
4
5
6
7
8
9
10
11
0.030 – 0.055 (0.762 – 1.397) RAD TYP
0.005 (0.127) MIN
0.037 ± 0.005 (0.940 ± 0.127)
GLASS SEALANT
0.390 – 0.420 (9.906 – 10.668)
0.055 ± 0.005 (1.397 ± 0.127)
0.225 (5.715) MAX
95° ± 5°
0.180 (4.572) MAX
0.020 – 0.070 (0.508 – 1.778)
0.008 – 0.012 (0.203 – 0.305)
86° 94°
0.125 (3.175) MIN
0.485 ± 0.050 (12.319 ± 1.270)
MAX BOTH ENDS 0.100 (2.540)
0.100 ± 0.010 (2.540 ± 0.254) TYP
0.018 ± 0.003 (0.457 ± 0.076)

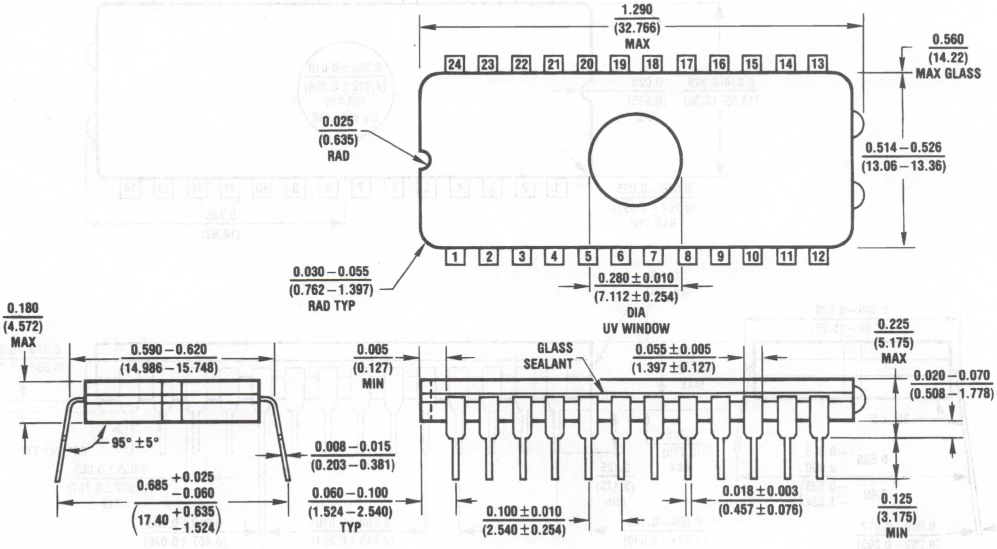
J22A (REV G)

24 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J24A

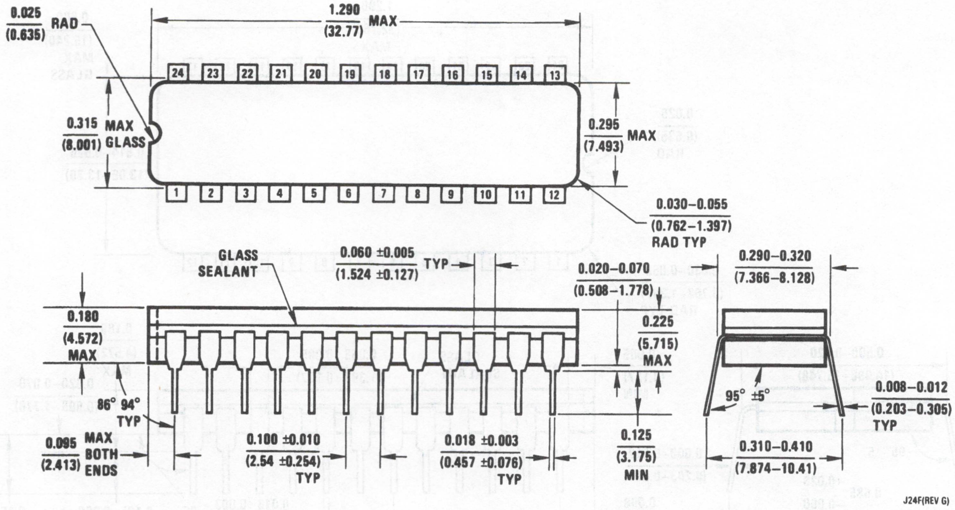

1.290
(32.766)
MAX
0.600
(15.240)
MAX
GLASS
24 23 22 21 20 19 18 17 16 15 14 13
1 2 3 4 5 6 7 8 9 10 11 12
0.025
(0.635)
RAD
0.514–0.526
(13.06–13.36)
0.030–0.055
(0.762–1.397)
RAD TYP
0.590–0.620
(14.986–15.748)
0.005
(0.127)
MIN
GLASS
SEALANT
0.055 ±0.005
(1.397 ±0.127)
0.180
(4.572)
MAX
0.020–0.070
(0.508–1.778)
95° ±5°
0.008–0.012
(0.203–0.305)
0.685 +0.025 −0.060
(17.40 +0.635 −1.524)
0.098
(2.489)
MAX
0.100 ±0.010
(2.540 ±0.254)
0.018 ±0.003
(0.457 ±0.076)
86°
94°
TYP
0.125–0.200
(3.175–5.080)
MIN
0.150
(3.810)
MIN

J24A (REV H)

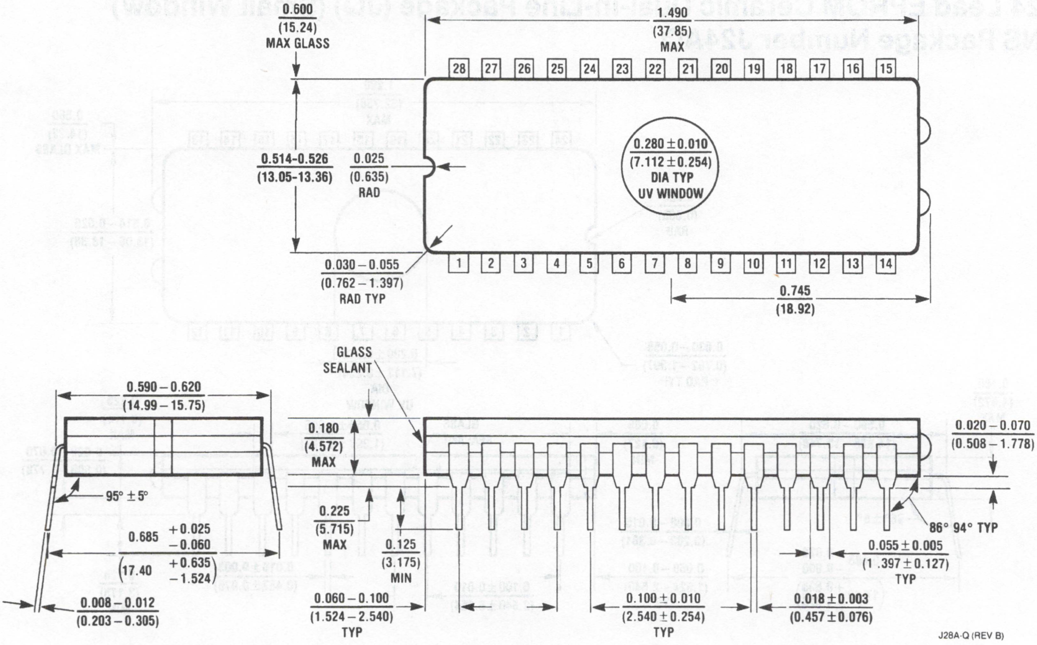
24 Lead EPROM Ceramic Dual-In-Line Package (JQ) (Small Window)
NS Package Number J24AQ


1.290
(32.766)
MAX
0.560
(14.22)
MAX GLASS
24 23 22 21 20 19 18 17 16 15 14 13
1 2 3 4 5 6 7 8 9 10 11 12
0.025
(0.635)
RAD
0.514–0.526
(13.06–13.36)
0.030–0.055
(0.762–1.397)
RAD TYP
0.280±0.010
(7.112±0.254)
DIA
UV WINDOW
0.180
(4.572)
MAX
0.590–0.620
(14.986–15.748)
0.005
(0.127)
MIN
GLASS
SEALANT
0.055±0.005
(1.397±0.127)
0.225
(5.175)
MAX
0.020–0.070
(0.508–1.778)
95°±5°
0.008–0.015
(0.203–0.381)
0.685 +0.025 −0.060
(17.40 +0.635 −1.524)
0.060–0.100
(1.524–2.540)
TYP
0.100±0.010
(2.540±0.254)
0.018±0.003
(0.457±0.076)
0.125
(3.175)
MIN

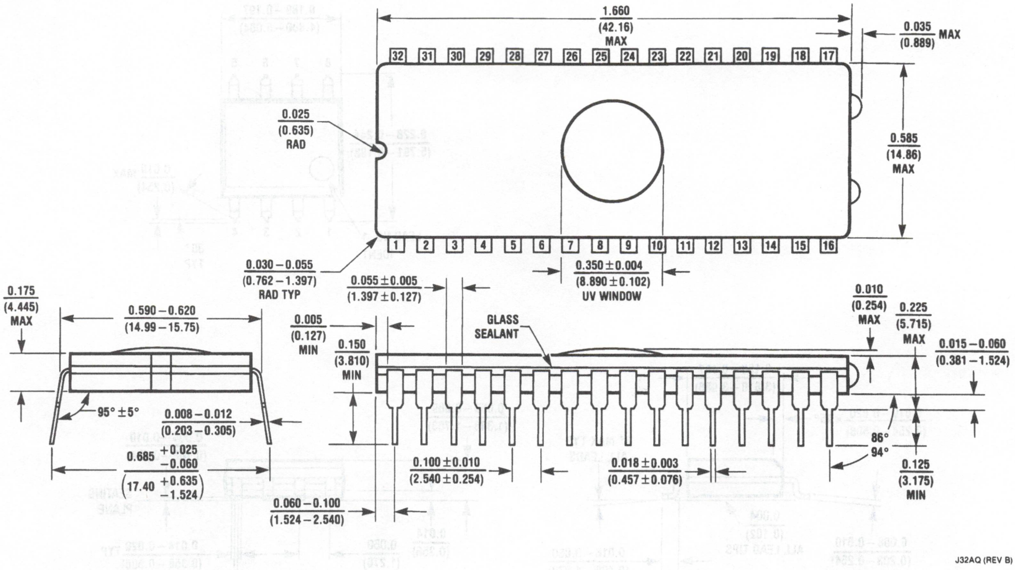
24 Lead Ceramic Dual-In-Line Package (J) NS Package Number J24F


0.025 (0.635) RAD
1.290 (32.77) MAX
24
23
22
21
20
19
18
17
16
15
14
13
0.315 (8.001) MAX GLASS
0.295 (7.493) MAX
1
2
3
4
5
6
7
8
9
10
11
12
0.030–0.055 (0.762–1.397) RAD TYP
GLASS SEALANT
0.060 ±0.005 (1.524 ±0.127) TYP
0.020–0.070 (0.508–1.778)
0.290–0.320 (7.366–8.128)
0.180 (4.572) MAX
0.225 (5.715) MAX
95° ±5°
0.008–0.012 (0.203–0.305) TYP
86° 94° TYP
0.095 (2.413) MAX BOTH ENDS
0.100 ±0.010 (2.54 ±0.254) TYP
0.018 ±0.003 (0.457 ±0.076) TYP
0.125 (3.175) MIN
0.310–0.410 (7.874–10.41)
J24F(REV G)

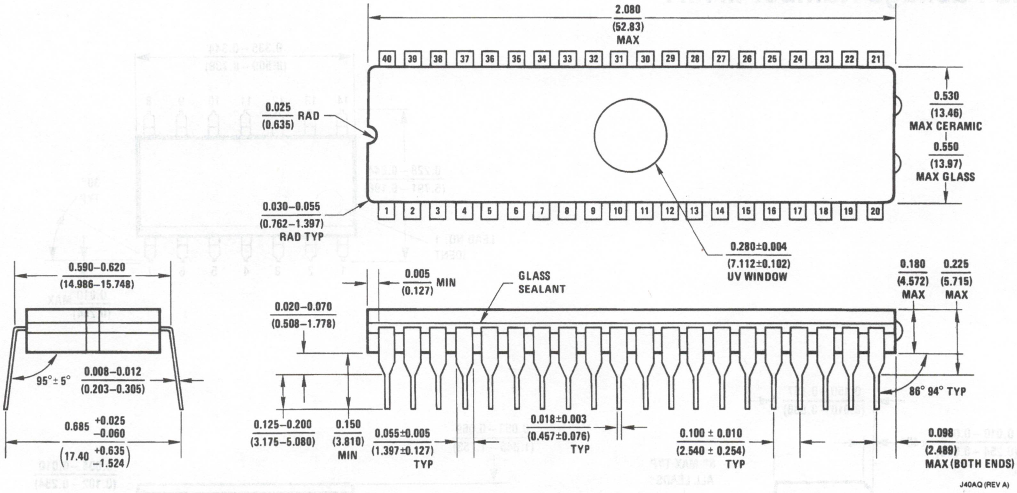
28 Lead EPROM Ceramic Dual-In-Line Package (JQ) (Small Window) NS Package Number J28AQ


0.600 (15.24) MAX GLASS
1.490 (37.85) MAX
28
27
26
25
24
23
22
21
20
19
18
17
16
15
0.280 ± 0.010 (7.112 ± 0.254) DIA TYP UV WINDOW
0.514-0.526 (13.05-13.36)
0.025 (0.635) RAD
1
2
3
4
5
6
7
8
9
10
11
12
13
14
0.030 – 0.055 (0.762 – 1.397) RAD TYP
0.745 (18.92)
GLASS SEALANT
0.590 – 0.620 (14.99 – 15.75)
95° ± 5°
0.685 +0.025 −0.060 (17.40 +0.635 −1.524)
0.008 – 0.012 (0.203 – 0.305)
0.180 (4.572) MAX
0.225 (5.715) MAX
0.125 (3.175) MIN
0.060 – 0.100 (1.524 – 2.540) TYP
0.020 – 0.070 (0.508 – 1.778)
86° 94° TYP
0.055 ± 0.005 (1.397 ± 0.127) TYP
0.100 ± 0.010 (2.540 ± 0.254) TYP
0.018 ± 0.003 (0.457 ± 0.076)
J28A-Q (REV B)

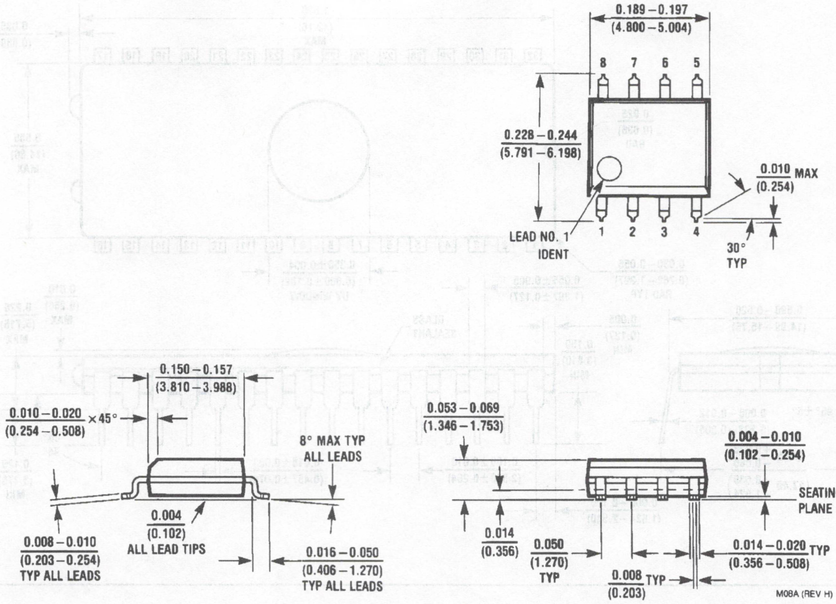
32 Lead EPROM Ceramic Dual-In-Line Package (JQ)
NS Package Number J32AQ


1.660
(42.16)
MAX
0.035
(0.889)
MAX
32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17
0.025
(0.635)
RAD
0.585
(14.86)
MAX
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
0.030 – 0.055
(0.762 – 1.397)
RAD TYP
0.055 ± 0.005
(1.397 ± 0.127)
0.350 ± 0.004
(8.890 ± 0.102)
UV WINDOW
0.175
(4.445)
MAX
0.590 – 0.620
(14.99 – 15.75)
0.005
(0.127)
MIN
0.150
(3.810)
MIN
GLASS
SEALANT
0.010
(0.254)
MAX
0.225
(5.715)
MAX
0.015 – 0.060
(0.381 – 1.524)
95° ± 5°
0.008 – 0.012
(0.203 – 0.305)
0.685 +0.025 −0.060
(17.40 +0.635 −1.524)
0.100 ± 0.010
(2.540 ± 0.254)
0.018 ± 0.003
(0.457 ± 0.076)
86°
94°
0.125
(3.175)
MIN
0.060 – 0.100
(1.524 – 2.540)
J32AQ (REV B)

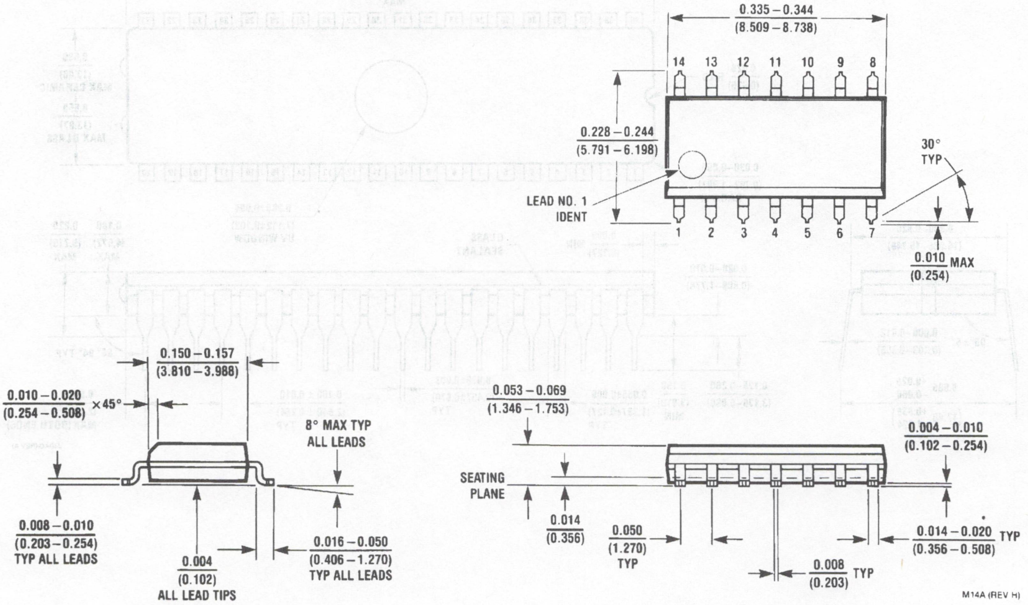
40 Lead EPROM Ceramic Dual-In-Line Package (JQ)
NS Package Number J40AQ


2.080
(52.83)
MAX
40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21
0.025
(0.635)
RAD
0.530
(13.46)
MAX CERAMIC
0.550
(13.97)
MAX GLASS
0.030–0.055
(0.762–1.397)
RAD TYP
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
0.280±0.004
(7.112±0.102)
UV WINDOW
0.590–0.620
(14.986–15.748)
0.005
(0.127)
MIN
GLASS
SEALANT
0.180
(4.572)
MAX
0.225
(5.715)
MAX
0.020–0.070
(0.508–1.778)
95° ± 5°
0.008–0.012
(0.203–0.305)
86° 94° TYP
0.685 +0.025 −0.060
(17.40 +0.635 −1.524)
0.125–0.200
(3.175–5.080)
0.150
(3.810)
MIN
0.055±0.005
(1.397±0.127)
TYP
0.018±0.003
(0.457±0.076)
TYP
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.098
(2.489)
MAX (BOTH ENDS)
J40AQ (REV A)

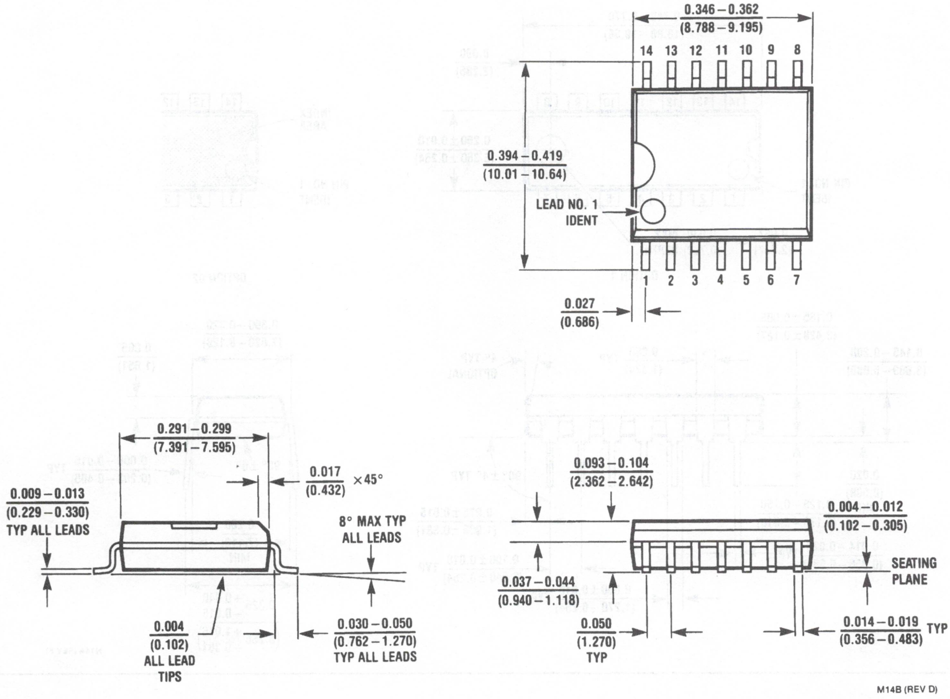
8 Lead (0.150″ Wide) Molded Small Outline Package (M)
NS Package Number M08A


0.189 – 0.197
(4.800 – 5.004)
8
7
6
5
0.228 – 0.244
(5.791 – 6.198)
0.010 MAX
(0.254)
LEAD NO. 1
IDENT
1
2
3
4
30°
TYP
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508)
× 45°
0.053 – 0.069
(1.346 – 1.753)
8° MAX TYP
ALL LEADS
0.004 – 0.010
(0.102 – 0.254)
SEATING
PLANE
0.004
(0.102)
ALL LEAD TIPS
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.014
(0.356)
0.050
(1.270)
TYP
0.014 – 0.020 TYP
(0.356 – 0.508)
0.008 TYP
(0.203)
M08A (REV H)

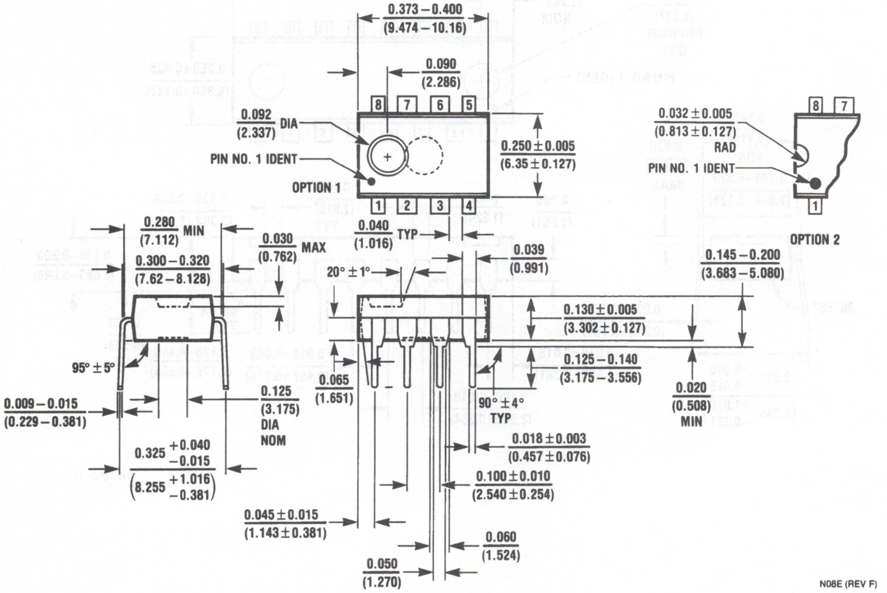
14 Lead (0.150″ Wide) Molded Small Outline Package (M)
NS Package Number M14A


0.335 – 0.344
(8.509 – 8.738)
14
13
12
11
10
9
8
0.228 – 0.244
(5.791 – 6.198)
30°
TYP
LEAD NO. 1
IDENT
1
2
3
4
5
6
7
0.010 MAX
(0.254)
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508)
× 45°
8° MAX TYP
ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
SEATING
PLANE
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.014
(0.356)
0.050
(1.270)
TYP
0.014 – 0.020 TYP
(0.356 – 0.508)
0.008 TYP
(0.203)
M14A (REV H)

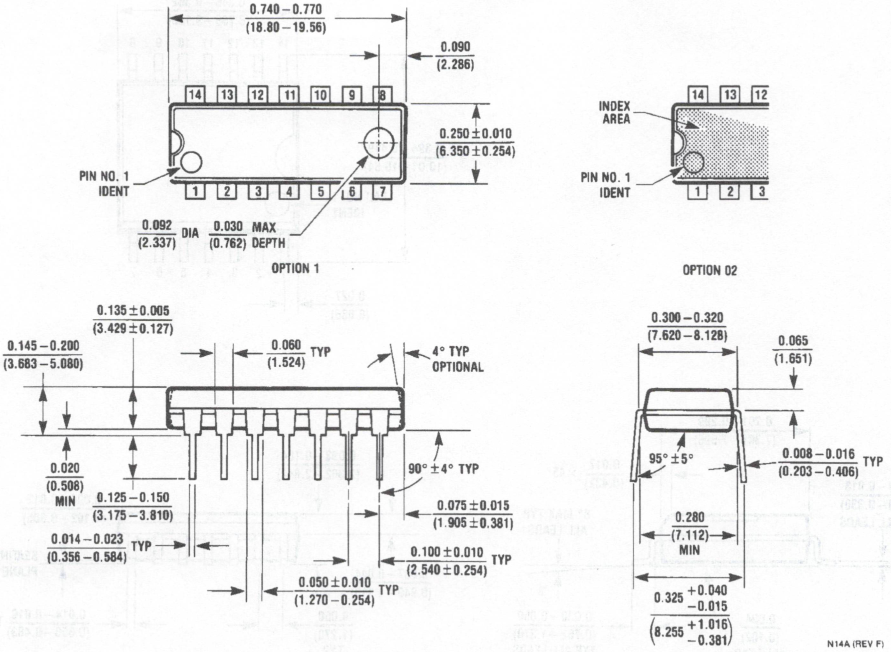
14 Lead (0.300" Wide) Molded Small Outline Package (M)
NS Package Number M14B


0.346 – 0.362
(8.788 – 9.195)
14 13 12 11 10 9 8
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1 IDENT
1 2 3 4 5 6 7
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.595)
0.017
(0.432)
× 45°
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
8° MAX TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
SEATING PLANE
0.037 – 0.044
(0.940 – 1.118)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M14B (REV D)

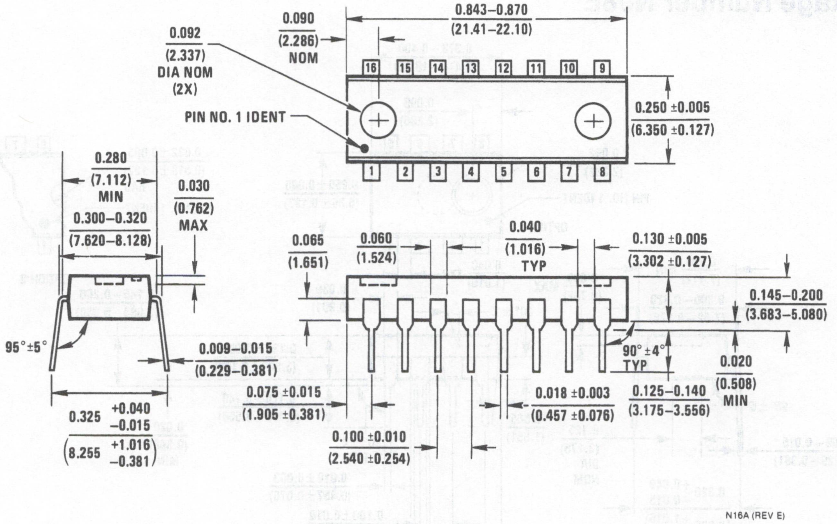
8 Lead Molded Dual-In-Line Package (N)
NS Package Number N08E


0.373 – 0.400
(9.474 – 10.16)
0.090
(2.286)
8 7 6 5
0.092
(2.337)
DIA
PIN NO. 1 IDENT
OPTION 1
1 2 3 4
0.250 ± 0.005
(6.35 ± 0.127)
0.032 ± 0.005
(0.813 ± 0.127)
RAD
PIN NO. 1 IDENT
8 7
1
OPTION 2
0.280
(7.112)
MIN
0.300 – 0.320
(7.62 – 8.128)
0.030
(0.762)
MAX
0.040
(1.016)
TYP
0.039
(0.991)
20° ± 1°
0.145 – 0.200
(3.683 – 5.080)
0.130 ± 0.005
(3.302 ± 0.127)
95° ± 5°
0.125 – 0.140
(3.175 – 3.556)
0.020
(0.508)
MIN
0.065
(1.651)
0.125
(3.175)
DIA NOM
90° ± 4°
TYP
0.009 – 0.015
(0.229 – 0.381)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)
0.045 ± 0.015
(1.143 ± 0.381)
0.060
(1.524)
0.050
(1.270)
N08E (REV F)

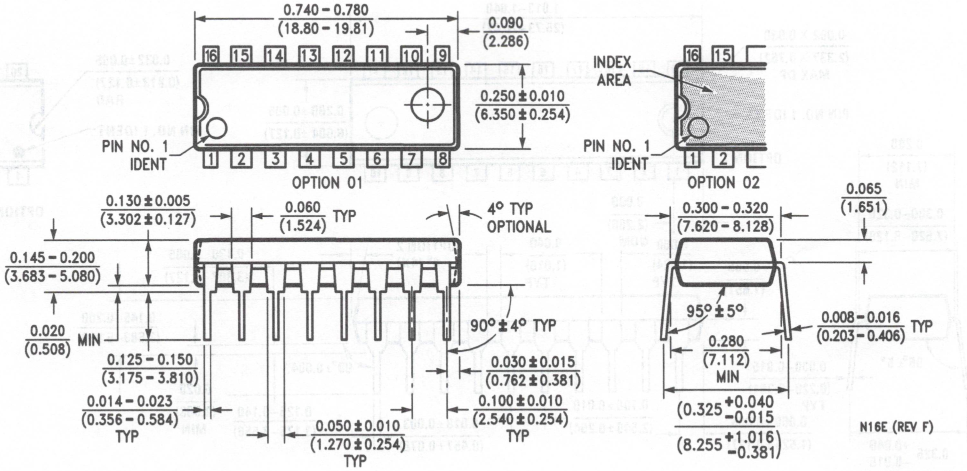
14 Lead Molded Dual-In-Line Package (N)
NS Package Number N14A


0.740 – 0.770
(18.80 – 19.56)
0.090
(2.286)
14 13 12 11 10 9 8
0.250 ± 0.010
(6.350 ± 0.254)
PIN NO. 1 IDENT
1 2 3 4 5 6 7
0.092 (2.337) DIA
0.030 (0.762) MAX DEPTH
OPTION 1
INDEX AREA
PIN NO. 1 IDENT
14 13 12
1 2 3
OPTION 02
0.135 ± 0.005
(3.429 ± 0.127)
0.145 – 0.200
(3.683 – 5.080)
0.060
(1.524) TYP
4° TYP OPTIONAL
0.020
(0.508)
MIN
0.125 – 0.150
(3.175 – 3.810)
90° ± 4° TYP
0.075 ± 0.015
(1.905 ± 0.381)
0.014 – 0.023
(0.356 – 0.584) TYP
0.100 ± 0.010
(2.540 ± 0.254) TYP
0.050 ± 0.010
(1.270 – 0.254) TYP
0.300 – 0.320
(7.620 – 8.128)
0.065
(1.651)
95° ± 5°
0.008 – 0.016
(0.203 – 0.406) TYP
0.280
(7.112)
MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
N14A (REV F)

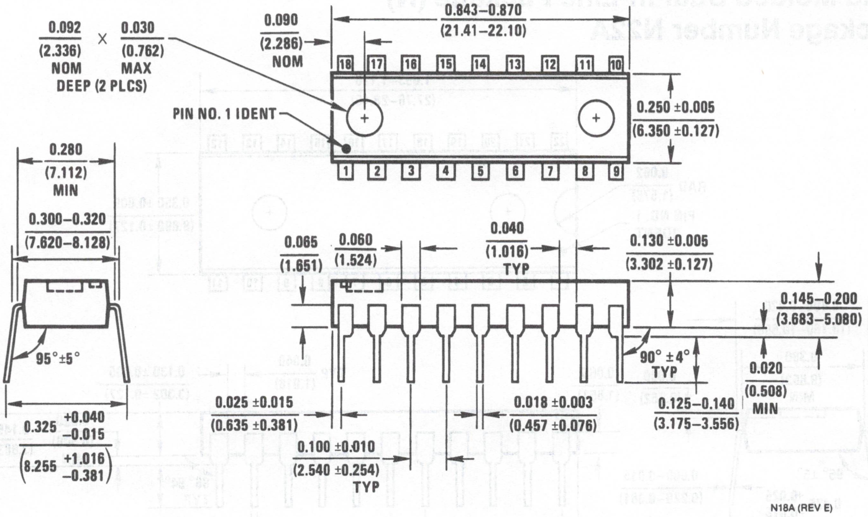
16 Lead Molded Dual-In-Line Package (N)
NS Package Number N16A


0.843–0.870
(21.41–22.10)
0.090
(2.286)
NOM
0.092
(2.337)
DIA NOM
(2X)
PIN NO. 1 IDENT
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
0.250 ±0.005
(6.350 ±0.127)
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
0.030
(0.762)
MAX
95° ±5°
0.009–0.015
(0.229–0.381)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.065
(1.651)
0.060
(1.524)
0.040
(1.016)
TYP
0.130 ±0.005
(3.302 ±0.127)
0.145–0.200
(3.683–5.080)
90° ±4°
TYP
0.020
(0.508)
MIN
0.075 ±0.015
(1.905 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.125–0.140
(3.175–3.556)
0.100 ±0.010
(2.540 ±0.254)
N16A (REV E)

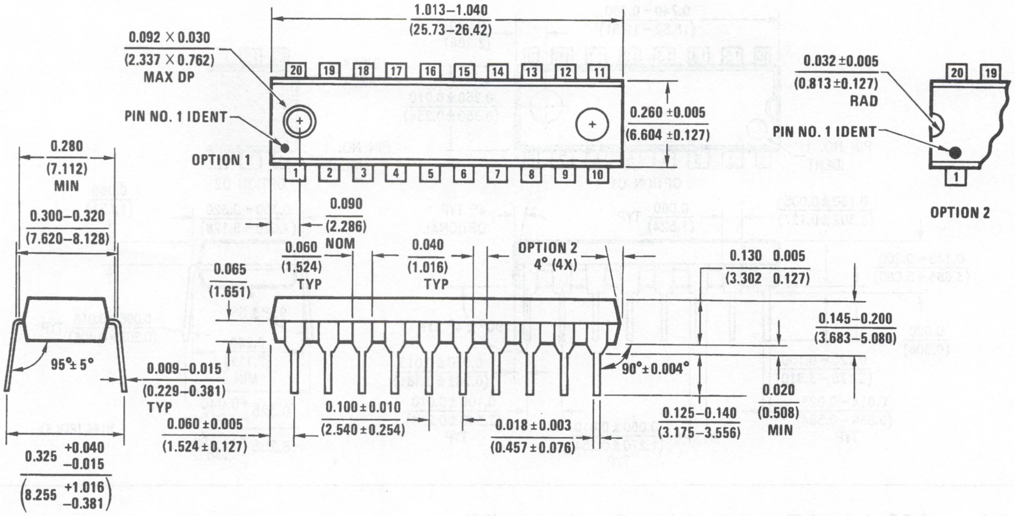
16 Lead Molded Dual-In-Line Package (N)
NS Package Number N16E


0.740 – 0.780
(18.80 – 19.81)
0.090
(2.286)
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
0.250 ± 0.010
(6.350 ± 0.254)
PIN NO. 1
IDENT
OPTION 01
INDEX
AREA
PIN NO. 1
IDENT
OPTION 02
0.130 ± 0.005
(3.302 ± 0.127)
0.060
(1.524)
TYP
4° TYP
OPTIONAL
0.145 – 0.200
(3.683 – 5.080)
0.020
(0.508)
MIN
0.125 – 0.150
(3.175 – 3.810)
0.014 – 0.023
(0.356 – 0.584)
TYP
0.050 ± 0.010
(1.270 ± 0.254)
TYP
90° ± 4° TYP
0.030 ± 0.015
(0.762 ± 0.381)
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.300 – 0.320
(7.620 – 8.128)
0.065
(1.651)
95° ± 5°
0.280
(7.112)
MIN
0.008 – 0.016
(0.203 – 0.406)
TYP
(0.325 +0.040 −0.015)
(8.255 +1.016 −0.381)
N16E (REV F)

18 Lead Molded Dual-In-Line Package (N)
NS Package Number N18A

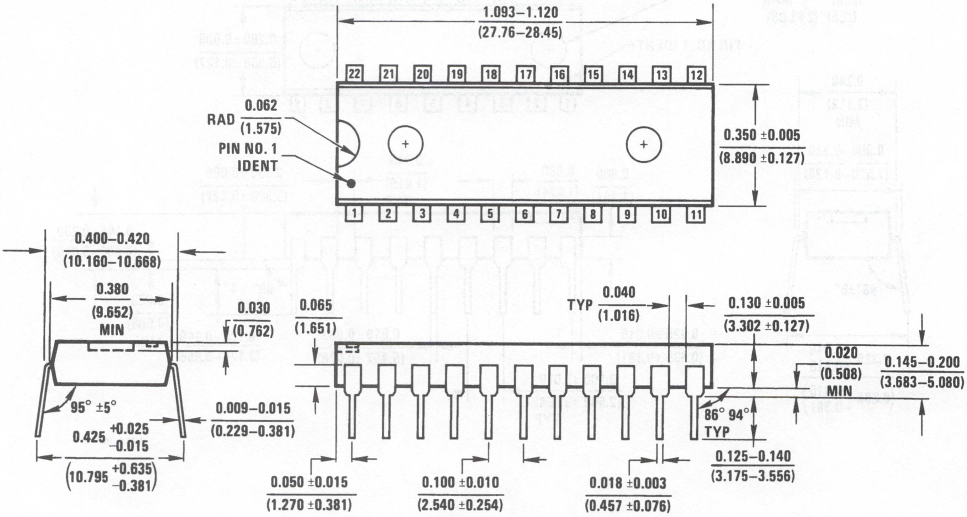

0.092
(2.336)
NOM
×
0.030
(0.762)
MAX
DEEP (2 PLCS)
0.090
(2.286)
NOM
0.843–0.870
(21.41–22.10)
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9
PIN NO. 1 IDENT
0.250 ±0.005
(6.350 ±0.127)
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
95°±5°
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.065
(1.651)
0.060
(1.524)
0.040
(1.016)
TYP
0.130 ±0.005
(3.302 ±0.127)
0.145–0.200
(3.683–5.080)
90° ±4°
TYP
0.020
(0.508)
MIN
0.125–0.140
(3.175–3.556)
0.025 ±0.015
(0.635 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.100 ±0.010
(2.540 ±0.254)
TYP
N18A (REV E)

20 Lead Molded Dual-In-Line Package (N)
NS Package Number N20A


1.013–1.040
(25.73–26.42)
0.092 × 0.030
(2.337 × 0.762)
MAX DP
PIN NO. 1 IDENT
OPTION 1
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
0.260 ±0.005
(6.604 ±0.127)
0.032 ±0.005
(0.813 ±0.127)
RAD
PIN NO. 1 IDENT
OPTION 2
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
0.090
(2.286)
NOM
0.060
(1.524)
TYP
0.065
(1.651)
0.040
(1.016)
TYP
OPTION 2
4° (4X)
0.130 0.005
(3.302 0.127)
0.145–0.200
(3.683–5.080)
95° ± 5°
0.009–0.015
(0.229–0.381)
TYP
90° ± 0.004°
0.020
(0.508)
MIN
0.100 ± 0.010
(2.540 ± 0.254)
0.018 ± 0.003
(0.457 ± 0.076)
0.125–0.140
(3.175–3.556)
0.060 ± 0.005
(1.524 ± 0.127)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

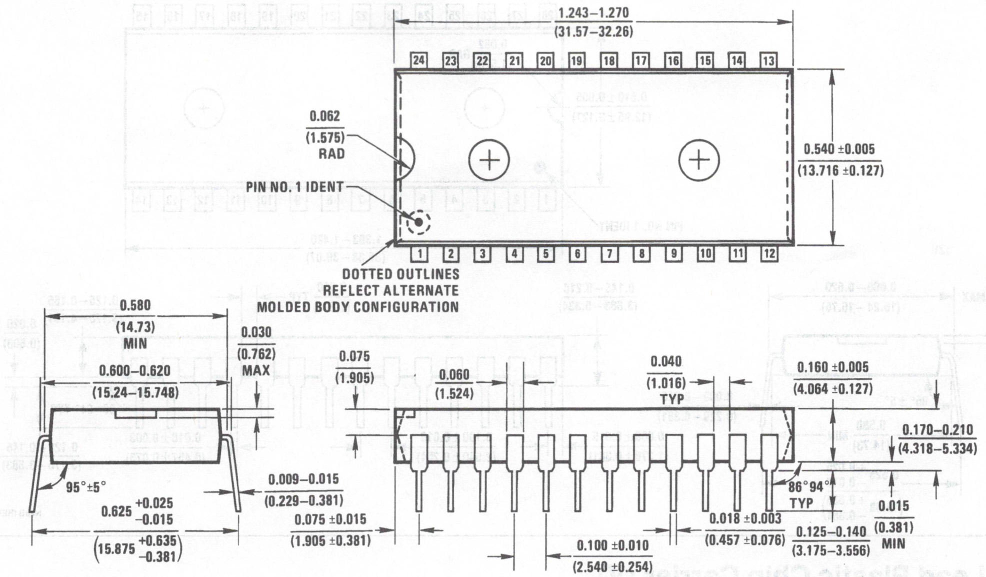
N20A (REV G)

22 Lead Molded Dual-In-Line Package (N)
NS Package Number N22A


1.093–1.120
(27.76–28.45)
22
21
20
19
18
17
16
15
14
13
12
1
2
3
4
5
6
7
8
9
10
11
RAD 0.062
(1.575)
PIN NO. 1
IDENT
0.350 ±0.005
(8.890 ±0.127)
0.400–0.420
(10.160–10.668)
0.380
(9.652)
MIN
0.030
(0.762)
0.065
(1.651)
TYP 0.040
(1.016)
0.130 ±0.005
(3.302 ±0.127)
0.020
(0.508)
MIN
0.145–0.200
(3.683–5.080)
95° ±5°
0.009–0.015
(0.229–0.381)
0.425 +0.025 −0.015
(10.795 +0.635 −0.381)
86° 94°
TYP
0.125–0.140
(3.175–3.556)
0.050 ±0.015
(1.270 ±0.381)
0.100 ±0.010
(2.540 ±0.254)
0.018 ±0.003
(0.457 ±0.076)

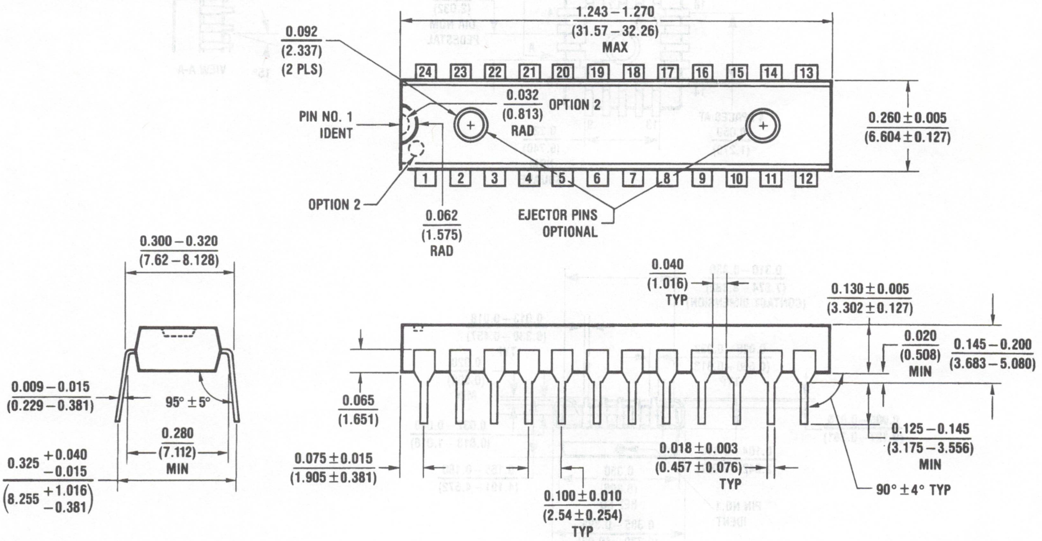
N22A (REV D)

24 Lead Molded Dual-In-Line Package (N)
NS Package Number N24A


1.243–1.270
(31.57–32.26)
24 23 22 21 20 19 18 17 16 15 14 13
0.062
(1.575)
RAD
PIN NO. 1 IDENT
0.540 ±0.005
(13.716 ±0.127)
1 2 3 4 5 6 7 8 9 10 11 12
DOTTED OUTLINES
REFLECT ALTERNATE
MOLDED BODY CONFIGURATION
0.580
(14.73)
MIN
0.030
(0.762)
MAX
0.600–0.620
(15.24–15.748)
0.075
(1.905)
0.060
(1.524)
0.040
(1.016)
TYP
0.160 ±0.005
(4.064 ±0.127)
0.170–0.210
(4.318–5.334)
95°±5°
0.009–0.015
(0.229–0.381)
0.625 +0.025 −0.015
(15.875 +0.635 −0.381)
0.075 ±0.015
(1.905 ±0.381)
86°94°
TYP
0.018 ±0.003
(0.457 ±0.076)
0.125–0.140
(3.175–3.556)
0.015
(0.381)
MIN
0.100 ±0.010
(2.540 ±0.254)

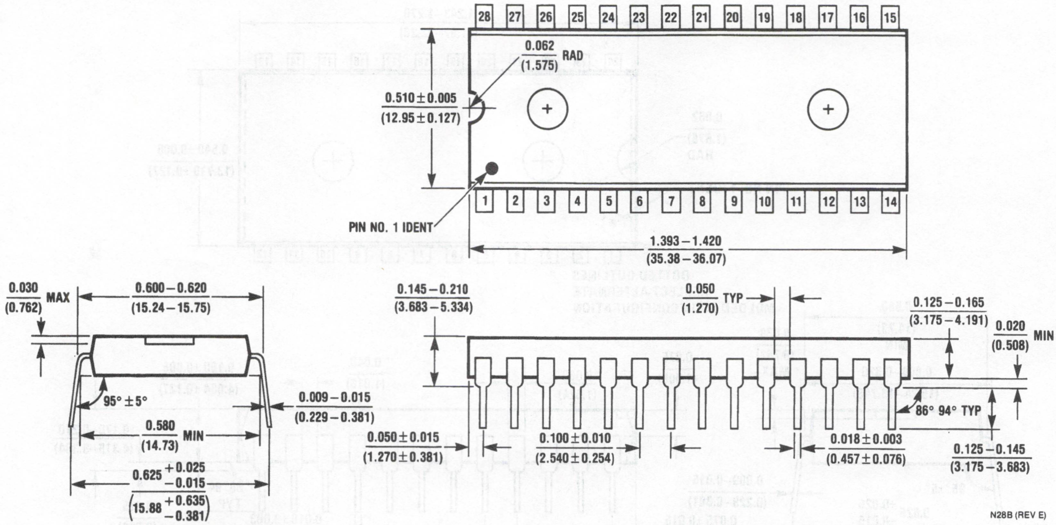
N24A (REV E)

24 Lead Skinny Dual-In-Line Package (0.300″ Centers Molded) (N)
NS Package Number N24C

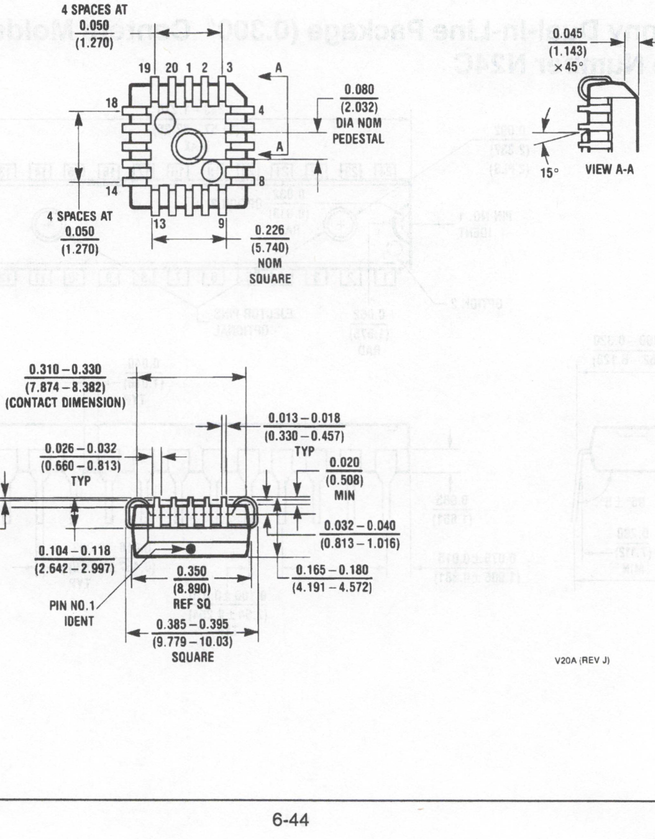

0.092
(2.337)
(2 PLS)
1.243 – 1.270
(31.57 – 32.26)
MAX
24 23 22 21 20 19 18 17 16 15 14 13
0.032
(0.813)
RAD
OPTION 2
PIN NO. 1
IDENT
0.260 ± 0.005
(6.604 ± 0.127)
1 2 3 4 5 6 7 8 9 10 11 12
OPTION 2
0.062
(1.575)
RAD
EJECTOR PINS
OPTIONAL
0.300 – 0.320
(7.62 – 8.128)
0.040
(1.016)
TYP
0.130 ± 0.005
(3.302 ± 0.127)
0.020
(0.508)
MIN
0.145 – 0.200
(3.683 – 5.080)
0.009 – 0.015
(0.229 – 0.381)
95° ± 5°
0.065
(1.651)
0.280
(7.112)
MIN
0.125 – 0.145
(3.175 – 3.556)
MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.075 ± 0.015
(1.905 ± 0.381)
0.018 ± 0.003
(0.457 ± 0.076)
TYP
0.100 ± 0.010
(2.54 ± 0.254)
TYP
90° ± 4° TYP

N24C (REV F)

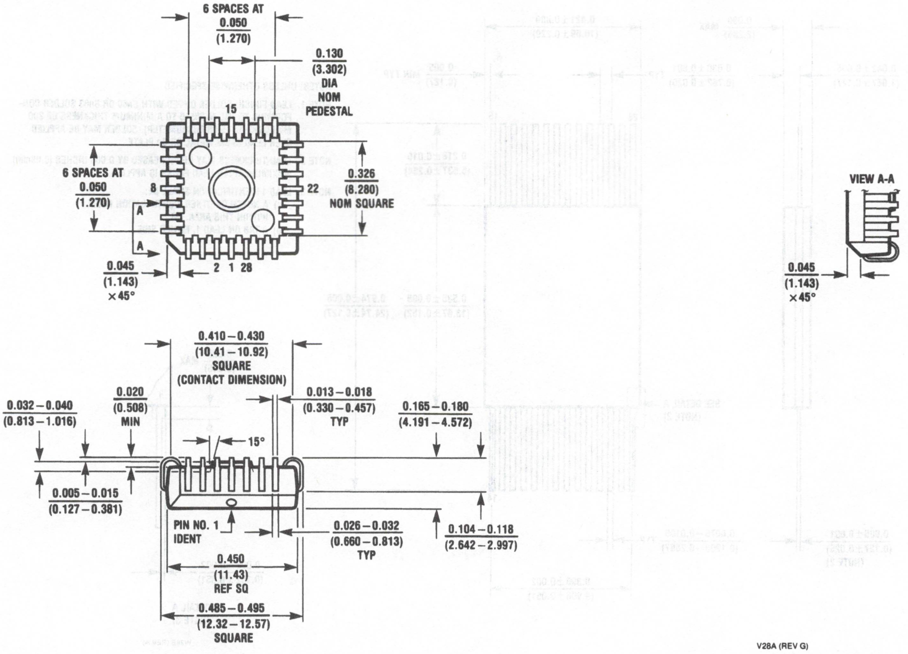
28 Lead Molded Dual-In-Line Package (N)
NS Package Number N28B


28 27 26 25 24 23 22 21 20 19 18 17 16 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14
0.062 (1.575) RAD
0.510 ± 0.005 (12.95 ± 0.127)
PIN NO. 1 IDENT
1.393 − 1.420 (35.38 − 36.07)
0.030 (0.762) MAX
0.600 − 0.620 (15.24 − 15.75)
95° ± 5°
0.580 (14.73) MIN
0.625 +0.025 −0.015 (15.88 +0.635 −0.381)
0.009 − 0.015 (0.229 − 0.381)
0.145 − 0.210 (3.683 − 5.334)
0.050 (1.270) TYP
0.125 − 0.165 (3.175 − 4.191)
0.020 (0.508) MIN
86° 94° TYP
0.050 ± 0.015 (1.270 ± 0.381)
0.100 ± 0.010 (2.540 ± 0.254)
0.018 ± 0.003 (0.457 ± 0.076)
0.125 − 0.145 (3.175 − 3.683)
N28B (REV E)

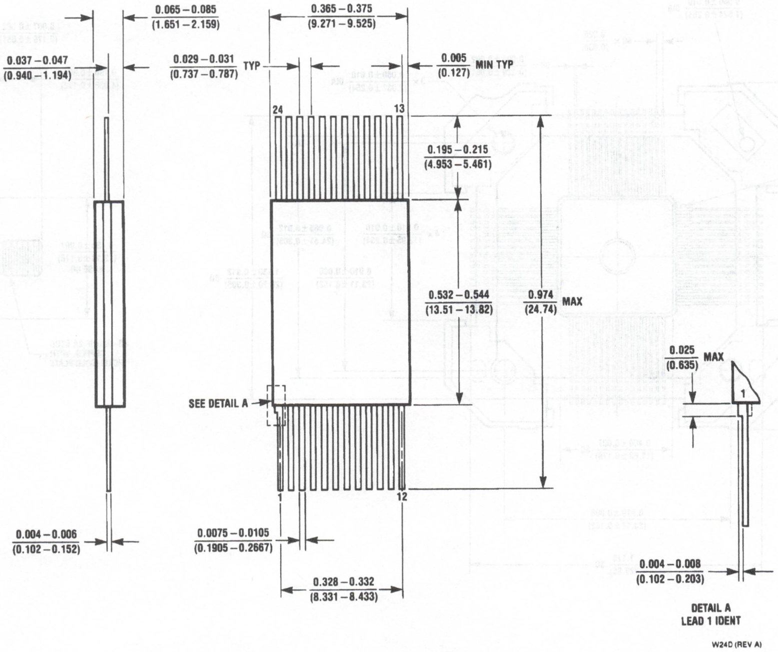
20 Lead Plastic Chip Carrier (V)
NS Package Number V20A


4 SPACES AT 0.050 (1.270)
19 20 1 2 3
18
4
8
14
13
9
A
A
0.080 (2.032) DIA NOM PEDESTAL
0.045 (1.143) × 45°
15°
VIEW A-A
4 SPACES AT 0.050 (1.270)
0.226 (5.740) NOM SQUARE
0.310 − 0.330 (7.874 − 8.382) (CONTACT DIMENSION)
0.013 − 0.018 (0.330 − 0.457) TYP
0.026 − 0.032 (0.660 − 0.813) TYP
0.020 (0.508) MIN
0.005 − 0.015 (0.127 − 0.381)
0.032 − 0.040 (0.813 − 1.016)
0.104 − 0.118 (2.642 − 2.997)
0.350 (8.890) REF SQ
0.165 − 0.180 (4.191 − 4.572)
PIN NO.1 IDENT
0.385 − 0.395 (9.779 − 10.03) SQUARE
V20A (REV J)

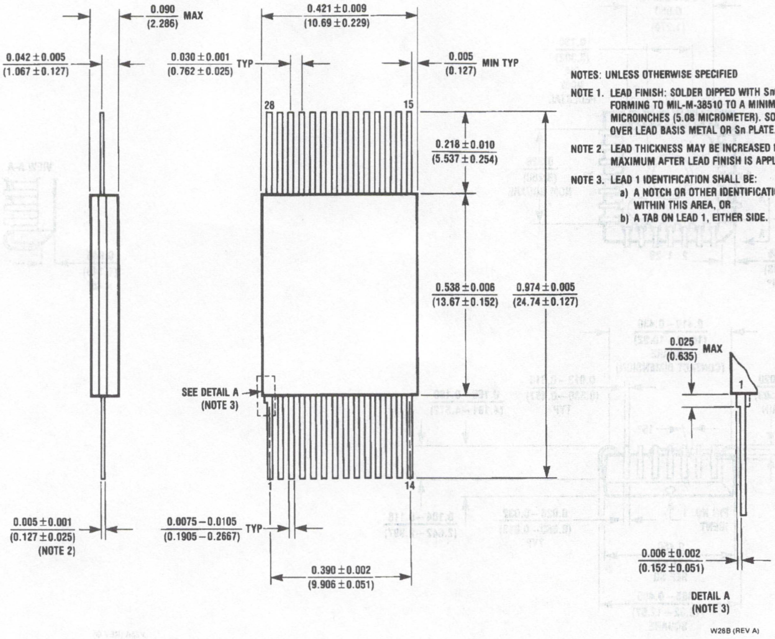
28 Lead Plastic Chip Carrier (V)
NS Package Number V28A


6 SPACES AT
0.050
(1.270)
0.130
(3.302)
DIA
NOM
PEDESTAL
15
6 SPACES AT
0.050
(1.270)
8
22
0.326
(8.280)
NOM SQUARE
A
A
2 1 28
0.045
(1.143)
×45°
VIEW A-A
0.045
(1.143)
×45°
0.410–0.430
(10.41–10.92)
SQUARE
(CONTACT DIMENSION)
0.032–0.040
(0.813–1.016)
0.020
(0.508)
MIN
0.013–0.018
(0.330–0.457)
TYP
0.165–0.180
(4.191–4.572)
15°
0.005–0.015
(0.127–0.381)
PIN NO. 1
IDENT
0.026–0.032
(0.660–0.813)
TYP
0.104–0.118
(2.642–2.997)
0.450
(11.43)
REF SQ
0.485–0.495
(12.32–12.57)
SQUARE
V28A (REV G)

24 Lead Cerpac, Fine Pitch Package (W)
NS Package Number W24D


0.065–0.085
(1.651–2.159)
0.365–0.375
(9.271–9.525)
0.037–0.047
(0.940–1.194)
0.029–0.031
(0.737–0.787)
TYP
0.005
(0.127)
MIN TYP
24
13
0.195–0.215
(4.953–5.461)
0.532–0.544
(13.51–13.82)
0.974
(24.74)
MAX
0.025
(0.635)
MAX
1
SEE DETAIL A
1
12
0.004–0.006
(0.102–0.152)
0.0075–0.0105
(0.1905–0.2667)
0.328–0.332
(8.331–8.433)
0.004–0.008
(0.102–0.203)
DETAIL A
LEAD 1 IDENT
W24D (REV A)

28 Lead Cerpac, Fine Pitch Package (W)
NS Package Number W28B


0.090 (2.286) MAX
0.421±0.009 (10.69±0.229)
0.042±0.005 (1.067±0.127)
0.030±0.001 (0.762±0.025) TYP
0.005 (0.127) MIN TYP
28
15
0.218±0.010 (5.537±0.254)
0.538±0.006 (13.67±0.152)
0.974±0.005 (24.74±0.127)
SEE DETAIL A (NOTE 3)
1
14
0.005±0.001 (0.127±0.025) (NOTE 2)
0.0075–0.0105 (0.1905–0.2667) TYP
0.390±0.002 (9.906±0.051)
0.025 (0.635) MAX
1
0.006±0.002 (0.152±0.051)
DETAIL A (NOTE 3)
W28B (REV A)

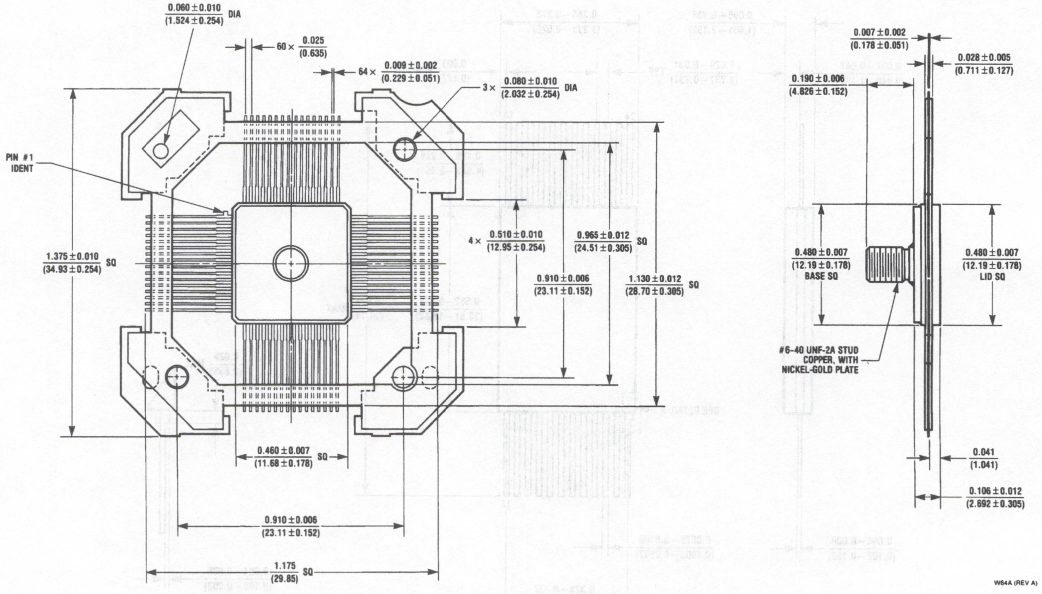
NOTES: UNLESS OTHERWISE SPECIFIED

NOTE 1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES (5.08 MICROMETER). SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.

NOTE 2. LEAD THICKNESS MAY BE INCREASED BY 0.003 INCHES (0.08mm). MAXIMUM AFTER LEAD FINISH IS APPLIED.

NOTE 3. LEAD 1 IDENTIFICATION SHALL BE:
- a) A NOTCH OR OTHER IDENTIFICATION MARK WITHIN THIS AREA, OR
- b) A TAB ON LEAD 1, EITHER SIDE.

64 Lead Cerquad Flatpak (W)
NS Package Number W64A


0.060±0.010 (1.524±0.254) DIA
60× 0.025 (0.635)
64× 0.009±0.002 (0.229±0.051)
3× 0.080±0.010 (2.032±0.254) DIA
PIN #1 IDENT
1.375±0.010 (34.93±0.254) SQ
4× 0.510±0.010 (12.95±0.254)
0.965±0.012 (24.51±0.305) SQ
0.910±0.006 (23.11±0.152)
1.130±0.012 (28.70±0.305) SQ
0.460±0.007 (11.68±0.178) SQ
0.910±0.006 (23.11±0.152)
1.175 (29.85) SQ
0.007±0.002 (0.178±0.051)
0.028±0.005 (0.711±0.127)
0.190±0.006 (4.826±0.152)
0.480±0.007 (12.19±0.178) BASE SQ
0.480±0.007 (12.19±0.178) LID SQ
#6-40 UNF-2A STUD COPPER, WITH NICKEL-GOLD PLATE
0.041 (1.041)
0.106±0.012 (2.692±0.305)
W64A (REV A)

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